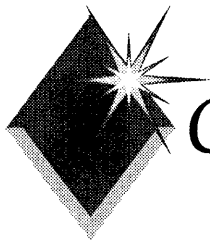


The Architecture of the NS486 Integrated Processor

Mario Nemirovsky
Integrated Processor Unit
National Semiconductor Corp.
2900 Semiconductor Dr.
Santa Clara, CA 95052



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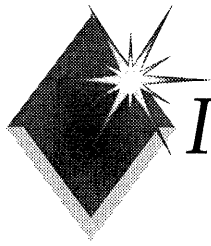


Outline

- ◆ Introduction
- ◆ Objectives
- ◆ Architecture
- ◆ System Overview
- ◆ Performance
- ◆ Conclusions



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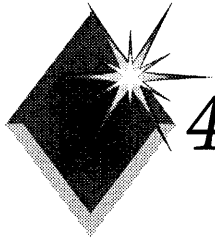
Introduction

- ◆ 486 CPU core for the Intelligent Device Market
- ◆ Core optimization for best cost/performance ratio



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486 Architectures

- ◆ Large ISA
- ◆ Sophisticated Addressing Modes
- ◆ Complex Protection Mechanisms



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Objectives

- ◆ Compatibility to 486 architecture
- ◆ Low cost implementation
- ◆ Schedule
- ◆ High performance
- ◆ Processor targeted for embedded applications



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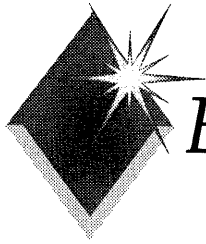
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Architectural Goals

- ◆ Target frequency 25 MHz
- ◆ 486 performance
- ◆ No floating point





Execution Pipeline

◆ Simple pipeline

- ◆ Three stages (decode, execute, write back)

time	1	2	3	4	5
Decode	ADD	SUB	INC		
Execute		ADD	SUB	INC	
Write			ADD	SUB	INC



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Fast Memory Access

- ◆ Single cycle address computation
- ◆ DRAM page memory access
 - ◆ Single cycle access to DRAM
- ◆ e.g., MOV ax,mem
MOV bx,mem
INC ax

time	1	2	3	4	5
Decode	MOV ax	MOV bx	INC ax		
Execute		MOV ax	MOV bx	INC ax	
Write			MOV ax	MOV bx	INC ax
Mem				MOV ax	MOV bx



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NS486 Architecture

- ◆ Architecture optimized for embedded applications
 - ◆ Single cycle reads, writes, pushes, and pops
 - ◆ String operations faster than 486
- ◆ Instruction cache (1 Kbytes)

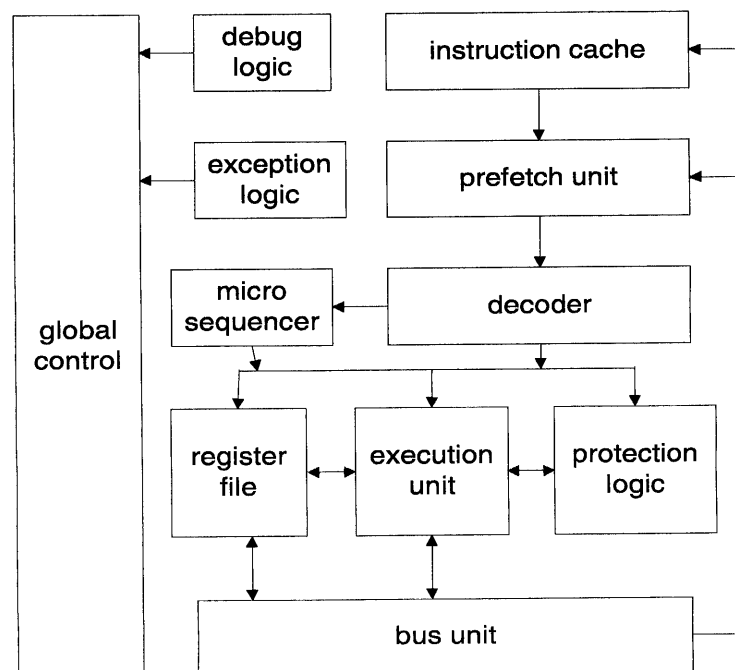
time	1	2	3	4	5	6
Decode	ADD	JMP			Target	Target
Execute		ADD	JMP			
Write			ADD	JMP		
Mem					JMP	



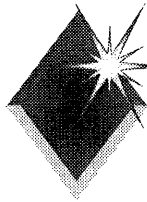
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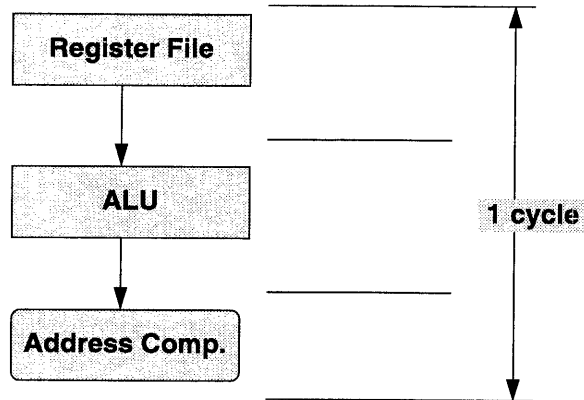
NS486 Block Diagram



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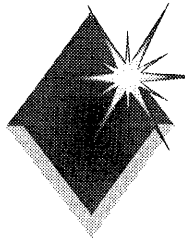


Pipeline Timing




Performance Analysis

- ◆ Objective: To optimize the design to execute the target workload
- ◆ Develop representative benchmarks
- ◆ Analyze benchmark instruction mix



Instruction Timing

instr	addressing mode	i386SX	i386DX	Cx486DLC	i486DX	NS486
<i>data transfer</i>						
MOV	reg-to-reg	2	2	1	1	1
MOV	mem-to-reg	6	4	2	1	1
MOV	reg-to-mem	4	2	2	1	1
POP	reg	6	6	3	4	1
PUSH	reg	4	4	2	1	1
REPNE CMPS		5+9c	5+9c	5+8c	7+7c	7+5c
REP MOV		7+4c	7+4c	5+4c	12+3c	5+4c
REPNE SCAS		5+8c	5+8c	4+5c	7+5c	5+4c
<i>arithmetic/logic</i>						
ALU	reg-to-reg	2	2	1	1	1
ALU	mem-to-reg	10	6	3	2	3
ALU	reg-to-mem	11	7	3	3	3
MULT	byte	12/17	12/17	3	12/18	11/13
MULT	word	12/25	12/25	3	12/26	19/21
MULT	dword	12/41	12/41	7	12/42	35/37
SHL,SHR	reg by 1	3	3	2	3	1
SHL,SHR	reg by CL	3	3	3	3	1
CMP	reg-to-reg	2	2	1	1	1
CMP	reg-to-mem	5	5	3	2	3
STC,CLC		2	2	1	2	1
<i>control</i>						
Jcc	relative	7+m/3	7+m/3	6/1	3/1	3/1
JMP	relative	7+m	7+m	6	3	3
JMP	reg indirect	7+m	7+m	6	5	3
CALL	relative	11+m	9+m	7	3	4
CALL	reg indirect	11+m	9+m	8	5	4
RET	near	12+m	12+m	10	5	4
LOOP		11+m	11+m	9/3	7/6	6/4

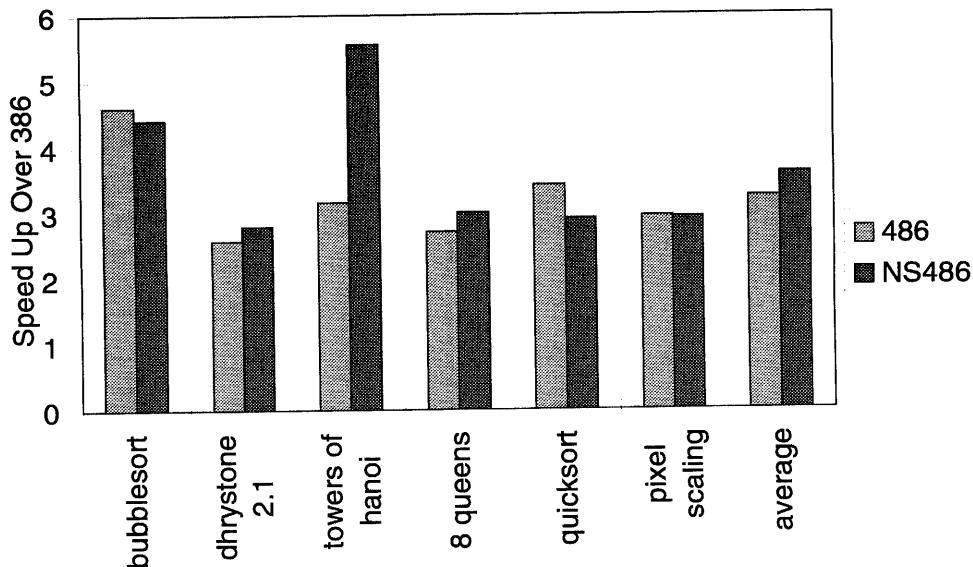
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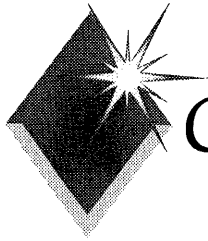
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Benchmark Results



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Conclusions

- ◆ NS486 core is much simpler and smaller than the Intel 486.
- ◆ Performance is close to a 486 running at the same frequency
- ◆ Enhanced performance can be achieved through adding extra caches and enhancing the bus to 32-bits.



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Die Picture



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