

Final Program

Monday, August 14, 1995—Memorial Auditorium

9:00–9:15	Welcome and Opening Remarks Nam Ling, General Chair Hasan S. AlKhatib and Norman P. Jouppi, Program Co-Chairs		
9:15–10:45	Session 1: Embedded Processors Session Chair: Robert Garner, Sun Microsystems		page
1.1	The First Superscalar 29K™ Family Member B. McMinn, Advanced Micro Devices		1
1.2	The Architecture of the NS486 Integrated Processor M. D. Nemirovsky, National Semiconductor		11
1.3	The MiniRISC™ CW4010: A Superscalar MIPS Processor ASIC Core , P. Cobb, J. Cesana, LSI Logic		19
10:45–11:15	Break		
11:15–12:15	Keynote Address: “Nanometers and Gigabucks” Gordon Moore, Chairman of Intel Corporation		
12:15–1:45	Lunch		
1:45–3:15	Session 2: x86 Processors Session Chair: Mark Horowitz, Stanford University		
2.1	Optimizing the P6 Pipeline , D. Papworth, Intel Corporation		31
2.2	AMD–K5™ Microprocessor D. Christie, Advanced Micro Devices		41
2.3	Building a Better Beast: Native vs. RISC-like vs. VLIW Methods of Implementing x86 Microprocessors T. Garibay, Cyrix		49
3:15–3:45	Break		
3:45–5:15	Session 3: RISC–1 Session Chair: Winfried W. Wilcke, HaL Computer Systems		
3.1	Performance Evaluation of the Superscalar Speculative Execution HaL SPARC64 Processor A. Essen, S. Goldstein, HaL Computer Systems		59
3.2	SPARC64™+: HAL’s Second Generation 64-bit SPARC Processor G. W. Shen, HaL Computer Systems		75
3.3	Memory Performance Features of the 64-bit PA-8000 B. Naas, Hewlett-Packard		87
5:15–7:00	Monday Evening Buffet Dinner		
7:00–9:00	Evening Panel Session: What is the Role of Competing Architectures in an x86 World Order? Moderator: John Wharton, Consultant/Analyst, Applications Research. Panel members: Keith Diefendorff, Senior Member Technical Staff, Motorola; David Ditzel, President and CEO, Transmeta Corporation; John Novitsky, Director, CPU Products Group, Micro-Module Systems; Nick Tredennick, CEO, TechNerds International; Pete Wilson, Director, Microsystems Architecture, Groupe Bull		

Final Program

Tuesday, August 15, 1995—Memorial Auditorium

9:00–10:30	Session 4: MPEG , Session Chair: Vivian Shen, Hewlett-Packard	page
4.1	A Two-Chip Real-Time MPEG2 Video Encoder with Wide Range Motion Estimation , T. Kondo, K. Suguri, M. Ikeda, T. Abe, H. Matsuda, T. Okubo, K. Ogura, NTT LSI Laboratories; Y. Tashiro, NTT Human Interface Laboratories	95
4.2	VLSI Architecture of the I-Frame Encoder for the MPEG-2 Video Compression , A. Ngai, IBM	103
4.3	S3 Single Chip MPEG-1 Audio/Video Decoder C. Stearns, S3 Inc.	111
10:30–11:00	Break	
11:00–12:30	Session 5: Graphics and Compression Session Chair: Shanker Singh, IBM	
5.1	3D Graphics Processor Chip Set , M. Awaga, Fujitsu Limited	121
5.2	A Single Chip Video CD with Hi-Fi Audio for Consumer Applications J. Fandrianto, B. Martin, Integrated Information Technology	135
5.3	Fast and Highly Reliable IBMLZ1 Compression Chip and Algorithm for Storage J. M. Cheng, L. M. Duyanovich, IBM	143 paper: 155
12:30–2:00	Lunch	
2:00–4:00	Session 6: Parallel and Vector Processing Session Chair: Alan Jay Smith, UC Berkeley	
6.1	Hot Compilers for Future Hot Chips , S. P. Amarisinghe, J. A. M. Anderson, R. S. French, M. W. Hall, M. S. Lam, S. W. Liao, B. R. Murphy, C. W. Tseng, C. S. Wilson, R. P. Wilson, Stanford Univ.	167
6.2	Scylla: A Memory Controller with Integrated Protocol Engines for Distributed Shared Memory Support A. Nowatzky, G. Aybay, M. Browne, B. Radke, S. Vishin, Sun Microsystems	179
6.3	The T0 Vector Microprocessor , K. Asanovic, J. Beck, B. Irissou, B. E. D. Kingsbury, N. Morgan, J. Wawrzynek, UC Berkeley	187
6.4	A 150 MHz Superscalar RISC Processor with Pseudo Vector Processing Feature , K. Saito, M. Hashimoto, K. Matsubara, H. Sawamoto, R. Yamagata, T. Kumagai, E. Kamada, T. Hotta, T. Nakano, Hitachi, Ltd.; T. Isobe, Hitachi Computer Engineering Co., Ltd.; K. Nakazawa, University of Tsukuba	197
4:00–4:30	Break	
4:30–6:00	Session 7: RISC-2 , Session Chair: Donald Alpert, Intel Corp.	
7.1	UltraSPARC™-I: A 64-bit Superscalar Processor with Multimedia Support , M. Tremblay, Sun Microsystems	207
7.2	withdrawn	
7.3	Smaller, Faster, Cooler... Evolving the PowerPC Family D. Balsler, Somerset Microprocessor Devel. Center, IBM/Motorola	217
7.4	R10000 Superscalar Microprocessor , A. Ahi, A. Borndica, G. Shippen, H. Sucar, H. Su, J. Chuang, N. Vasseghi, R. Ramchandani, R. Martin, R. Conrad, Y. Chen, K. Yeager, W. Voegtili Jr., M. Seddighnezhad, Y. Van Atta, Silicon Graphics	227
6:30	Closing Remarks	