The Thunder SPARC Processor

HOT Chips VI

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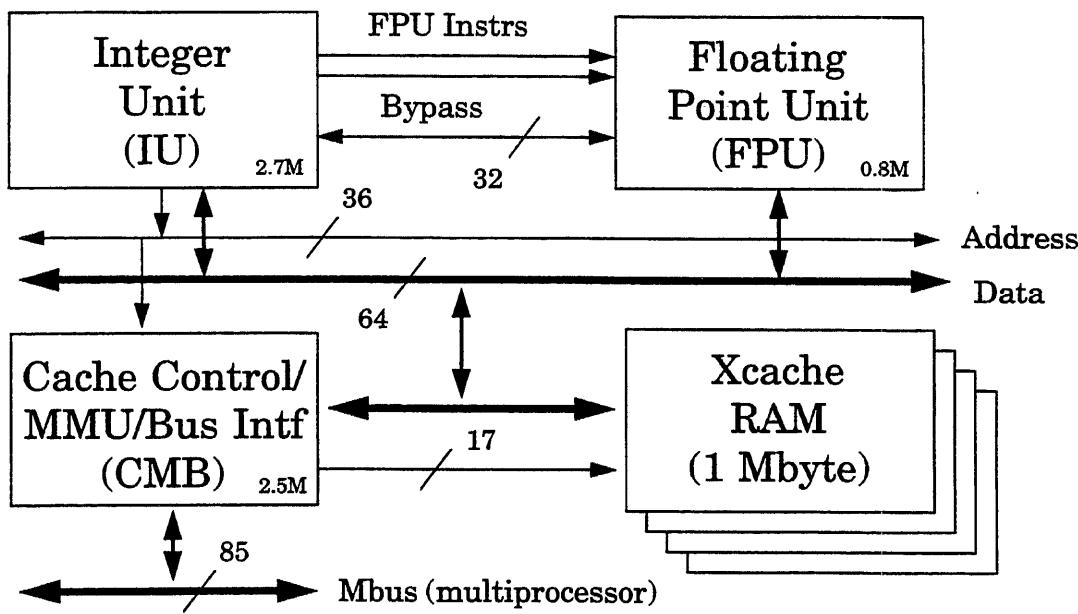
Metaflow Background

- Company founded in 1987
- Pioneers in out-of-order/speculative execution microprocessor design
- First major design contract was LSI Logic's "Lightning" SPARC chipset (completed 1991)
- "Thunder" SPARC 3-chip set is improved version of "Lightning" 4-chip set
- Project 100% funded by Hyundai Electronics
- Thunder chipset first silicon July 1993
- Patented out-of-order architecture

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Thunder SPARC Mbus Module

```
┌──────────────┐   FPU Instrs    ┌──────────────┐
│   Integer    │ ──────────────→ │   Floating   │
│    Unit      │                 │ Point Unit   │
│    (IU)      │ ←── Bypass ──── │    (FPU)     │
│        2.7M  │        32       │         0.8M │
└──────────────┘                 └──────────────┘
```

36

Address

64

Data

```
┌──────────────┐                 ┌──────────────┐
│ Cache Control/│    ←──────→    │   Xcache     │
│ MMU/Bus Intf │        17       │    RAM       │
│    (CMB)     │ ──────────────→ │  (1 Mbyte)   │
│        2.5M  │                 │              │
└──────────────┘                 └──────────────┘
```

85

Mbus (multiprocessor)

Thunder SPARC Chipset

- Superscalar fetch, issue, and execution
- Dynamic scheduling (dataflow)
- Out-of-order execution
- Speculative execution
- Above "hidden" from the programmer
- Factor of 2-3 performance advantage <u>from architecture</u>

Microprocessor Hardware Trends

● Superscalar instruction issue

● Super-pipelined execution units

● Super-fast processor clocks (>100 MHz)

● Out-of-order execution

● Speculative execution

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Out-of-Order Execution

PROGRAM ORDER   COMPLETION ORDER

```
float A, X, XX, X1
int n
.                                .
.                                .
.                                .
X1 = 1 / A;                      n = n + 1;
XX = A * A;                      X = X + A;
n = n + 1;                       XX = A * A;
X = X + A;                       X1 = 1 / A;
.                                .
.                                .
.                                .
```

Operation	Clocks
FP divide	10
FP multiply	5
FP add	3
Integer add	1

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Speculative Execution

$$\sum_{i=0}^{n} \sqrt{X_i}$$

C EXAMPLE

Speculative execution opportunity

```
for ( i = 0; i < MAX; ++i ) {
    if (X[i] < 0) error_exit();
    sum = sum + sqrt(X[i]);
}
```
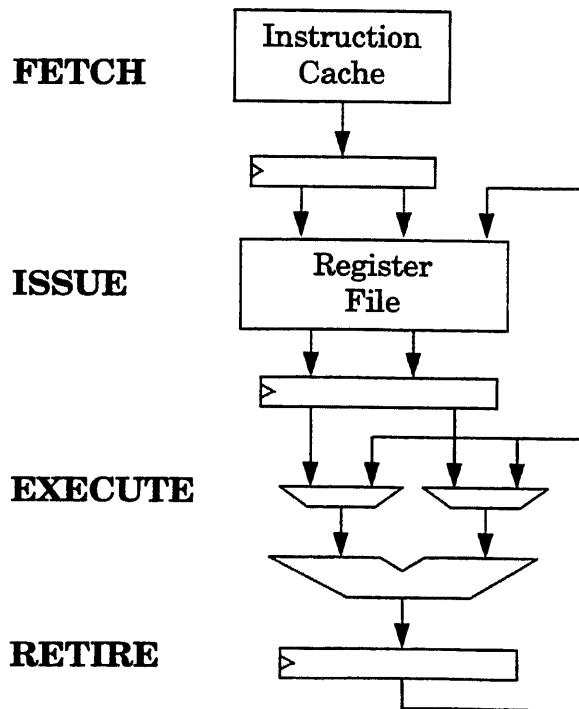
Speculative execution opportunity

FORTRAN EXAMPLE
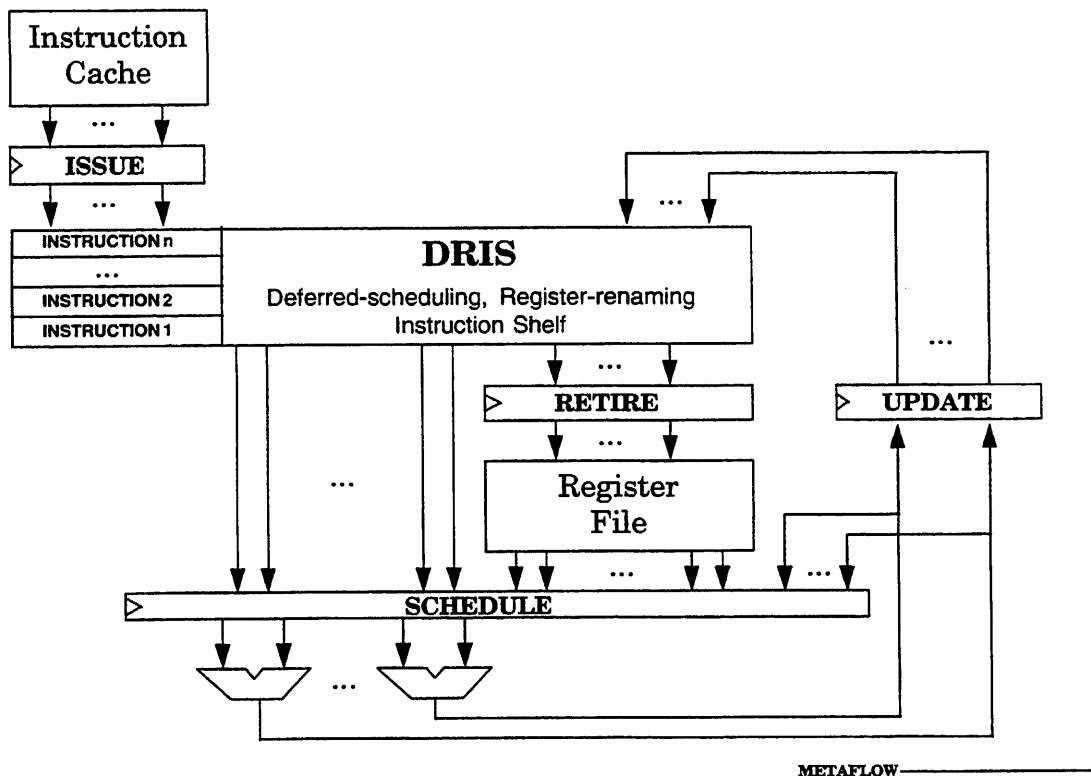
```
    DO 100 i = 1, max
    IF (X(i) .LT. 0) CALL error_exit
100 CONTINUE
```

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Conventional Pipeline

FETCH

Instruction
Cache

ISSUE

Register
File

EXECUTE

RETIRE

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Metaflow Pipeline (DRIS)

```
┌──────────────┐
│ Instruction  │
│   Cache      │
└──────────────┘
     │  ...  │
     ▼       ▼
┌──────────────┐
▷     ISSUE    │
└──────────────┘
     │  ...  │
     ▼       ▼
┌────────────┬──────────────────────────────────┐
│INSTRUCTION n│            DRIS                  │
├────────────┤  Deferred-scheduling, Register-renaming │
│    ...     │          Instruction Shelf        │
├────────────┤                                   │
│INSTRUCTION 2│                                  │
├────────────┤                                   │
│INSTRUCTION 1│                                  │
└────────────┴──────────────────────────────────┘
                         ...
                    ┌──────────────┐        ┌──────────────┐
                 ▷  │    RETIRE    │     ▷  │    UPDATE    │
                    └──────────────┘        └──────────────┘
                         ...
                    ┌──────────────┐
                    │   Register   │
                    │     File     │
                    └──────────────┘
                         ...
┌──────────────────────────────────────────────────────────┐
▷                      SCHEDULE                              │
└──────────────────────────────────────────────────────────┘
```

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Metaflow DRIS Entry

Source Operand 1

Locked	RegNum	ID

Source Operand 2

Locked	RegNum	ID
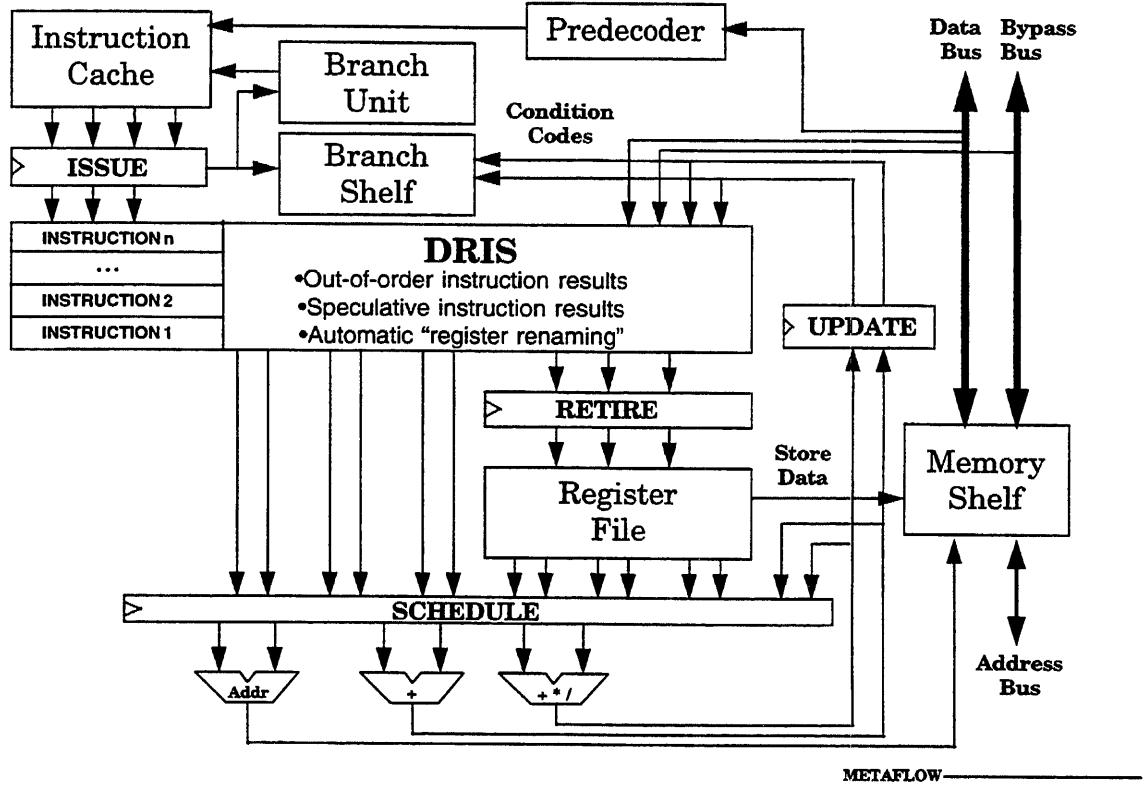
Destination

Latest	RegNum	Instruction's Results

| Dispatched	Functional Unit	Executed	Program Counter
Yes/No	Class Number	Yes/No	Content

Thunder IU

Thunder Processor Distinguishing Features

- 4 instructions issued per clock (3 integer, 2 floating point instructions and one branch)
- 8 parallel functional units (3 integer ALUs, 2 FP ALUs, 1 branch unit, 2 memory/bypass)
- Dataflow-based out-of-order instruction issue/execution (memory/ALU operations), in-order completion, precise traps and interrupts
- Speculative execution beyond unresolved conditional branches (multiple basic blocks with instant state repair on error)
- Above mechanisms transparent to executing program (strict SPARC V8 compatibility)

Thunder Unusual Features

- Eager evaluation ("folds" conditional branches)
- Multiple instances of memory locations ("memory renaming")
- Out-of-order memory references
    - Multiple simultaneous cache miss processing ("non-blocking cache")
    - Split address and data memory transactions (memory response re-ordering allowed)
- Speculative memory reads with respect to shared memory coherence restrictions (emulates "strong consistency" model)
- Uninterrupted transitions between user and supervisor modes (traps/interrupts)

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Thunder Unusual Features (continued)

Floating Point Unit (FPU)

- Variable latency FPU (early termination for divide/square root)
- Non-blocking divide and square root (concurrent add/multiply)

Branch Prediction

- Dynamic branch prediction
- Generalized loop count prediction
- Return-from-subroutine (**RET**) "folding"
- Jump-through-register prediction (**JMPL** cache)
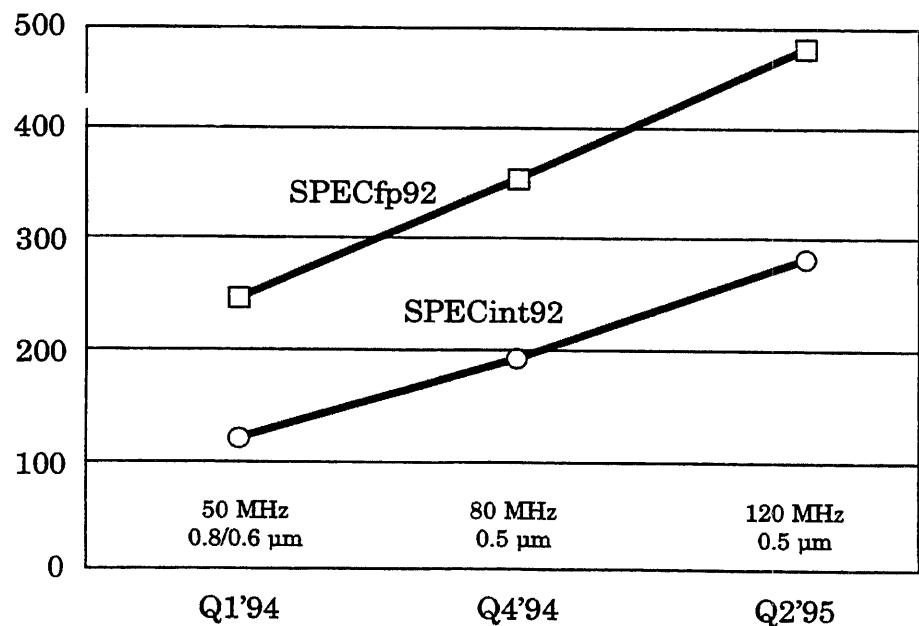
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Thunder Status

|	Thunder 1.0	Thunder 1.5
First Silicon	July/Nov 1993	Q4 1994
Foundry	VLSI Technologies	
CMOS technology	0.6/0.8 µm	0.5 µm
Metal layers	3	4
Supply voltage	5V	3.6V
Clock rate (processor)	50 MHz	80 MHz
(Mbus)	40 MHz	≤60 MHz
Die Size (mm square)	14.5/16.5	9.1/11.8
Package	IPGA (391 pins)	TBGA (600+ pins)
Methodology (data path/RAM)	Full custom	Full custom
(control logic)	Standard cell	Standard cell
(test)	JTAG/full scan	JTAG/full scan
External cache RAM (type)	"Viking"	"Pentium"
(size)	Eight 128K x 9	Eight 64K x 18
Total transistors (3 chips)	~6 million	~6 million
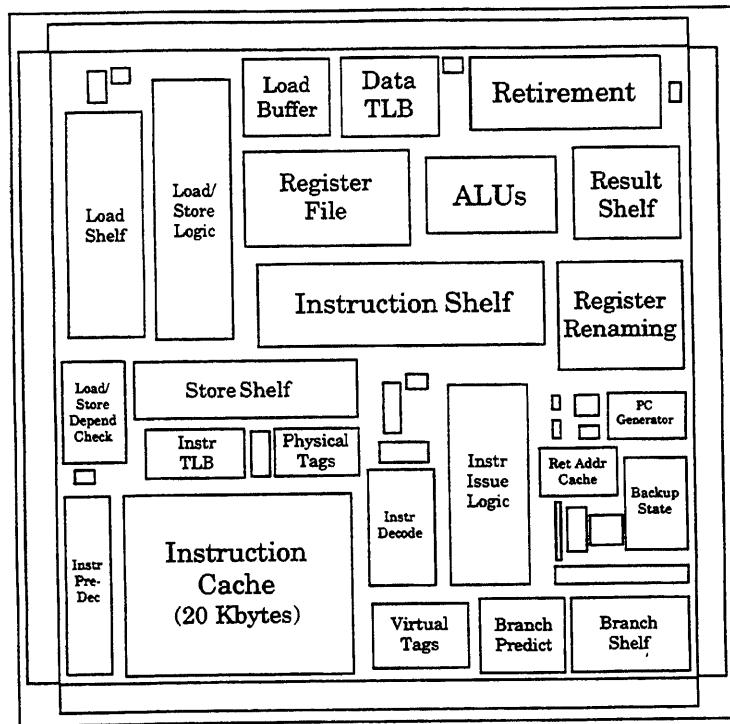
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Thunder Performance Goals

SPECfp92

SPECint92

| | 50 MHz
0.8/0.6 µm | 80 MHz
0.5 µm | 120 MHz
0.5 µm |
| Q1'94 | Q4'94 | Q2'95 |
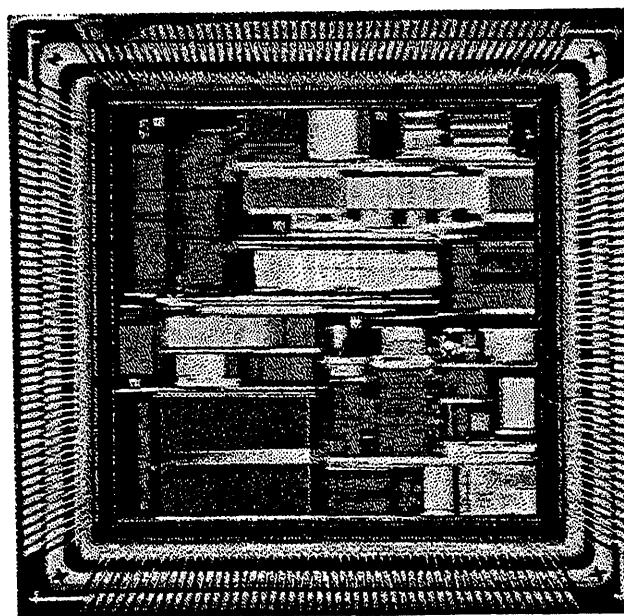
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Thunder 1.0 IU Floor Plan

Load Buffer	Data TLB	Retirement

Load Shelf
Load/Store Logic
Register File
ALUs
Result Shelf

Instruction Shelf
Register Renaming

Load/Store Depend Check
Store Shelf

Instr TLB
Physical Tags
Instr Issue Logic
PC Generator

Instr Decode
Ret Addr Cache
Backup State

Instr Pre-Dec
Instruction Cache (20 Kbytes)

Virtual Tags
Branch Predict
Branch Shelf
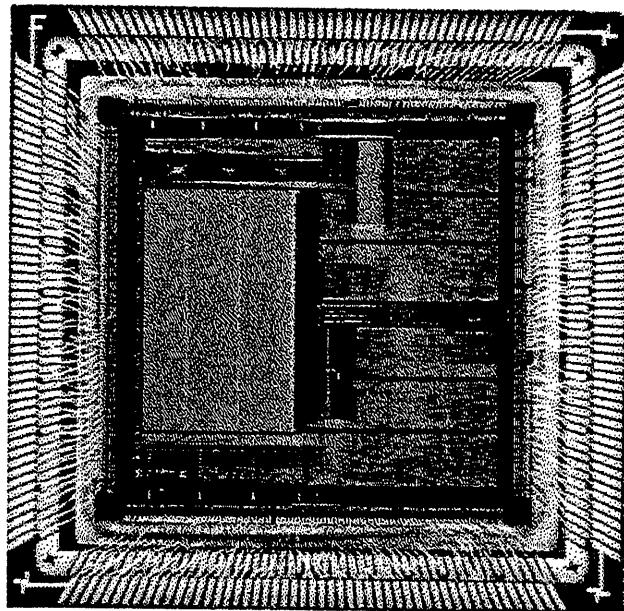
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Thunder 1.0 IU Die Photo

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Thunder 1.0 CMB Die Photo

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