# PowerPC 604™ RISC Microprocessor

Marvin Denman
Somerset Design Center



## Presentation Outline

- Overview
- Execution
- Branch Prediction
- Memory System
- Summary

## Overview

- PowerPC™ 32-bit architecture
- Targeted for Next Generation Desktop
- Four-way superscalar
- Speculative execution
- Multiprocessor Support
- Projected performance @ 100 Mhz
  - 160 SPECint92™
  - 165 SPECfp92™
- 196 $mm^2$, 0.5 um CMOS, 4 layer metal
- 3.6 Million transistors

MOTOROLA INC. IBM

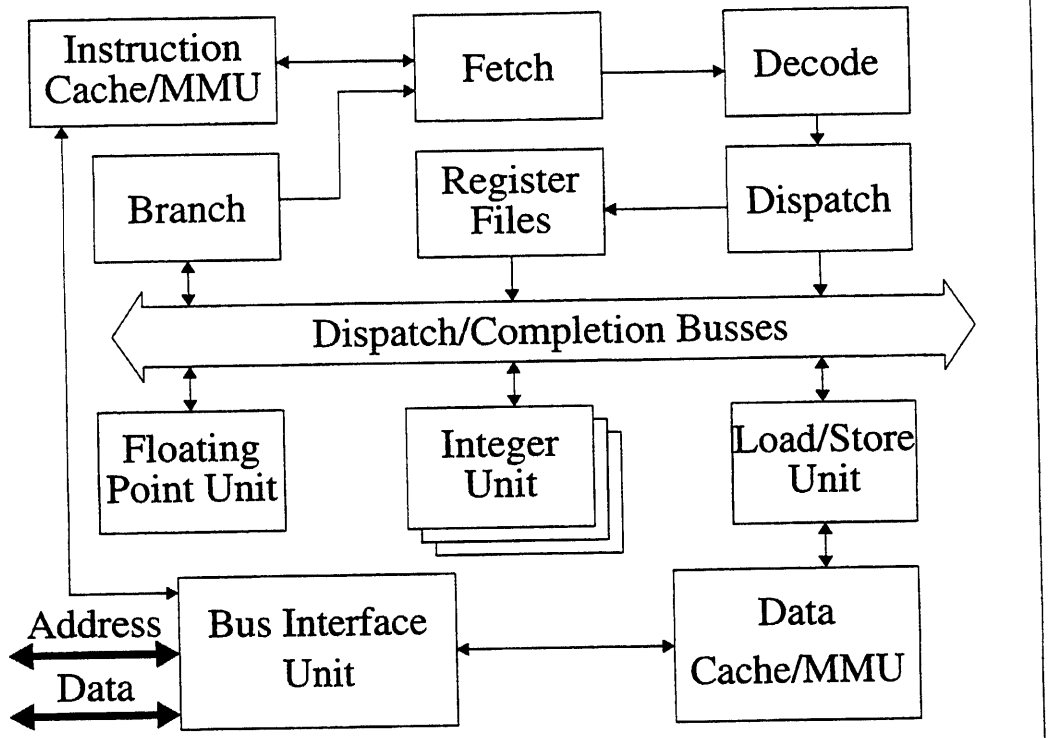
## Performance Strategy

- Dynamic branch prediction
- Speculative execution with rapid correction
- Register renaming to remove false dependencies
- Reservation stations for each execution unit
- Execution serialization for non-renamed resources
- Load and store queues



MOTOROLA INC. IBM

## PowerPC 604 Microprocessor Block Diagram

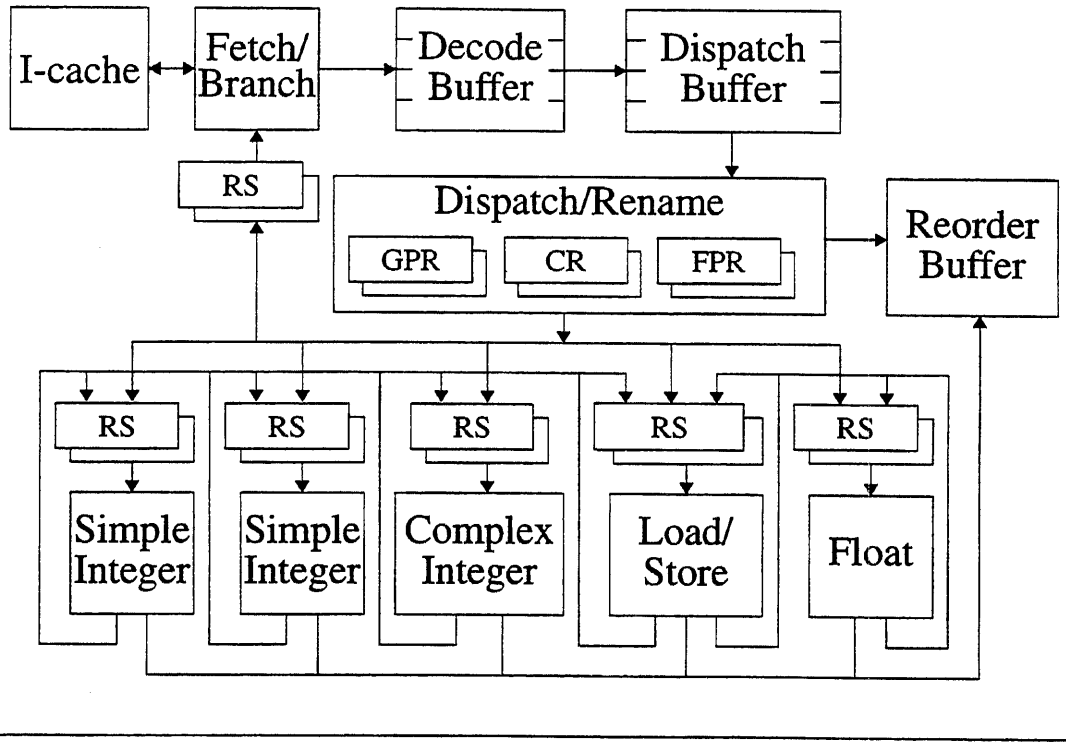





## Superscalar Speculative Execution Highlights

- 6 stage pipeline
  Fetch, decode, dispatch, execute, complete, writeback
- 8-entry instruction buffer (4 decode, 4 dispatch)
- Rename registers: 12 GPR, 8 FPR, 8 CR
- 16-entry reorder buffer
- 6 execution units
- 2-entry reservation stations on each execution unit
- Fast branch misprediction recovery

# 604[1] Execution




MOTOROLA INC. IBM

# Register Renaming Example

**Rename Registers**

| | A | R | DATA | V |
|---|---|---|---|---|
| 0 | 1 | 1 | F1F1F1F1 | 1 |
| 1 | 1 | 2 | 01010101 | 0 |
| 2 | 1 | 2 | 02020202 | 1 |
| 3 | 1 | 1 | 03030303 | 0 |
| | 0 | | ⋮ | 0 |
| 10 | 0 | 3 | 04040404 | 0 |
| 11 | 0 | 6 | 05050505 | 0 |

**Register File**

| | DATA |
|---|---|
| R0 | FFFF0000 |
| R1 | 11111111 |
| R2 | 22222222 |
| R3 | 33333333 |
| | ⋮ |
| R30 | 44444444 |
| R31 | 55555555 |

| Register | Value | Valid | Tag |
|---|---|---|---|
| 0 | FFFF0000 | 1 | X |
| 1 | X | 0 | 3 |
| 2 | 02020202 | 1 | X |
| 3 | 33333333 | 1 | X |



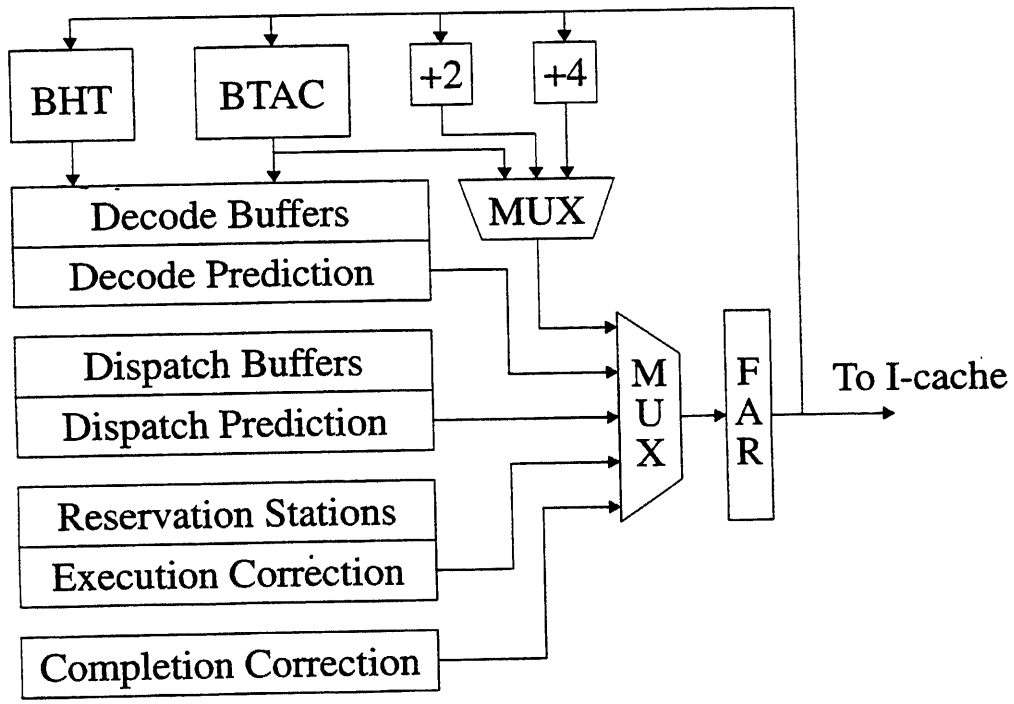
MOTOROLA INC. IBM

# Branch Prediction Highlights

- 64-entry fully associative Branch Target Address Cache (BTAC)
- 512-entry 4-state Branch History Table (BHT)
- Prediction at fetch, decode, and dispatch stages
- Rapid misprediction correction
- Speculative execution past up to 2 branches
- Speculative fetching past up to 6 branches



# Branch Prediction Organization

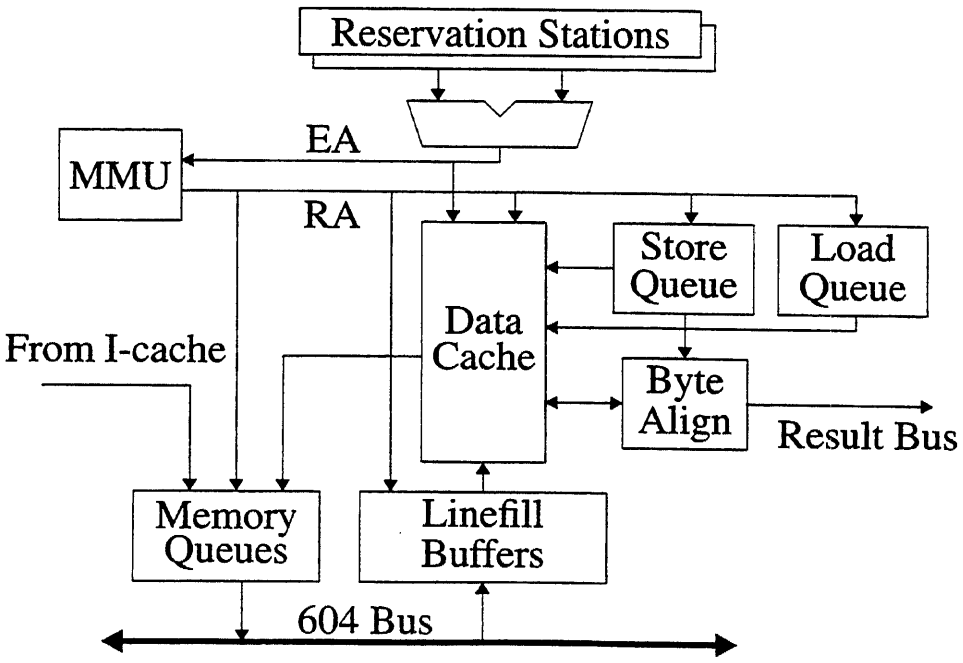


## Memory Pipeline Highlights

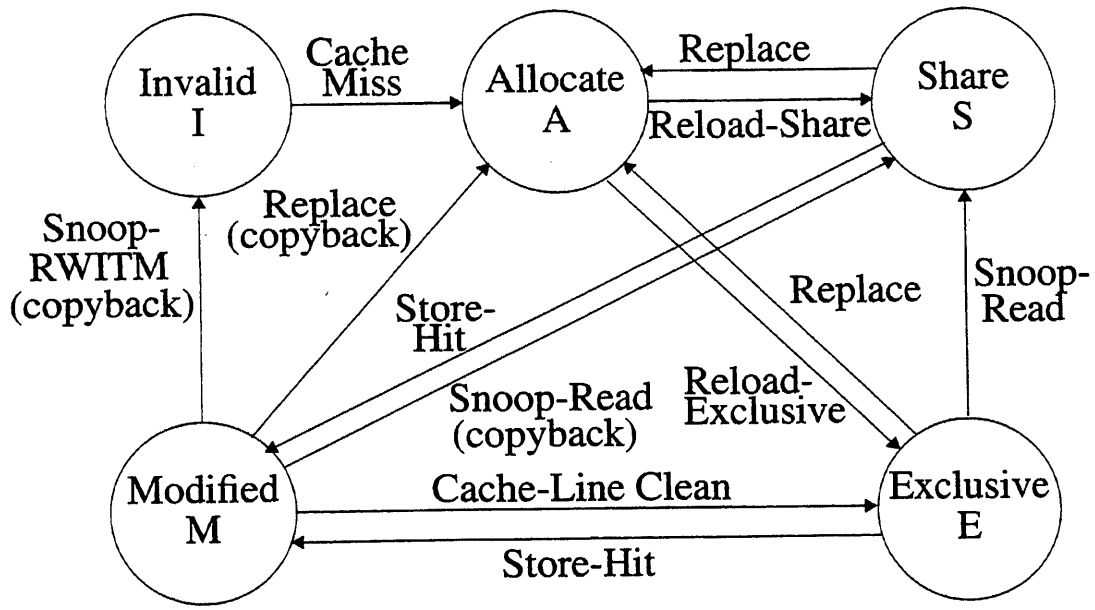
- 16 KB instruction and 16 KB data caches with parity
- Two 128-entry two-way set associative TLBs
- 6-entry store queue, 4-entry load queue
- 2-entry copyback queue with single cycle castout
- 2-entry data linefill buffer
- 1-entry instruction linefill buffer
- 2 cycle load on cache hits
- Loads can bypass stores
- Coherent data cache with dual ported tags for snoop
- Caches non-blocking on misses



## Data Memory Pipeline Organization



# Data Cache State Diagram
# MESIA Protocol






# Software / System Support

- Instruction and data address breakpoints
- Single step trace and branch trace
- Performance monitor
- IEEE 1149.1 JTAG
- Nap mode that continues to snoop

## Summary

- High performance PowerPC Architecture™
- Highly advanced superscalar processor
- Can execute up to 4 instructions per cycle
- Highly speculative execution
- 6 execution units
- Non-blocking pipelines
- Efficient memory operations
- System support



## Trademarks

[1] In this document the terms "PowerPC 604 RISC Microprocessor" and "604" are used to denote the third implementation of the PowerPC architecture.

™ PowerPC, PowerPC Architecture, and PowerPC 604 are trademarks of International Business Machines Corp.