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A PCI Bridge Chip (MPC105) with a Cache and Memory Controller for PowerPC™ Microprocessor

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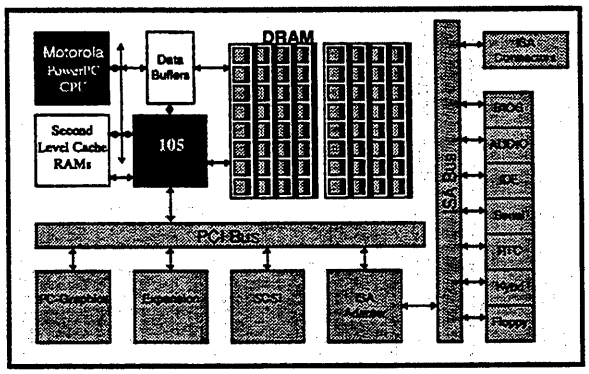
OUTLINE

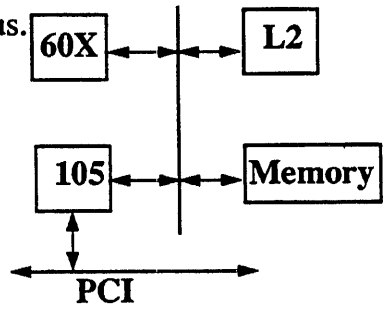
- INTRODUCTION
- DESIGN FEATURES
- ARCHITECTURE
- PERFORMANCE
- PACKAGING
- SUMMARY

PC System Using MPC105 and PowerPC Processor

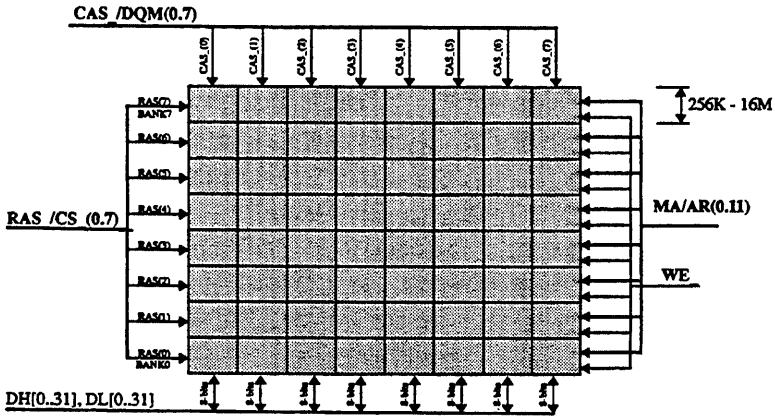


MPC105 Features

- Single chip.
- PowerPC Reference Platform (PReP) compliant.
- PowerPC 601, 603, 604 microprocessors.
- 32-bit address bus, 64 (or 32)-bit data bus.
- Direct mapped L2 cache (write-through, write-back).
- SMP upgrade.
- DRAM or SDRAM (1GByte).
- ROM (16MByte).
- Byte writes to flash EPROM (1MByte).
- Fully PCI compliant.
- Bi-endian support.
- Power management.

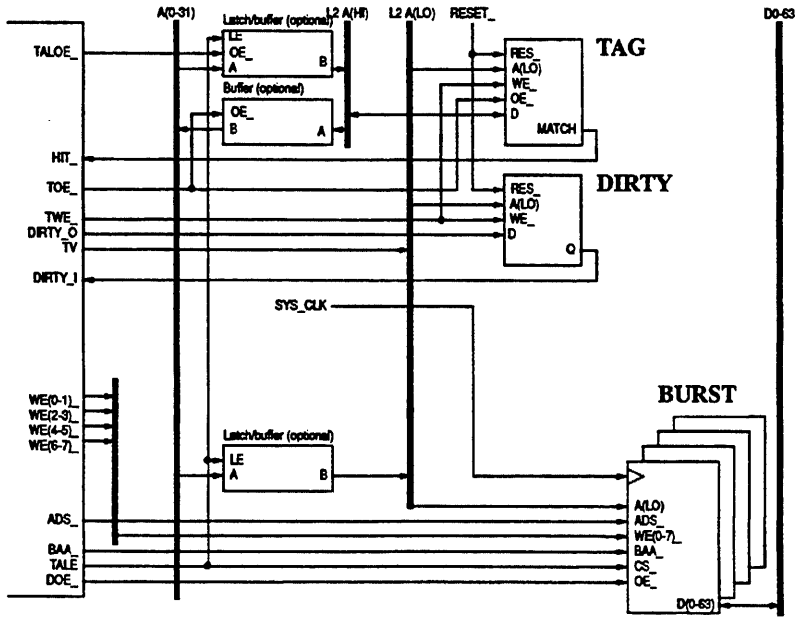


DRAM Memory Organization

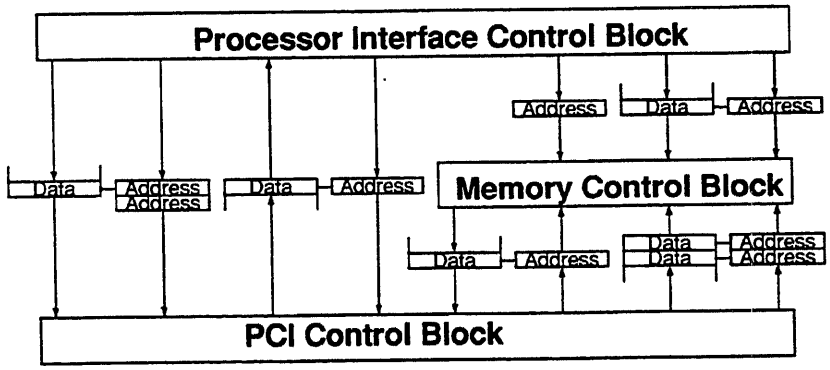


8 Banks support memory with sizes upto 1 GByte

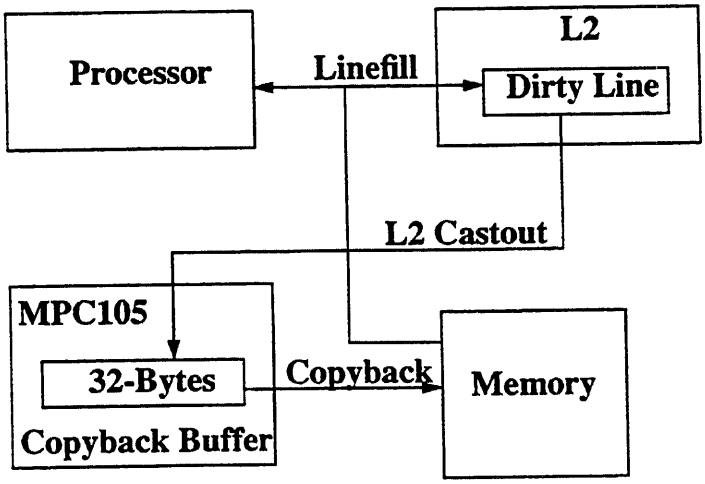
Secondary Cache System Block Diagram



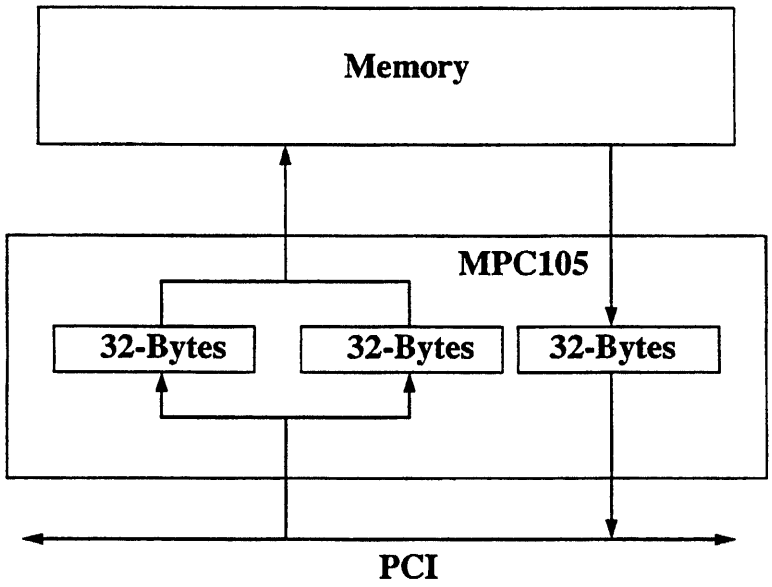
Internal Buffering



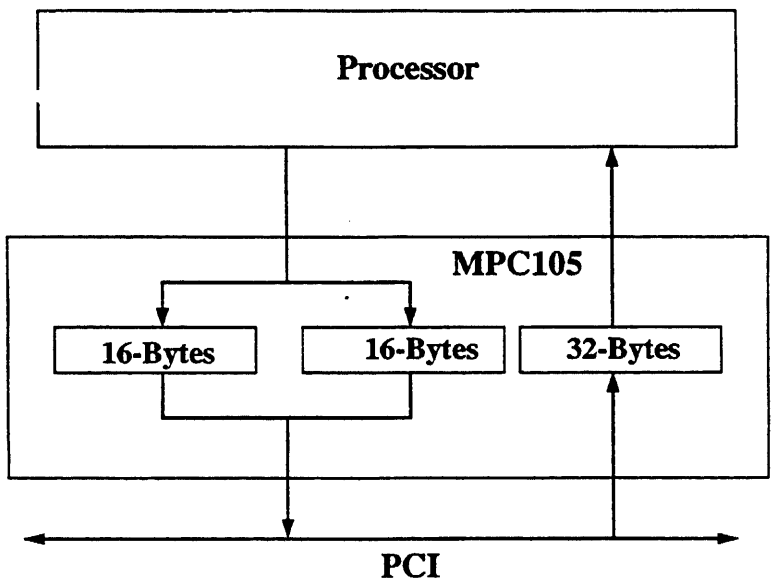
Copyback Buffer



PCI to Memory Read/Write Buffer



Processor to PCI Read/Write Buffer



Performance

Transaction	Number of Cycles
Processor-to-Memory	
Burst read from L2	3-1-1-1
Pipelined burst read from L2	3-1-1-1/1-1-1-1
Burst write to L2	3-1-1-1
Burst read from DRAM	8-3-3-3
Burst write to DRAM	8-3-3-3
PCI-to-Memory	
Pipelined Burst read	9-1-1-1-1-1-1-1/4-1-1-1-1-1-1-1
Pipelined Burst write	2-1-1-1-1-1-1-1/2-1-1-1-1-1-1-1
Processor-to-PCI	
Single read	12
Single write	5

2 to 1 mode

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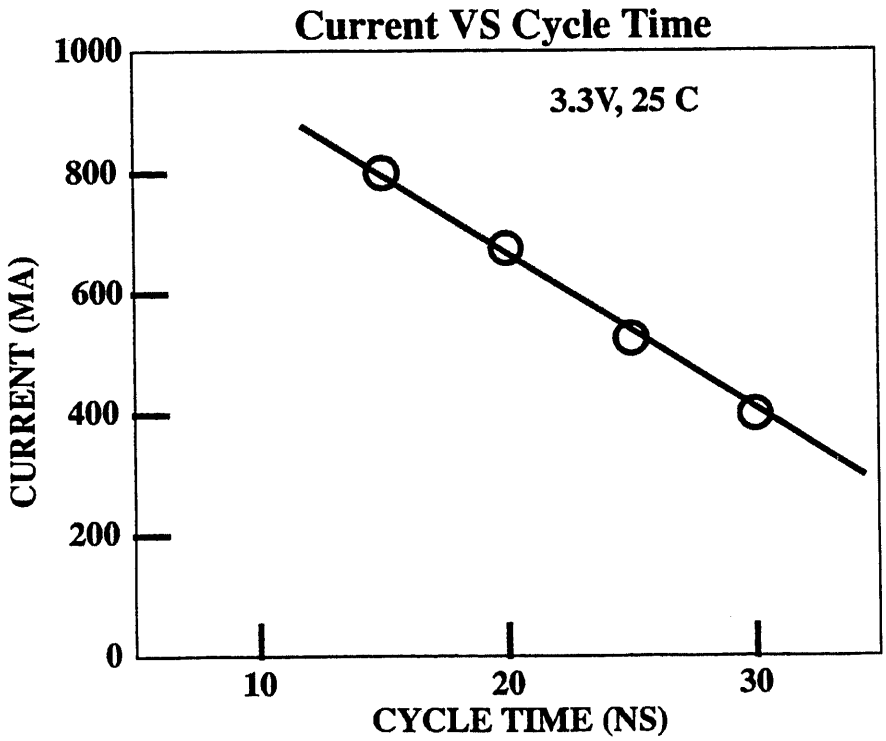
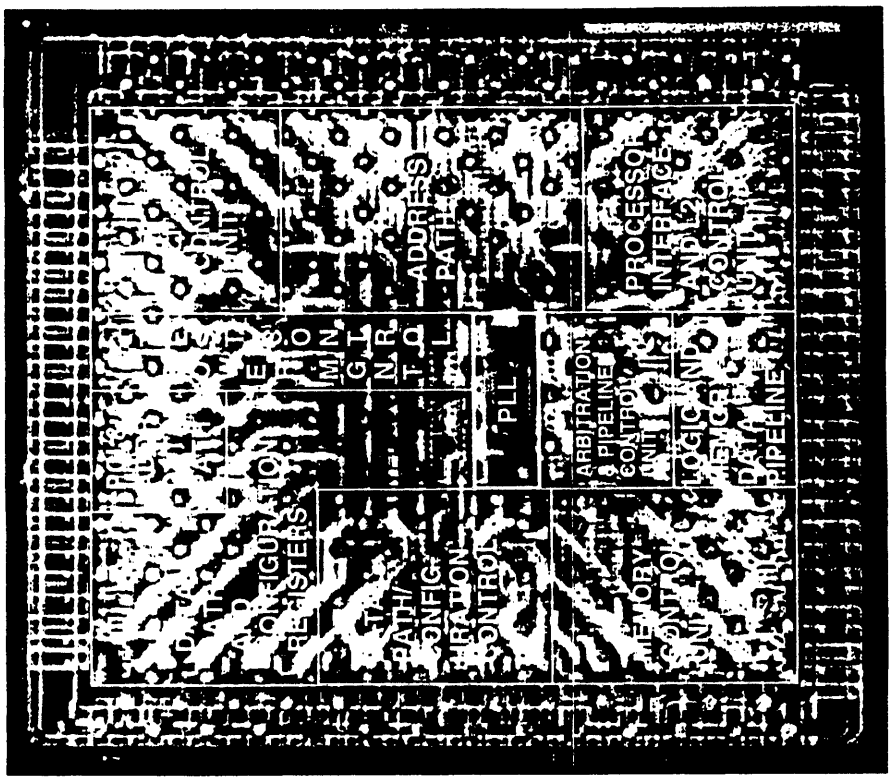


Motorola MPC105



PCI Bridge / Memory Controller for Power PC™

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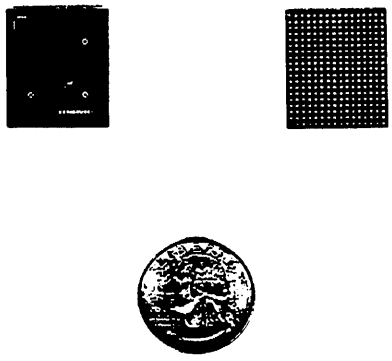
C4/CBGA Package Technology



SUMMARY

- PowerPC Reference Platform (PreP) compliant bridge between PowerPC microprocessor and PCI bus.
- PCI compliant.
- Integrated L2 cache and memory controller.
- Achitecture optimized for performance.
- 0.5um, 4-level metal CMOS technology.
- Die size of 6.2mmx5.7mm ($39mm^2$).
- 247K devices.
- C4/304 pin Ball Grid Array.
- Worst case power dissipation of 2.6 W at 66 MHz.
- Power management.