SH2: A Low Power RISC Micro for Consumer Applications

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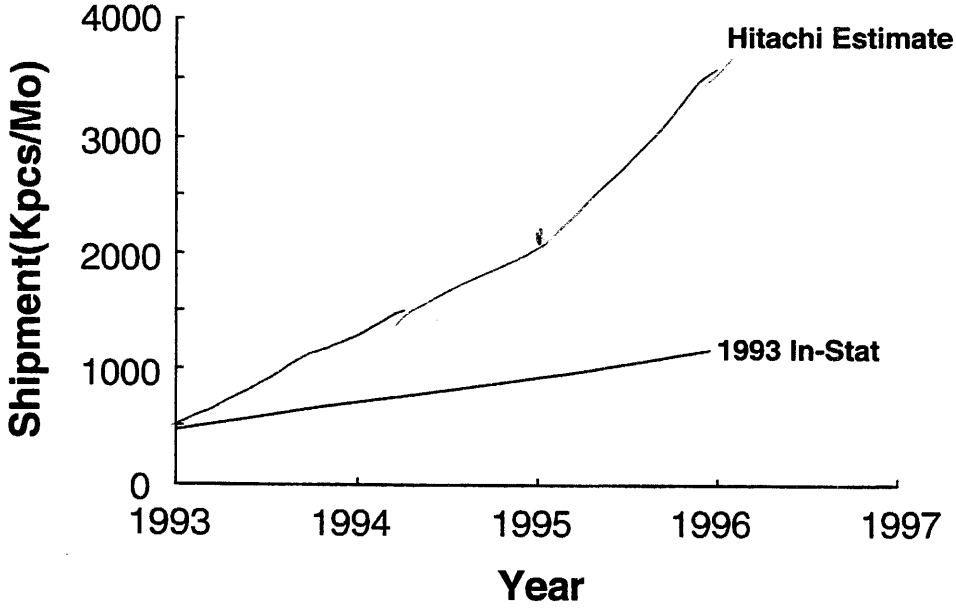
Why are RISCs in Consumer Market ?

- The consumer market is huge
  - Children drive an $8,000,000,000 consumer electronics market
  - Video game revenue now exceeds movie revenue
- Compatibility is not an issue.
  - Currently no consumer electronics standard exists.
- Consumer products are becoming sophisticated.
  - Graphical user interfaces, 3D animation, imaging, complex communications protocols, object-oriented programming
- Price sensitivity is high
  - A $20 price reduction doubles video game sales
  - A $29 or lower price point is comensurate with children's spending capability

World-Wide 32-bit RISC Shipments



SH Family History

Introduced in 1992

Two versions available now

SH1 : embedded controller

SH2 : embedded processor with cache

Two versions under development

SH3 : embedded processor with cache and mmu

SH4 : embedded processor with cache, and multi-media extensions

Over 300 design wins to date

Industry (41%), Consumer (25%), PC/Communications (20%), Automotive (14%).

Volume shipment started

1994: 200K/month, 1995: 1M/month (projected), 1996: 2M/month (projected)

Consumer (60%), PC/Communications (15%), Automotive (14%), Industry (11%)

SH2 Architectural Features

- 16-bit Fixed-Length Instructions
  - Unified data and instruction write through cache for performance with slow memories
  - Small object code footprint minimizes memory requirements and cache traffic
  - 32-bit instruction fetch allows data loads to be scheduled for non-conflicting access to the cache
  - Immediate data pooled in instruction stream
- 16 General Purpose Registers, 6 Special Purpose Registers
- DSP Capability (Multiply Accumulate)
  - supports fixed-point $\Sigma a_i * b_i$
  - 4 cycles for 32b * 32b + 64b -> 64b

SH2 On-chip Functions

- Direct support for popular memory interfaces
  - SDRAM, DRAM, PSRAM, Masked ROM, SRAM
  - 6 cycle cache fill (16-byte line) from SDRAM
- 32-bit Fixed-Point Multiplier for 3D coodinate transformations
- Free-running 64-bit/32-bit Division Unit for 3D perspective transformations
- DMAC, serial interface, timer, interrupt controller, and debugger interface
- Dual-Processor Configuration Support
- Software controlled phase-locked loop (PLL)

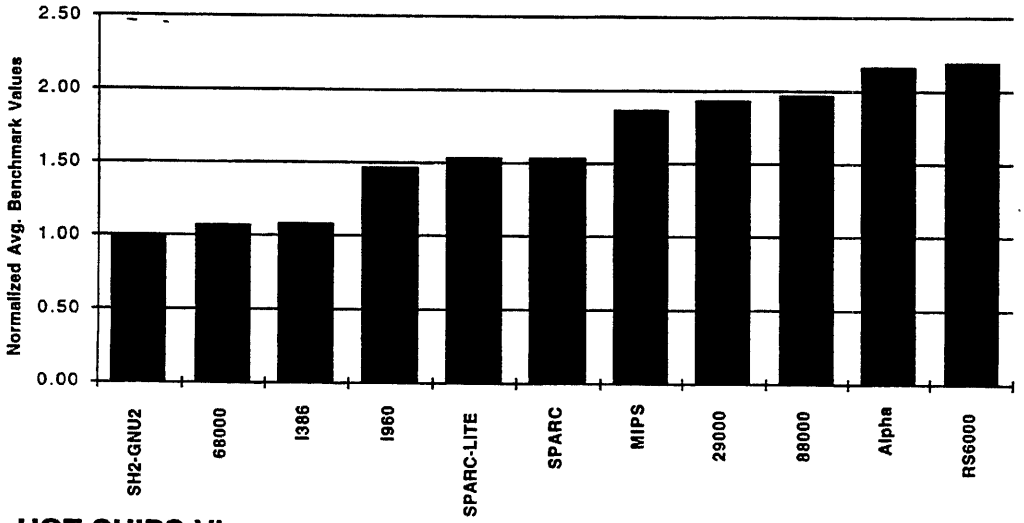
SH1 / SH2 Features

Machine	SH1	SH2
dhrystone 2.1:	16MIPS (28,112)	25MIPS (45,477)
Clock frequency:	20MHz @5V	28.7MHz @5V
Operating voltage:	2.7V ~ 5.5V	2.7V ~ 5.5V
CPU core size:	5.90mm2	5.45mm2
Multiplier size:	1.40mm2	2.66mm2
On-Chip Memories:	64KB ROM, 4KB RAM	4KB, 4-wayUnified$
On-Chip Peripherals:	4DMAC, 2serial, ITU, 8A/D DRAM controller	2DMAC, Serial, DiV SDRAM/DRAM i/f, etc.
Chip size:	8.67mm X8.67mm	7.59mm X7.44mm
Power consumption:	500mW @5V	400mW @ 5V
Process technology:	2-metal 0.8 micron	2-metal 0.8 micron
First silicon:	September, 1992	October,1993
Package:	112 PQFP	144 PQFP

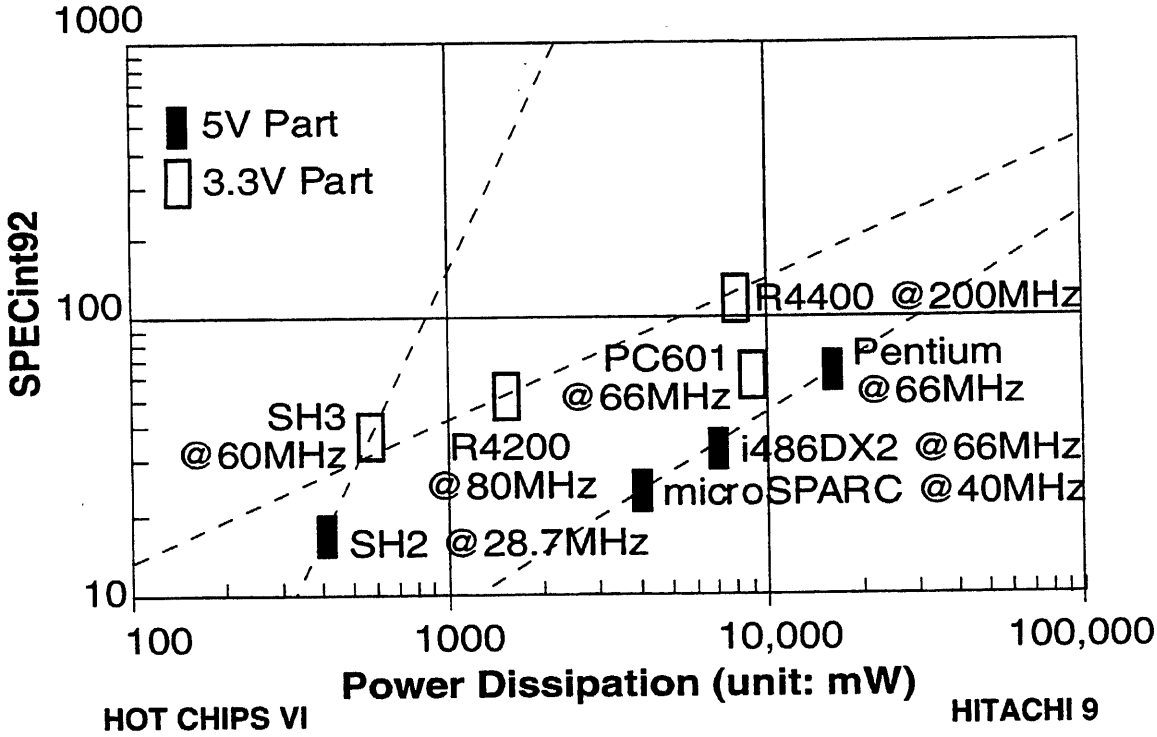
Smaller Object Size

(Further Improvement in Progress)

Data: courtesy of Cygnus Support.
All are measured with GNU CC



SPECint92 vs. Power



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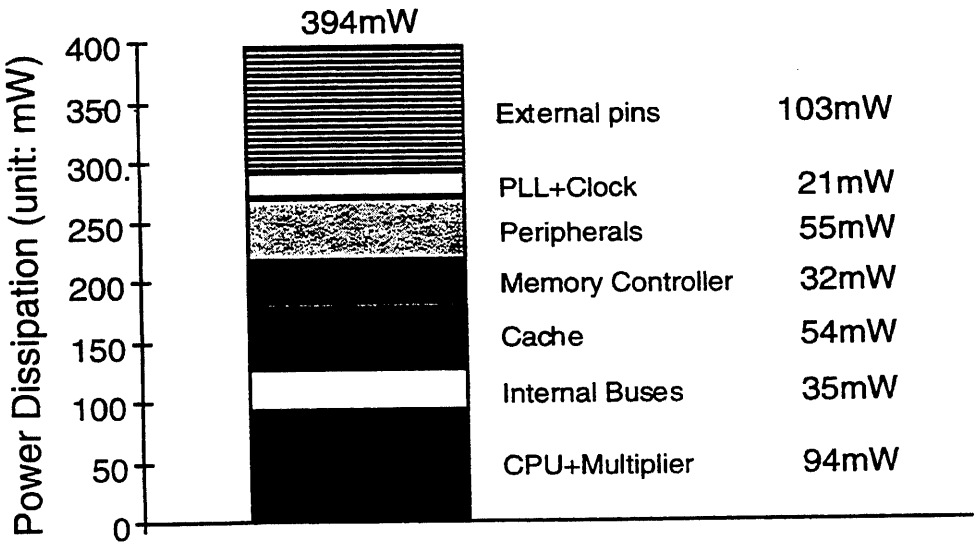
SH2 Power Consumption Breakdown



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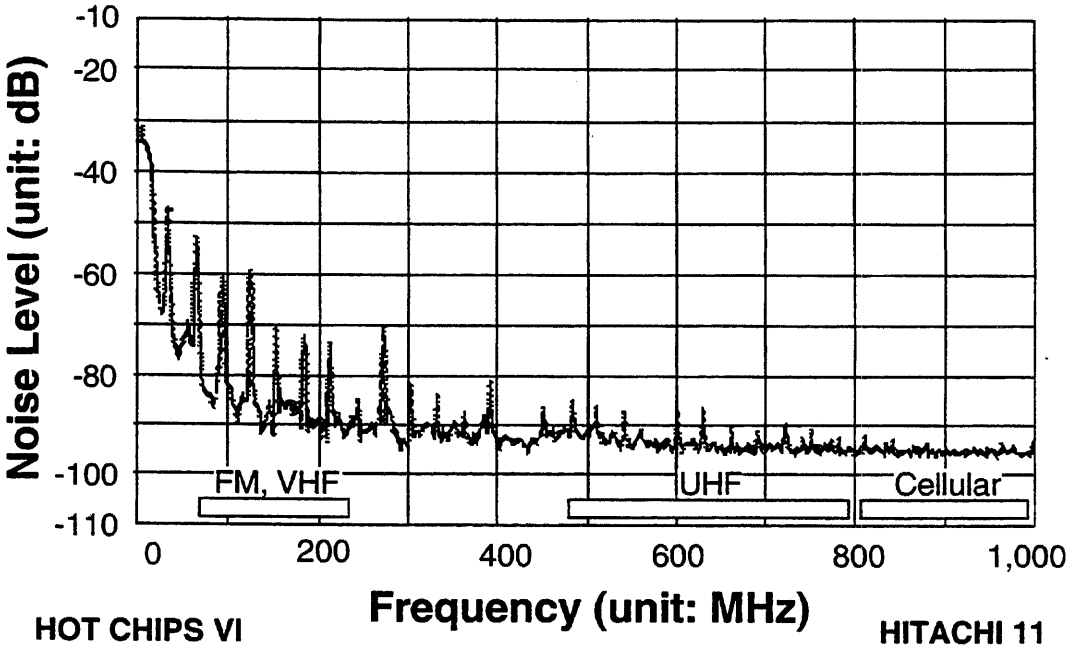
EMI Spectrum on an SH2 Power Line



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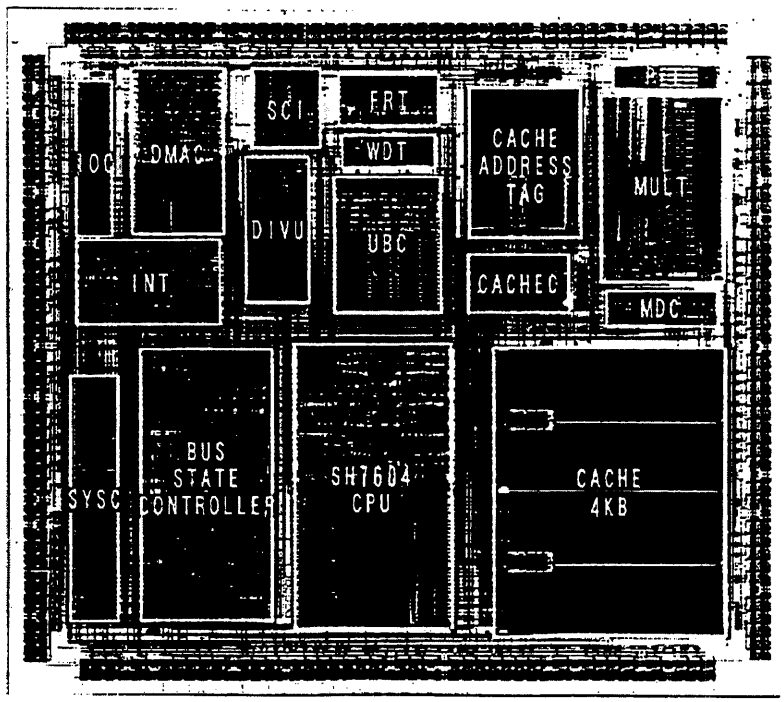
SH2 Die Photo



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SH3 / SH4 Roadmap

Machine	SH3	SH4
dhrystone 2.1:	60 / 100MIPS	300MIPS
Clock frequency:	60 / 100MHz @ 3.3V	200MHz @ 2.5V
Operating voltage:	2.2V ~ 3.6V	1.5V ~ 2.8V
Process technology:	3-metal 0.5 micron	3-metal 0.35 micron
First silicon:	1994	1995

Conclusions

SH2 gives good performance with a small die size and vanilla process.

- 25MIPS processor and peripherals in 56 mm2 @ 0.8 micron
- First processor to include an SDRAM interface
- Example application: video game accelerator box.

SH2 was designed for consumer applications from the start.

- 16-bit instructions contribute to small object code size
- Unified cache and data path help to keep die small
- DSP capability improves voice, image and 3D processing performance
- Low power, Low EMI, and Low Cost Design
- Low power cache
- Small CPU core (5.42mm2 @ 0.8 micron)