The new i960® Processor that offers More for Less, the i960®Jx Series

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Introducing the i960®Jx CPU

- Feature Set
- Special Features
- Power Saving Features
- Performance Results

Feature Set: Summary

- Single cycle execution of RISC ops.
- 3-ported register file with bypass.
- Concurrent Multiply/Divide unit.
- Parallel Loads with integer and MDU pipelines.
- HW-supported complex addressing modes.
- 4-KB I-cache; 8-set Local Register Cache.
- 2-KB D-cache and 1-KB on-chip data RAM.

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Feature Set: Summary (cont)

- 16 to 50+ MHz parts with Clock Doubler Mode.
- 28-41 VAX MIPS.
- 750K Transistors, 64mm^2 die size,
- 0.8-µm process 3-layer metal,
- 3.3V and 5V versions with 132-pin PGA /PQFP.
- Already Taped-Out; Availability in Late '94.

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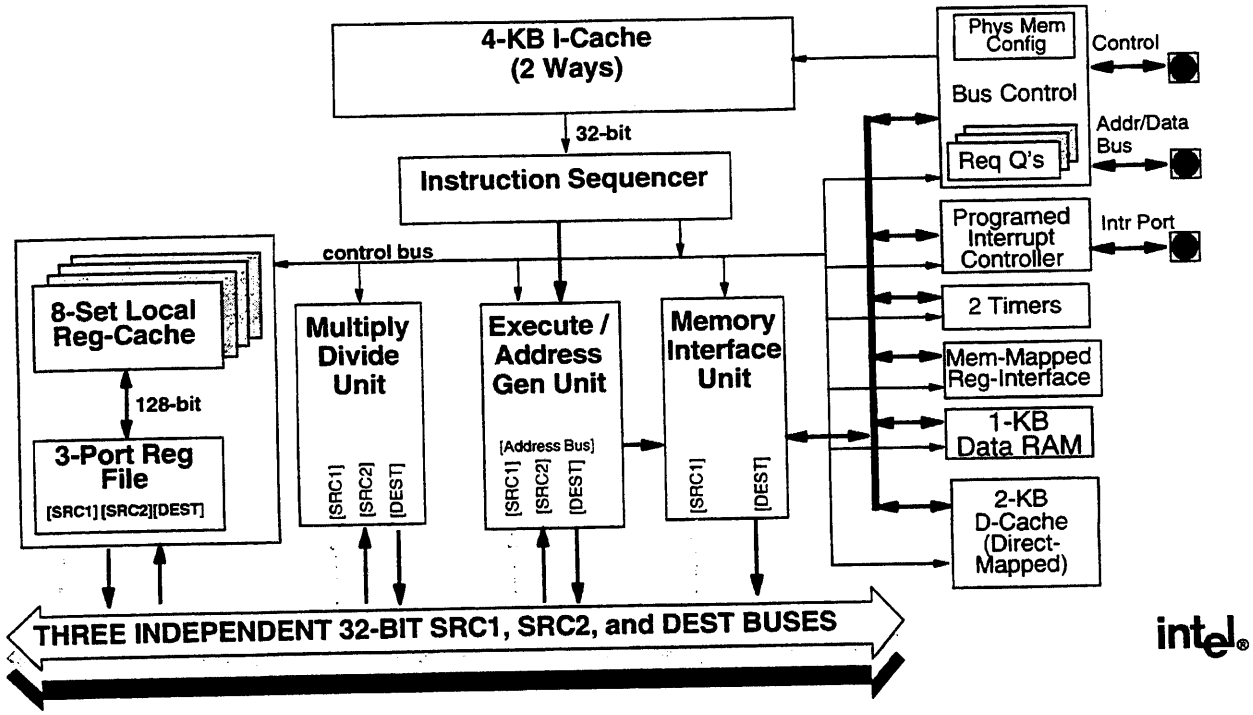
Feature Set: i960® JX CPU Diagram



Special Features: Addressing Modes

Address Computed	Jx Support	HLL Usage
off12	HW:1cyc	Gen 12-bit const
dsp32	HW:2cyc	x = global_addr
(ra)	HW:1cyc	x = *ptr
off12 + (ra)	HW:1cyc	x = local_addr
dsp32+(ra)	HW:2cyc	x = ptr->elt
(ra)+(rx)*sc2	µcode	x = p[i]
dsp32+(ra)+ (rx)*sc2	µcode	x = as[i]->elt
dsp32 + (rx)*sc2	HW:1cyc	
dsp32 + (IP) + 8	µcode	PIC code

Special Features: Fast Call / Return

- 16 Global Regs and "N" sets of 16 local Regs.
- Save & restore local Regs to Register cache.
- Wide paths to Register cache allows 6 cycle ops.
- When cache is full, Oldest sets "spilled" to memory.
- Sets reserved for high-priority interrupts to avoid spills.

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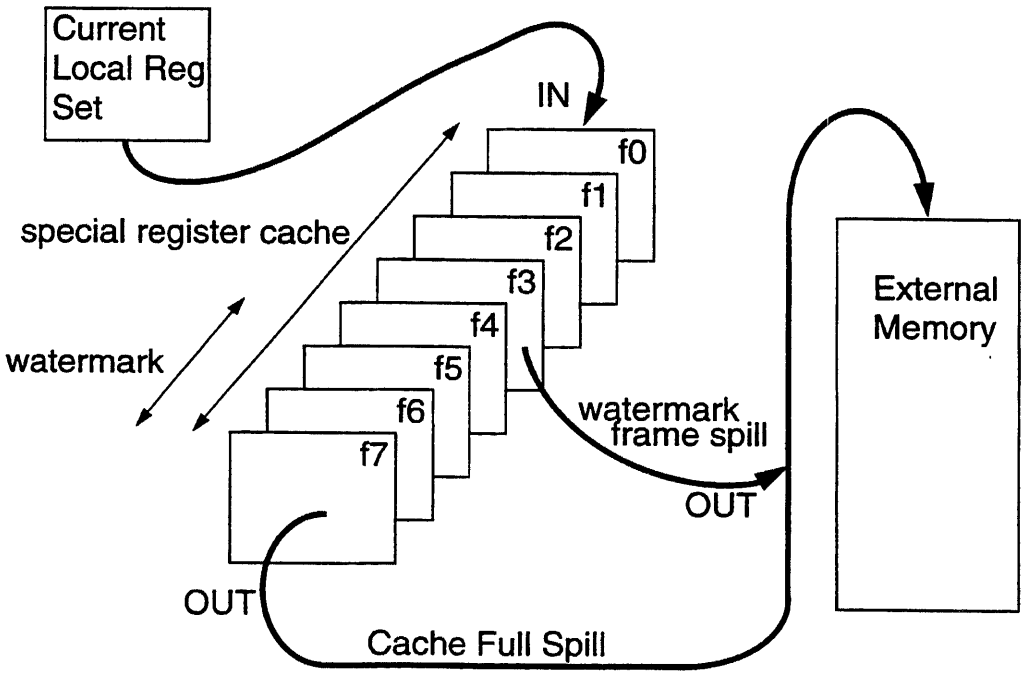
Special Features: Fast Call / Return



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Special Features: New i960 Ops

- Conditional ops avoid branches for short flows:

```
c   fragment: x = (a == b) ? y+y1 : z-z1;

ASM fragment: cmpo    a,b
              addoe   y,y1,x
              subone  z1,z,x
```

- Subword compares avoid masking.
- Byte-Swap instruction.

Special Features: Memory Accesses

- 1-KB on-chip RAM for key data & interrupt vectors.
- Profiling compiler can move variables to this RAM.
- Built-in unaligned memory reference support.
- Supports Big & Little endian memory accesses.
- Multi-word LD/ST ops: bus bursting & code density.

Power: Fully static, low-power design

- Typical Power usage: 0.5 watt - 3.3v @ 33MHz.
- Enhanced-Scalar is less power than super-scalar.
- Predict memory ops, then power-up D-cache.
- Don't drive µROM when not executing µcode.
- Stop clocks of an idle unit instead of ignoring result
- Multiplex Addr/Data bus: lower pin count & power.
- New HALT instruction can reduce power by 90%.
- Exit HALT by external interrupt or on-chip timers

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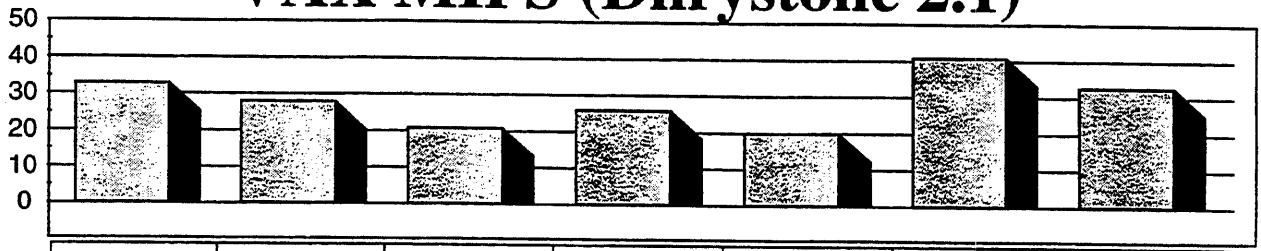
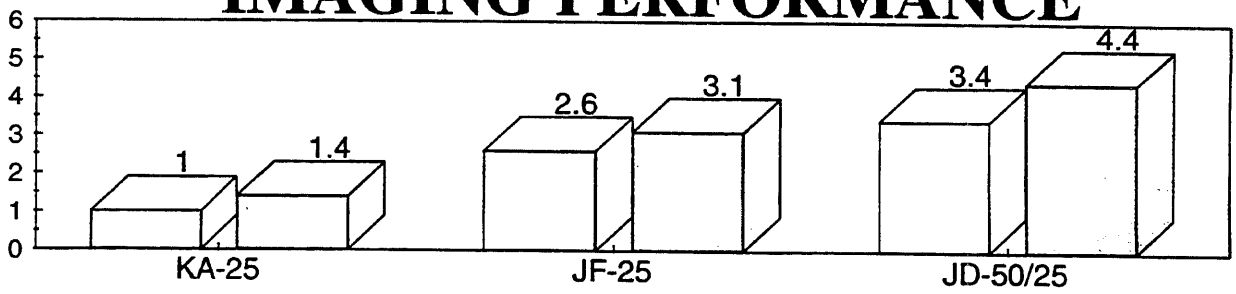
VAX MIPS (Dhrystone 2.1)



JF 40Mhz	JF 33Mhz	JF 25Mhz	JA 33Mhz	JA 25Mhz	JD 50/25Mhz	JD 40/20
33	28	21	26	20	41	33

IMAGING PERFORMANCE



Based on simulation of Postscript page "Golfer"

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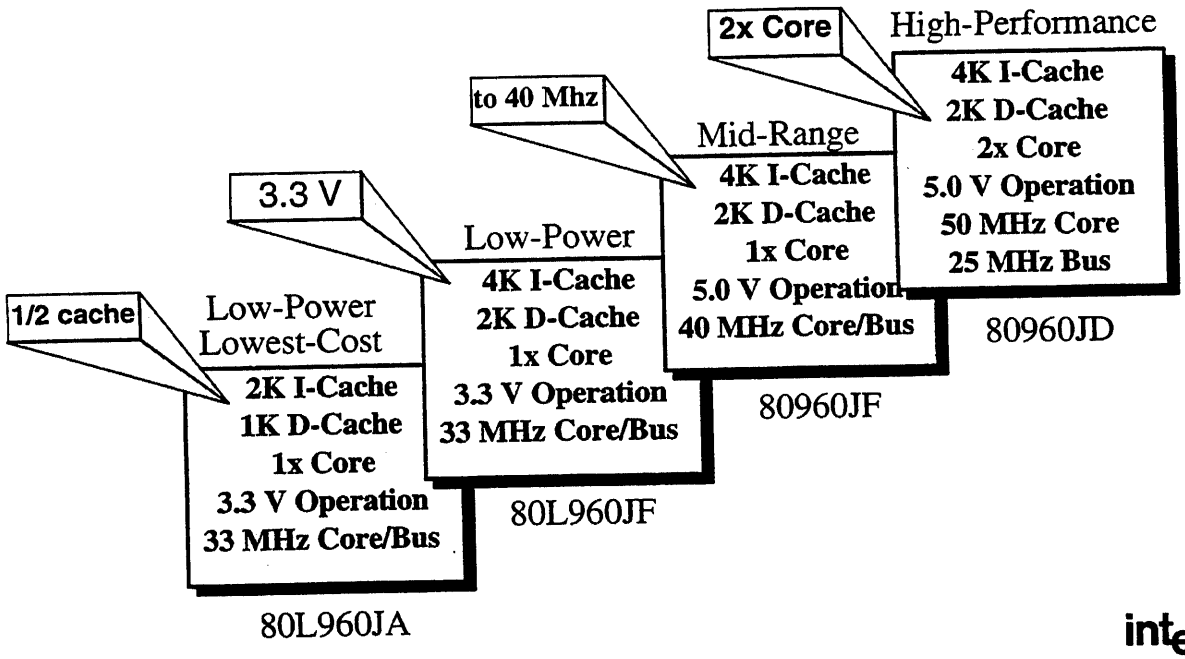
Processor Summary



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Backup: FeatureTable

	80L960JA	80960JF	80L960JF	80960JD
I-Cache (2-way)	2K	4K	4K	4K
D-Cache / DataRam	1K / 1K	2K / 1K	2K / 1K	2K / 1K
Cached local reg sets	8 sets	8 sets	8 sets	8 sets
VAX MIPS	28 (33MHz)	33 (40MHz)	28 (33MHz)	41 (50MHz)
Clock (MHz)	16, 25, 33	16,25,33,40	16,25,33	33,40,50
Clock Doubler mode	no	no	no	yes
Supply Voltage	3.3v	5v	3.3v	5v
Typical Power	0.5W (33MHz)	1.2W (33MHz)	0.5W (33MHz)	1.9W (50MHz)
Availability	3/95	12/94	3/95	6/95

750K Transistors, 64mm^2 die size, 0.8-µm process
3-layer metal, 132-pin PGA /PQFP