A 500 MHz BiCMOS Gigabyte/Second SCI-Link Implementation

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Agenda

- Problem definition and background
- SCI-Link architecture overview
- SCI-Link chip description
- Chip status and applications
- Further work

Introduction

- Problems:
  - Higher bandwidth at low latency needed
  - Higher I/O bandwidth to more I/O devices needed
  - Multi-drop busses are approaching physical limits

- Solution Approach:
  - Use point-to-point asynchronous interconnect
  - Build packets to produce logical multi-drop busses where needed

Introduction

Background:

In 1990, the AS/400 Division established a team to evaluate and develop a high-speed interconnect

Chose IEEE P1596 SCI (Scalable Coherent Interface) as a starting point for evaluation

Reasons for selection:

- Supported high-bandwidth low-latency link

  500 Mbit/sec/bit with 16-bit data, 1flag bit, 1 clock bit

- Scalable to moderate distance (8 meters)
- Standard
- Relatively complete

Introduction

Background:

Criteria for further evaluation :

- Suitability for 500 MHz implementation in CMOS
- Fault-tolerance of link protocol
- Applicability of high-level protocols for :

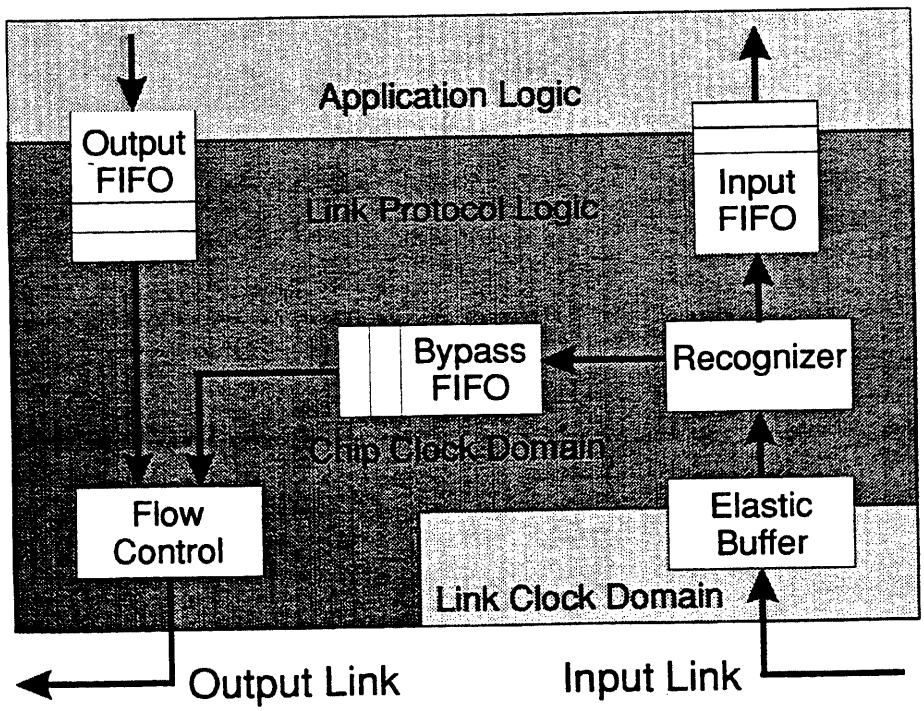
  Coherent shared memory

  Message passing

  I/O subsystem

In 1993, 500 MHz portion of the link protocol was design in BiCMOS

SCI-Link Architecture



SCI-Link Architecture

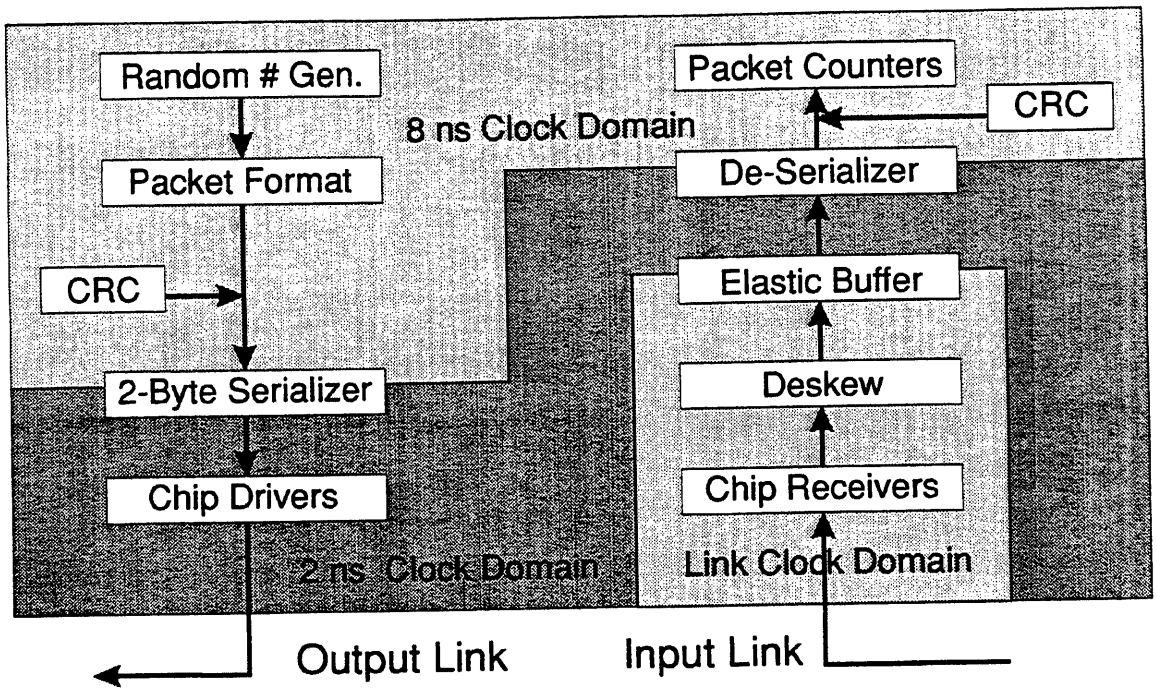
Modification to SCI link protocol for data integrity:

- 32-bit CRC
  - Meet commercial system data integrity requirements
  - More suitable for use in fiber technologies
- Hardware detection/retry of lost/corrupted packets
  - Avoid software invocation on detected link errors
- Duplicate packet suppression
  - Avoid data integrity failure
- End-to-end packet acknowledgment
  - Tolerate failures in redundant topologies

SCI-Link Chip Description

- Chip objective: demonstrate design feasibility of 500 MHz
- Essential portion of SCI-Link architecture implemented
- Necessary 500 MHz function included:
  - Driver/Receiver logic
  - Bit-to-bit deskew logic
  - Elastic buffer
  - Packet aligner
- Ancillary function included:
  - Random packet-data generator
  - Packet framing logic
  - 32-bit CRC
  - Statistics counters
  - Analyzer ports

SCI-Link Chip Description



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SCI-Link Testbed Description

- Chip:

Technology	0.8 micron BiCMOS
Die Size	12.7 mm x 12.7 mm
Voltage	3.6 Volts
Package	32 mm Ceramic SBC (BGA)
Chip Area	15%
Watts (500 MHz logic)	3 Watts

- Card: Standard AS/400 9x11" card, 6 signal, 4 power planes
- Cable: 5 meter cable, 50-pin connector (AMP)

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SCI-Link Chip Status

- Tape-out 6/93 / Power-on 1/94 / Debug complete 3/94
- Correct operation as slow as 125 MHz
- 500 MHz box-to-box (separate power and oscillators)
  - Error-free transmission of 8- to 512-byte packets on 5-meter cable
  - Functional bit-to-bit deskew
  - Functional elastic buffer
  - Passed Class A FCC EMC product-level testing

SCI-Link Media Evaluation

- Testbed for 500 MHz logic, card, copper cable/connector evaluation
- Testbed for emerging parallel fiber technologies
- OETC (ARPA-funded consortium): laser parallel fiber transceivers
  - 500 Mbit/sec/signal
  - Up to 100 meters
- JITNEY (NIST-funded consortium): LED parallel fiber transceivers
  - 500 Mbit/sec/signal
  - Up to 30 meters
- SCI-Link chip is basis for a testbed
  - Sophisticated packet generator
  - Bit error rate checker

Further Work

- CMOS designs underway
- Lower-cost, lower-speed designs underway
- Architectural evaluation and definition continues
  - System coupling - alleviating the multi-drop bus bottleneck
  - I/O coupling - scaling I/O subsystem connectivity and performance
- Evaluating emerging parallel fiber technologies

Conclusions

- SCI link protocol as starting point; modifications where needed
- Demonstrated 500 MHz link operation achievable in silicon
- Constructed testbed for evaluation of:
  - High-speed logic
  - Card designs
  - Connectors and cables
- Continued use of testbed for parallel fiber study
- Modifications continue to evolve
- Important enabling technology for future products