

# **UAI2110: A Universal GaAs ATM Interface Chip for High Speed Networks**

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## **Overview**

- Motivation and background**
- UAI2110 system features**
- UAI2110 architecture, transmitter, receiver**
- GaAs implementation, chip statistics**
- Target applications**

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## Motivation and background

- Universal interface chip which can support several line codes and word widths
- STM and ATM support
- Low complexity, low power consumption, low cost
- Chip should be used in PC environment (plug-in card) or another modular system
- Flexible configuration for different operating modes
- Built-in loop-back capability for diagnostic purposes
- Simple interface to external control unit

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## Features:

- Universal high speed serial interface for serial to parallel and parallel to serial conversion (SPPS)
- Physical line interface for SONET, SDH - STM1 (A) and STM4 (B), PDH -140Mbps (A) and -565Mbps(B), 100Mbps ATM UNI, FDDI, Ethernet 100Mbps and many proprietary transmission standards.
- Supports line codes like NRZ, NRZI, CMI, MCMI, Manchester, 4B5B, 8B10B, 16B20B, and other proprietary codes
- Configurable word width; 8bit, 10bit, 12bit, 16bit, 20bit
- Two versions:  $f_{max} = 320\text{MHz}$  (A) and  $f_{max} = 640\text{MHz}$  (B)

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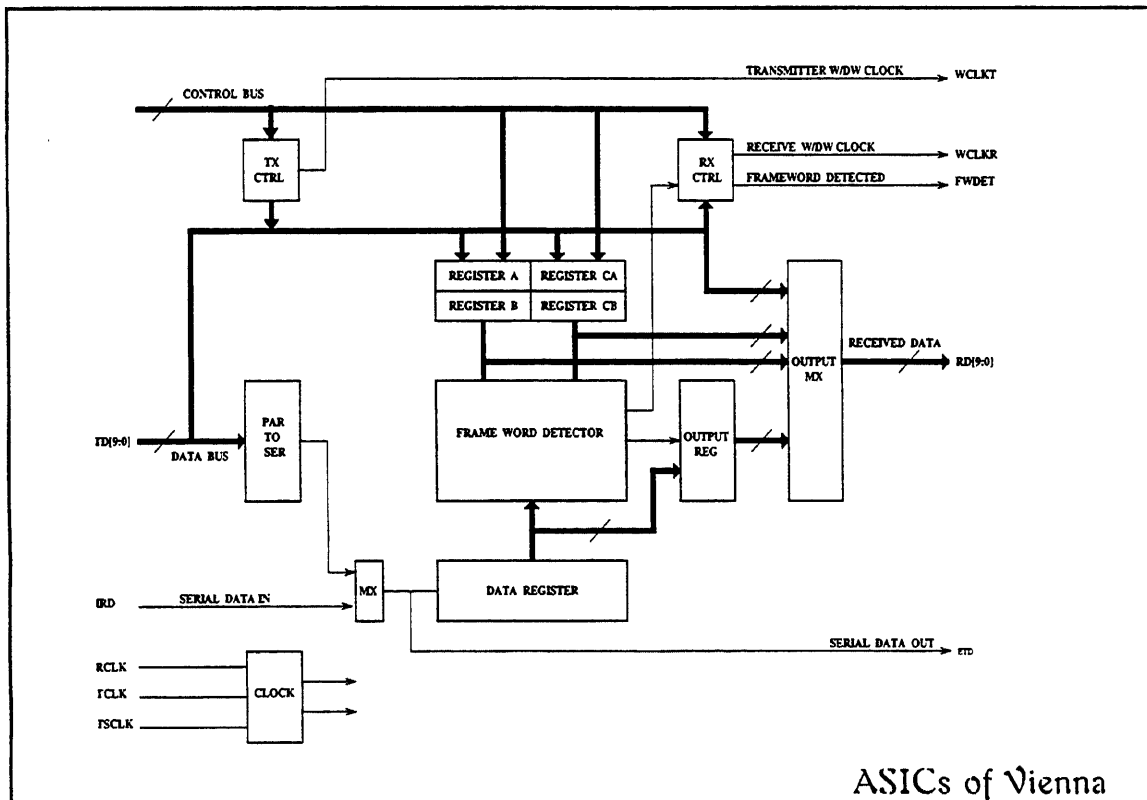
## Features (continued)

- TTL and differential positive ECL (PECL) compatible signal IOs
- Supports word and frame synchronization
- External clock recovery and synthesis
- Supports optical driver and receiver modules for fiber optic cable interfaces
- Supports category 5 UTP or STP cables
- 3 loop-back capabilities for internal and external tests
- Fully software configurable
- Low power consumption

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## Transmitter

- 10-bit input data bus
- Transmitter system clock generation for external data unit allows to control conversion to appropriate PDH or STM frame.
- Transmitter word and double word clock generation synchronizes proper data load into internal shifter.
- Clock period depends on a transmitted word width (8b,10b,16b,20b) and is configurable through data bus
- synchronization between system clock and word clock is controlled through a dedicated pin
- Appropriate coding of transmitted words is provided by external controller
- 10-bit output data bus can be used to observe transmitted words in a loop-back mode

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## Receiver

- 20-bit internal data bus
- Receiver system clock generation for external data unit allows to control proper conversion from PDH or STM frame.
- Receiver word and double word clock generation synchronizes proper data load into internal 10bit output register. Clock period depends on a received word width (8b,10b,16b,20b) and is configurable through data bus
- synchronization between system clock and word clock is controlled through a dedicated pin
- Word and double word clock is synchronized by the frame word detected signal
- Frame word synchronization can be disabled

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## Receiver (continued)

- Full speed frame word decoding and comparison is made in two operating modes
- Two internal 20bit registers are used for frame word comparison purposes
- Direct and inverted modes are available
- Two internal 20bit mask registers
- Direct frame word comparison mode (e.g. NRZ, NRZI, 4B5B line codes)
- Line code comparison mode (e.g. CMI, MCMI, Manchester),
- All modes can be changed "on the fly"
- Appropriate decoding of received words is provided by external controller
- Received serial data stream can go through the chip in signal loop mode

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## Clock

- Transmitter and receiver clocks are independent in the operating mode
- Test clock, receiver clock or transmitter clock can be used as a common clock for both transmitter and receiver during several operating and test modes
- Minimum skew on clock for different clocking modes

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## GaAs implementation

- Low power consumption and positive power supply was required
- .8u HGaAsII process and vcb50k standard cell library was available at Thomson CSF
- Library was ported to COMPASS v8r3.8 design tools
- VITESSE Design Kit was used for the timing calculation design rule checking and back annotated netlist generation
- Full custom TTL I/O cells were designed to allow positive power supply operation and to reduce power consumption
- Standard VSC3K pad ring was used
- THOMSON CSF MPW run for prototyping

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## Chip statistics

- .8u Thomson CSF HGaAsII DCFL Standard Cell with Full Custom TTL I/Os
- Clock rate 520MHz (A) 640MHz (B)
- Power supply 0, +3V, +5V
- Power consumption 1.5 - 1.7W
- LDCC132 package
- 5.54 x 3.44 (Standard VSC3K pad ring)
- 4.06 x 3.44 (Custom pad ring)
- COMPASS v8r3.8 Design System
- Design time: 12-man-weeks
- Tape out: June 93
- First prototypes: February 94 (MPW run was delayed)
- Device status: Full speed functionality under testing

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# Chip Layout

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## Target applications

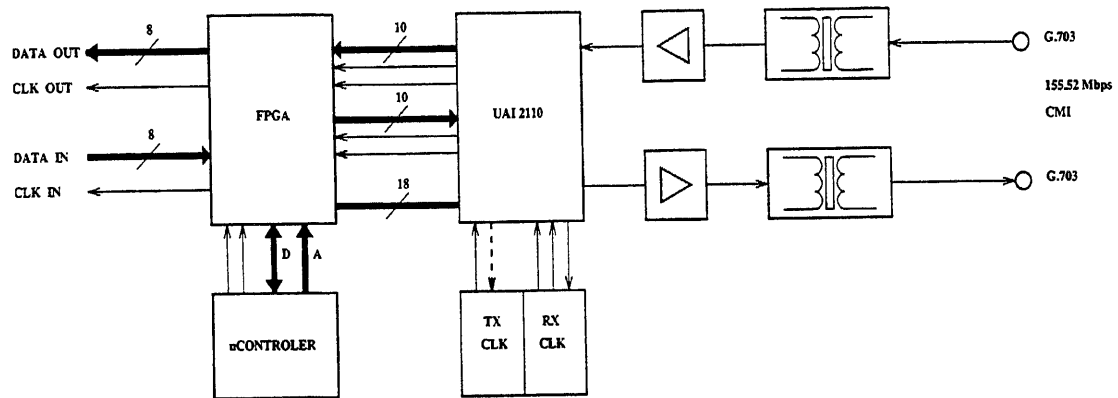
- **Universal network analysis instrument**
  - SDH - STM1 - 155.52 Mbit/s (CMI, G.703)**
  - STM4 - 622.08 Mbit/s (B)(NRZ,8B10B)**
  - (Synchronous Digital Hierarchy - Synchronous Transfer Mode - Coded Mark Inversion)**
  - PDH -140Mbps (A) and -565Mbps(B) (Plesiochronous Digital Hierarchy)**
  - ATM applications based on SDH - STM1 (Asynchronous Transfer Mode)**
  - FDDI (NRZI,4B5B) (Fiber Distributed Data Interface )**
  - Ethernet 100Mbps (Manchester II)**
  - Token Ring (Differential Manchester)**
- **Fast Ethernet terminal (100Base-2,100Base-VG,200Mbps, 300Mbps)**
- **Multimedia terminal**

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## ATM application based on SDH STM1



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