A 500-MHz, 32-b, 0.4-μm CMOS RISC Processor (GALLOP)

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Kazumasa SUZUKI, and Masakazu YAMASHINA

System ULSI Res. Lab. Microelectronics Res. Labs.

NEC Corporation

1120 Shimokuzawa, Sagamihara, Kanagawa 229, JAPAN
TEL +81-427-71-0746 FAX +81-427-71-0881
e-mail suzu@mel.cl.nec.co.jp masa@mel.cl.nec.co.jp

OUTLINE

1. Challenge
2. Chip photo and main features
3. Architecture for high speed processor
4. Key circuit techniques and experimental results
5. Summary

CHALLENGE

Making a high speed processor

- Fabrication technology 0.4 μm CMOS
- Design of high speed function blocks
- High speed oriented architecture
- Integration techniques for high speed function blocks

MAIN FEATURES & CHIP MICROPHOTOGRAPH

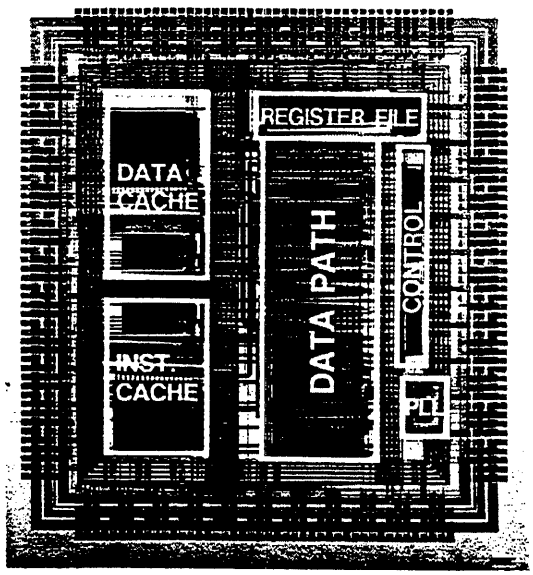
Fabrication technology
0.4- μm CMOS 3-level Al

Chip size
7.90 mm × 8.84 mm

Number of transistors
201,478

Power supply
3.3 V

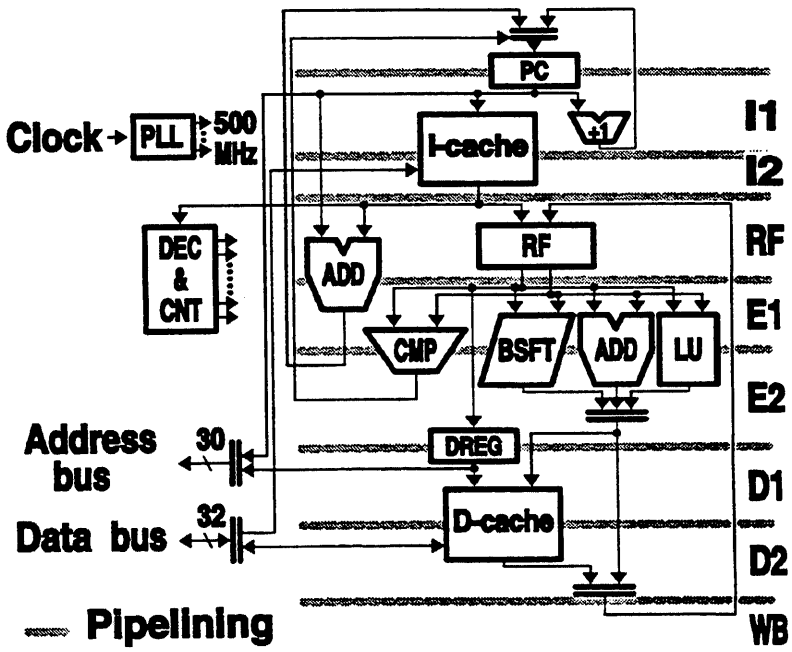
Power dissipation
6 W at 500 MHz



ARCHITECTURE FOR HIGH SPEED PROCESSOR

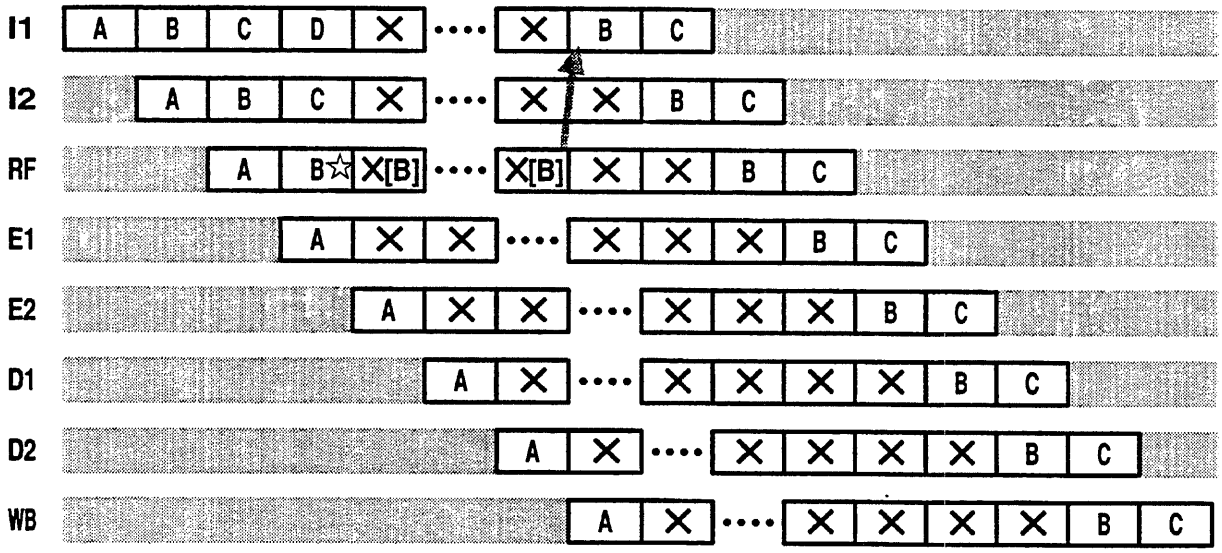
- 8-stage pipelined datapath
- Simple datapath control
  - No pipeline hold
  - No register forwarding
- Testing

ARCHITECTURE



SIMPLE CONTROL - NO PIPELINE HOLD

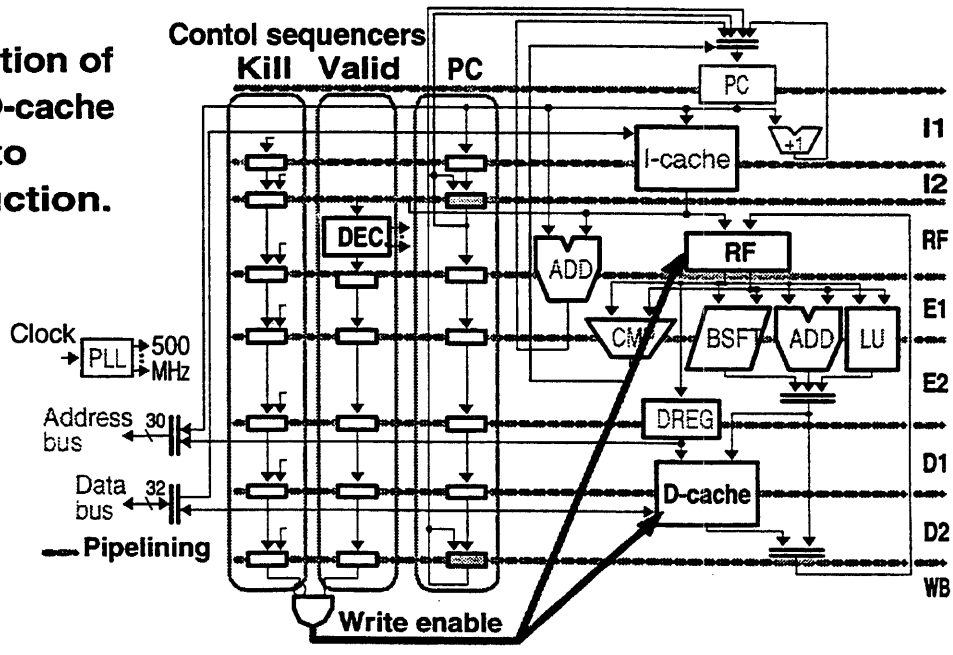
☆ Instruction cache misses on operation "B"



X kill

SIMPLE CONTROL - SEQUENCER

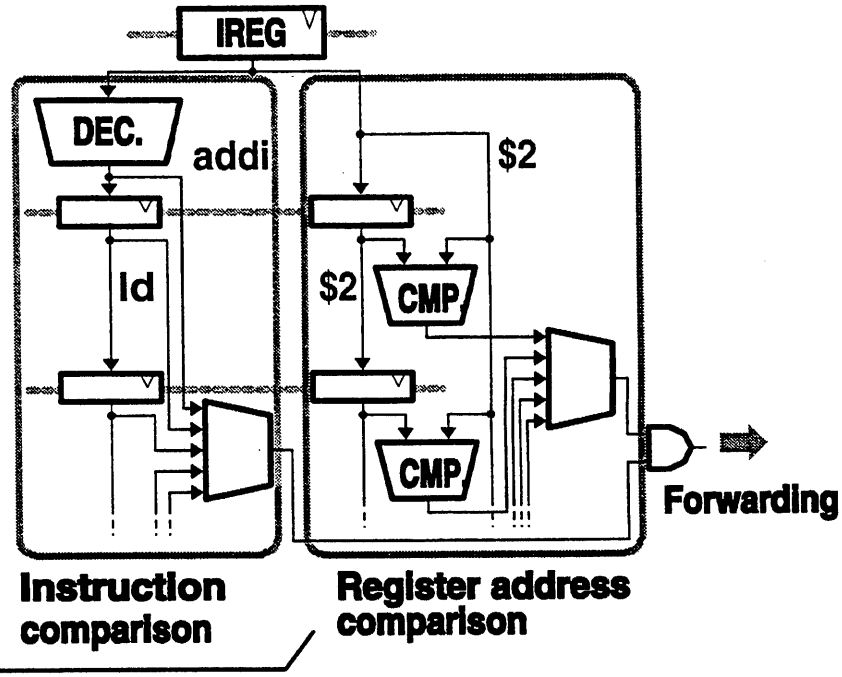
Only cancellation of writing RF & D-cache is essential to killing instruction.



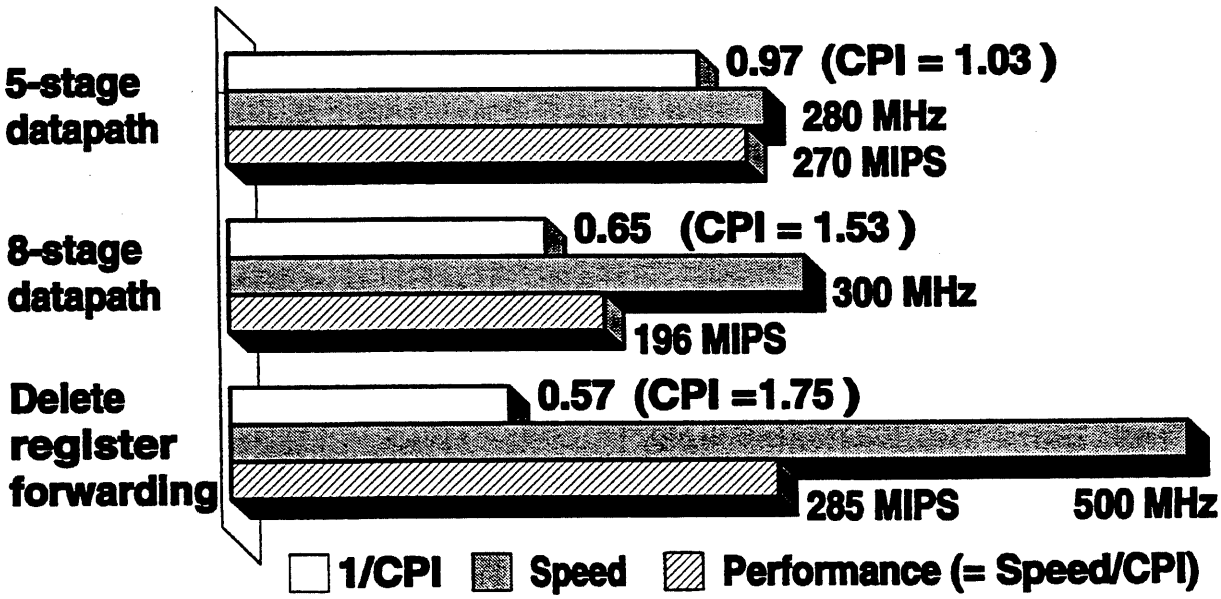
NO REGISTER FORWARDING

DATA HAZARD

```
ld    $2,0[$3]
addi  $2,$2, 1
```



PENALTY FOR HIGH SPEED



* CPI data is estimated from J.L.Hennessy & D.A.Patterson "Computer Architecture A Quantitative Approach", Appendix C

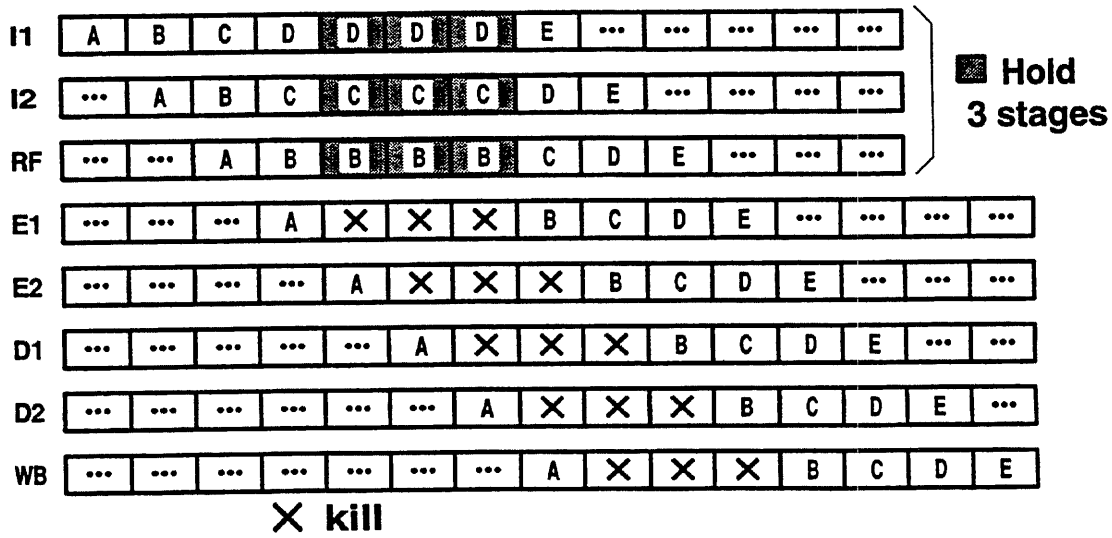
HINT FOR NEXT GENERATION

Simpler datapath control

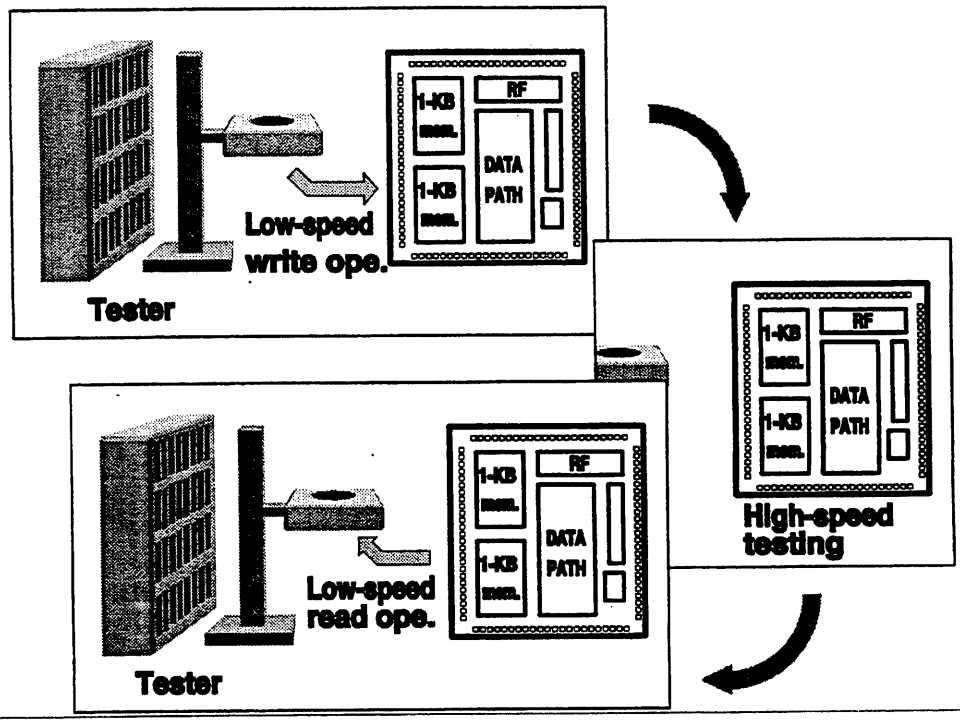
- Easily decoding instruction
  - ex. VLIW
- Encoding register forwarding operation in instruction
  - for implementing register forwarding handling
- Minimize the number of hold-stages
- Using pipeline sequencer

MINIMIZE NUMBER OF HOLD-STAGE

Data hazard occurs in "A" and "B".
Minimizing the number of hold-stages
reduces the loads of the control circuits.



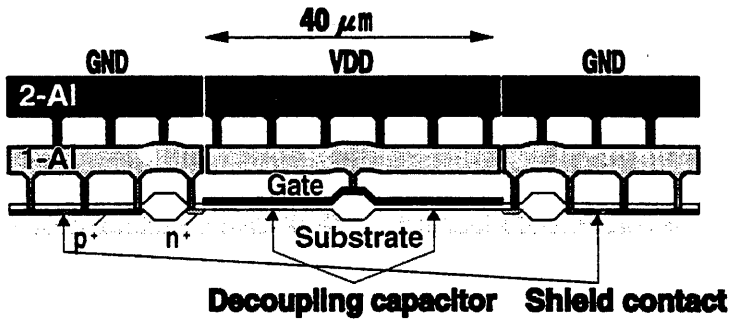
500-MHz TESTING



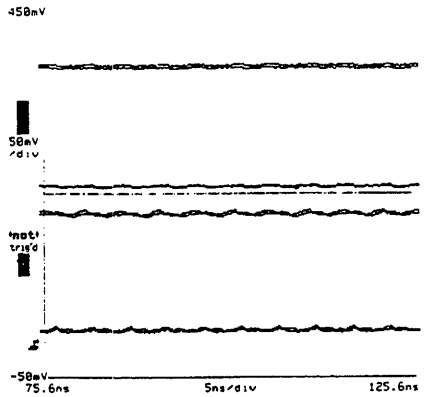
KEY CIRCUIT TECHNIQUES

- Stable power and ground lines
- High-frequency PLL clock generator
- Small-skew clock distribution strategy
- High-speed input and output buffer circuit

POWER & GROUND LINES



Power supply voltage bounce



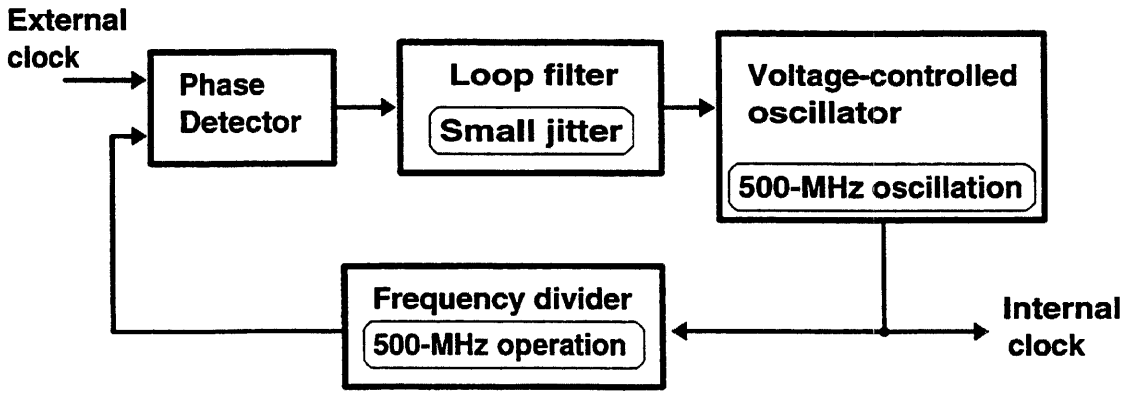
Total decoupling capacitance on chip 0.027 μF

PLL CLOCK GENERATOR

Requirements for PLL

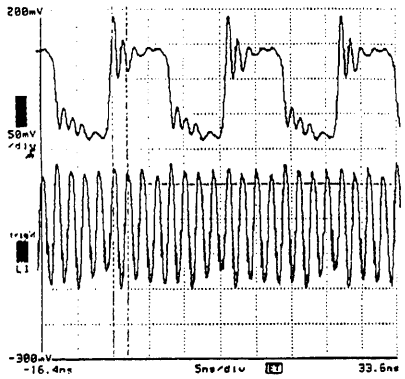
500-MHz output

Small output jitter



EXPERIMENTAL RESULTS OF PLL

PLL output waveform



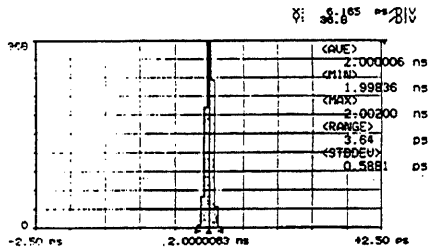
Input
62.5 MHz

Output
500 MHz

1 V/div.

5 ns/div.

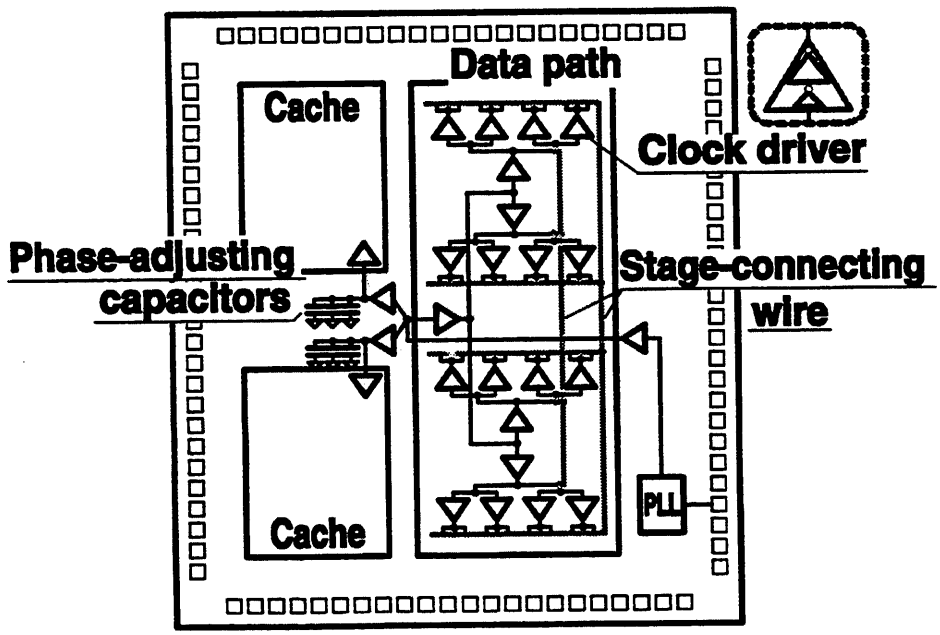
Output Jitter

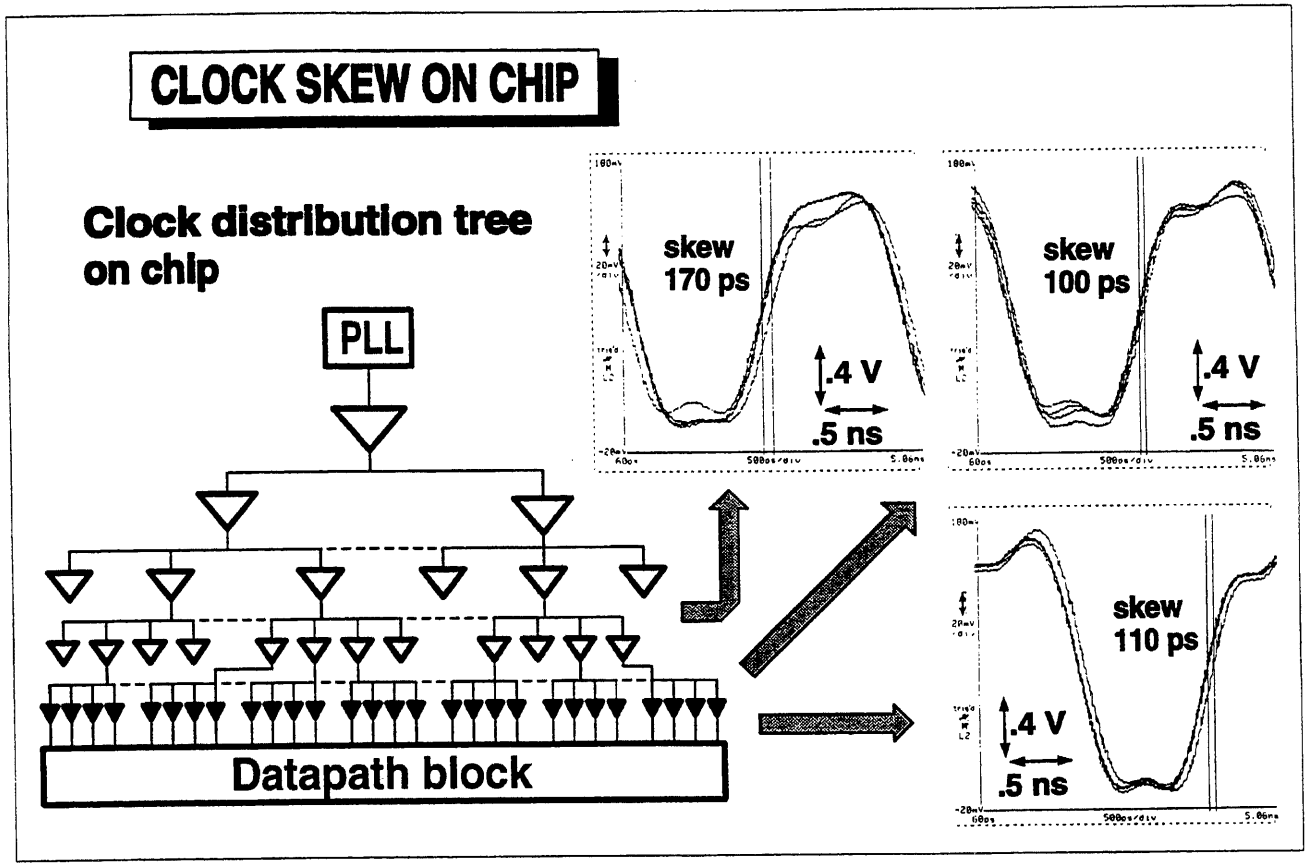


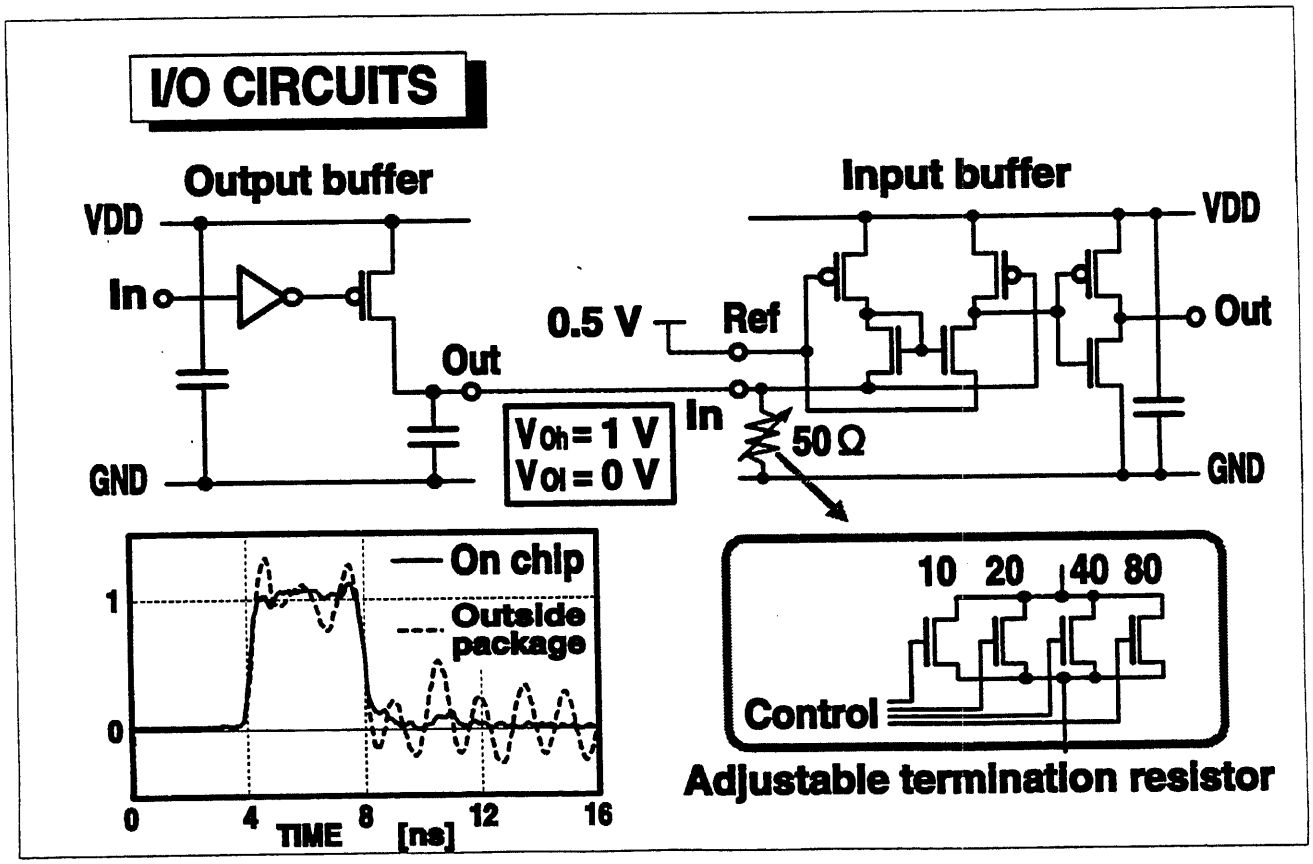
Output jitter 58 ps (3%)

(This signal is 1/16 pre-scaled.)

CLOCK DISTRIBUTION STRATEGY




CLOCK SKEW ON CHIP
Clock distribution tree on chip
PLL
Datapath block
skew 170 ps
.4 V
.5 ns
skew 100 ps
.4 V
.5 ns
skew 110 ps
.4 V
.5 ns


I/O CIRCUITS
Output buffer
VDD
In
Out
GND
Input buffer
VDD
0.5 V
Ref
Out
In
50 Ω
GND
VOh = 1 V
VOl = 0 V
On chip
Outside package
1
0
0
4
8
12
16
TIME [ns]
10 20 40 80
Control
Adjustable termination resistor

SUMMARY

- 500-MHz, 32-b, 0.4-μm CMOS RISC processor
- Architecture for high speed processor
  - 8-stage pipelined datapath
  - Simple datapath control using sequencer
  - No register forwarding in datapath
  - On chip test function
- High-speed circuit techniques
  - Power and ground line structures
  - PLL clock generator
  - Stage-connect clock distribution
  - High speed input and output buffer circuit