# POWER2+

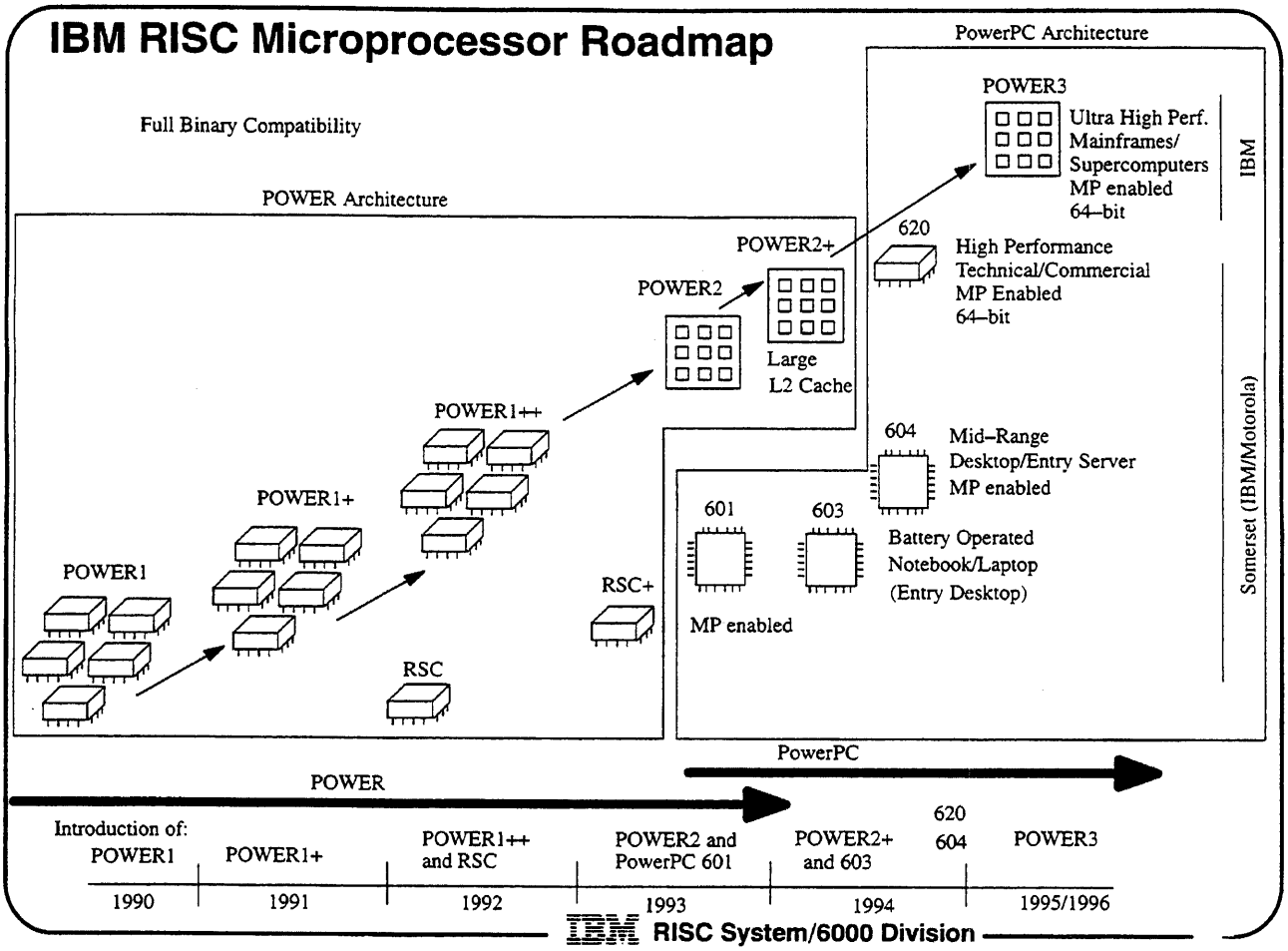
The Enhanced POWER2 Superscalar RISC Processor



## Agenda

- Microprocessor Roadmap
- Project Goals
- System Features
- Chip and Packaging Technology
- Performance Monitor
- Performance
- Summary

# IBM RISC Microprocessor Roadmap

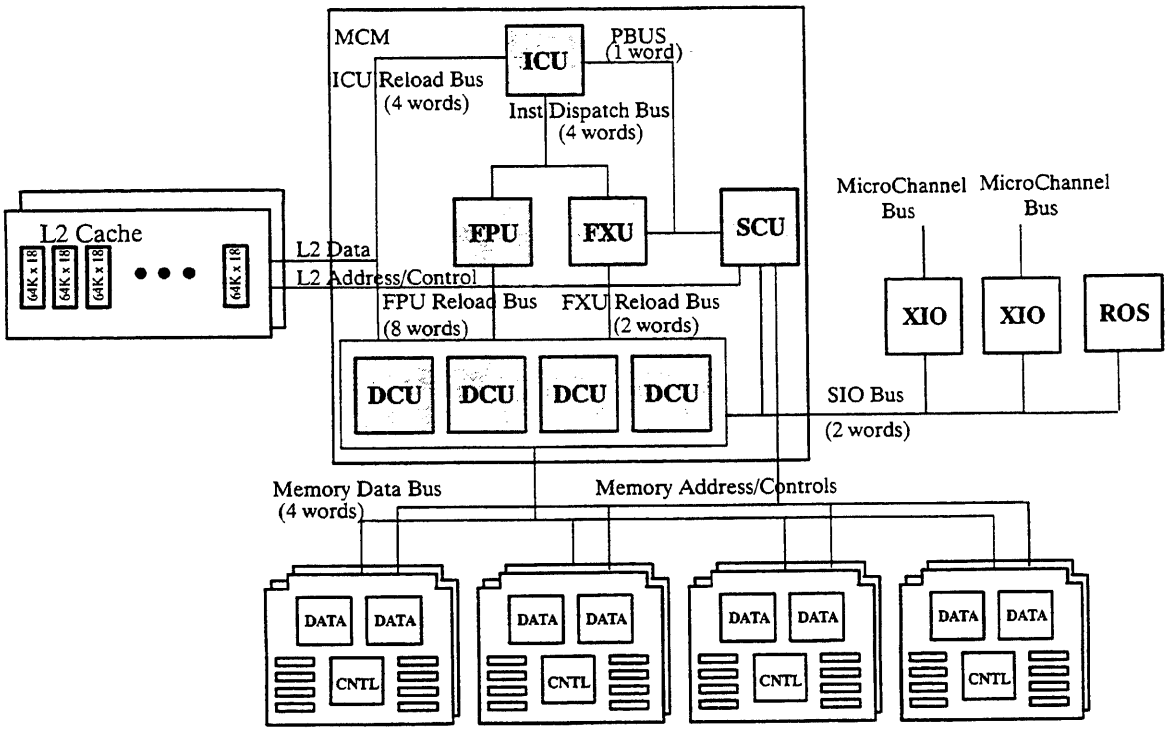





## Project Goals

- Leverage off of POWER2 design
- Target Commercial transaction processing capability on the high end
- Target cost reduced system on the low end
- Maintain competive fixed point and floating point performance

System Block Diagram, 4–word L2 Cache and Memory Bus

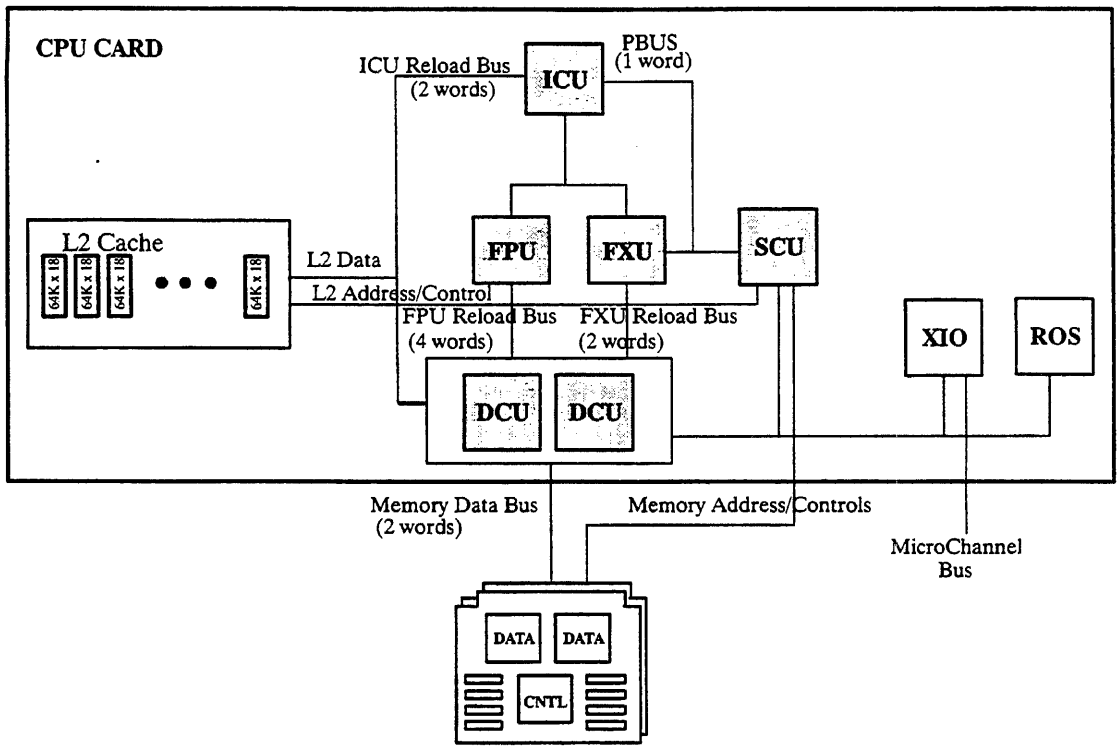





## High Performance MCM Chip Set for Servers

- 4 Data Cache Unit Chips
  - 128 Kbytes of DCache
- 32 Kbyte ICache
- 512 Kbyte – 2 Mbyte L2 Cache
- 4 Word Memory Interface
  - Minimum Memory Configuration of two memory cards
  - 64 Mbyte – 2048 Mbyte
- Ceramic Multi–Chip Module (MCM) CPU Package

System Block Diagram, 2–word L2 Cache and Memory Bus

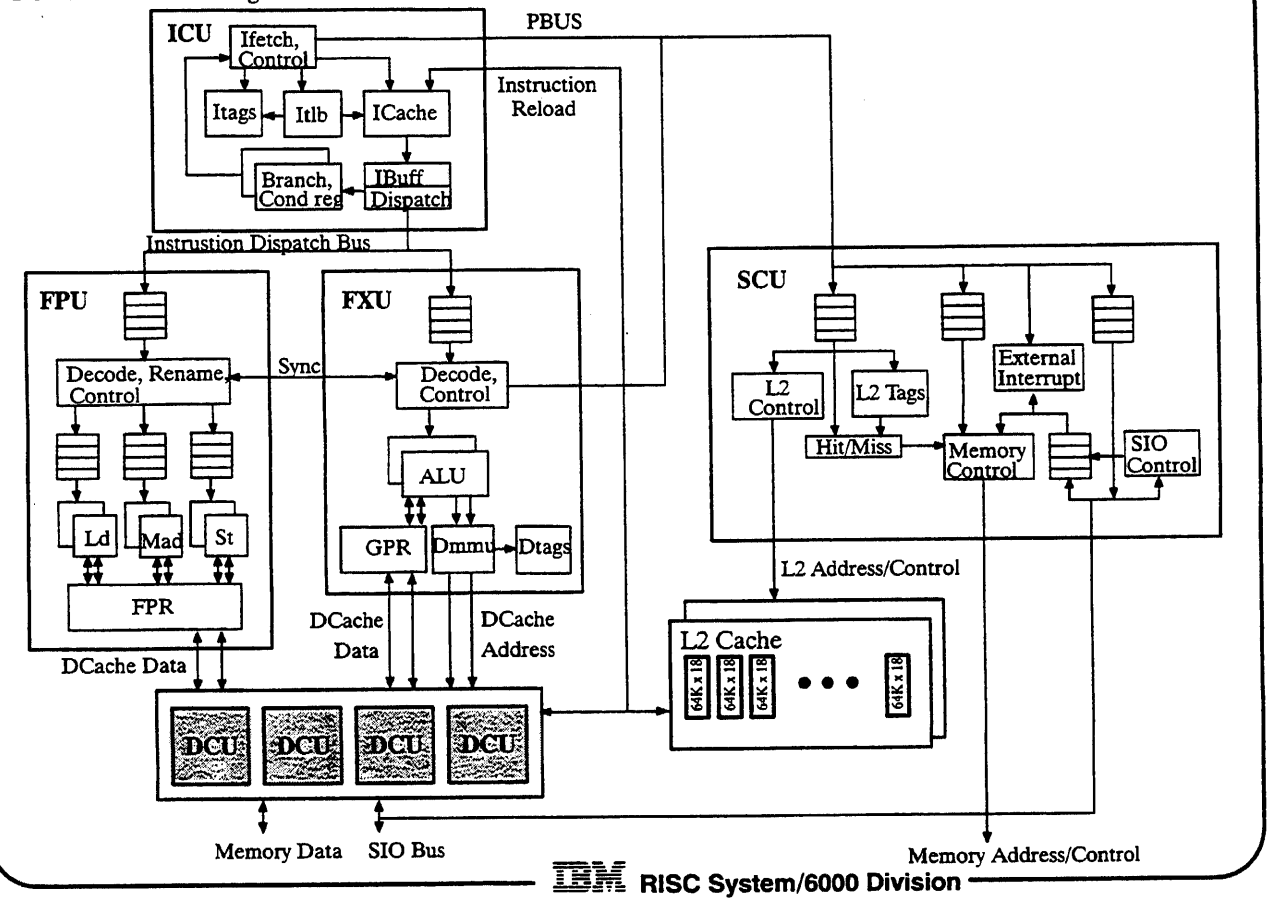





## Cost Reduced Chip Set for Desktop Systems

- 2 Data Cache Unit Chips
  - 64 Kbytes of DCache
- 32 Kbyte ICache
- 512 Kbyte – 1 Mbyte L2 Cache
- 2 Word Memory Interface
  - Minimum Memory Configuration of one memory card
  - 32 Mbyte – 512 Mbyte
- Single Chip Solder Ball Connect (SBC) CPU Package

**POWER2+ Block Diagram**






## Processor Core Features

- 6 Instruction Dispatch
- 8 Operations/cycle
- Large, multi–ported Data Cache
- High bandwidth buses
- Dual Fixed Point, Floating Point, Branch Units

## Optimized L2 Cache Subsystem

- 512 KB, 1 MB, 2 MB Second Level Cache
- Direct–Mapped, 128 byte line
- Store–through – Overlapped write to L2 and Memory
- Industry standard Burst SRAM
  - 2–1–1–1 Cache Hit Read and Write Timing
- Run at CPU clock speed
- Single bit correct, double bit detect ECC for all L2 Cache Accesses



## Storage Control Unit L2 Cache Features

- Programmable Second Level Cache and Main Memory Size
- Programmable Bus Width
- Integrated L2 Cache Tag RAM
- Overlapped L2 Tag lookup/compare with DRAM access
  - Single cycle L2 Tag lookup
  - DRAM access never started on L2 Cache Hit
  - No Memory cycle penalty for L2 Cache Miss
- Direct Store Segment Load/Store to L2 directory and data

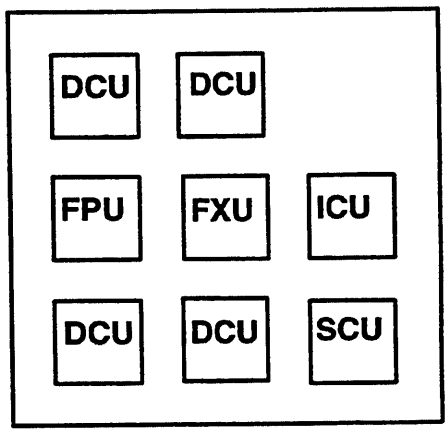
## CMOS Technology

- Lithography length of .7 micron
- Effective Channel length of .45 micron
- 4 levels of metal wiring
- 1 level of polysilicon
- 12.7 x 12.7 mm (ICU, FXU, FPU)
- 11.7 x 9.55 mm (DCU, SCU)

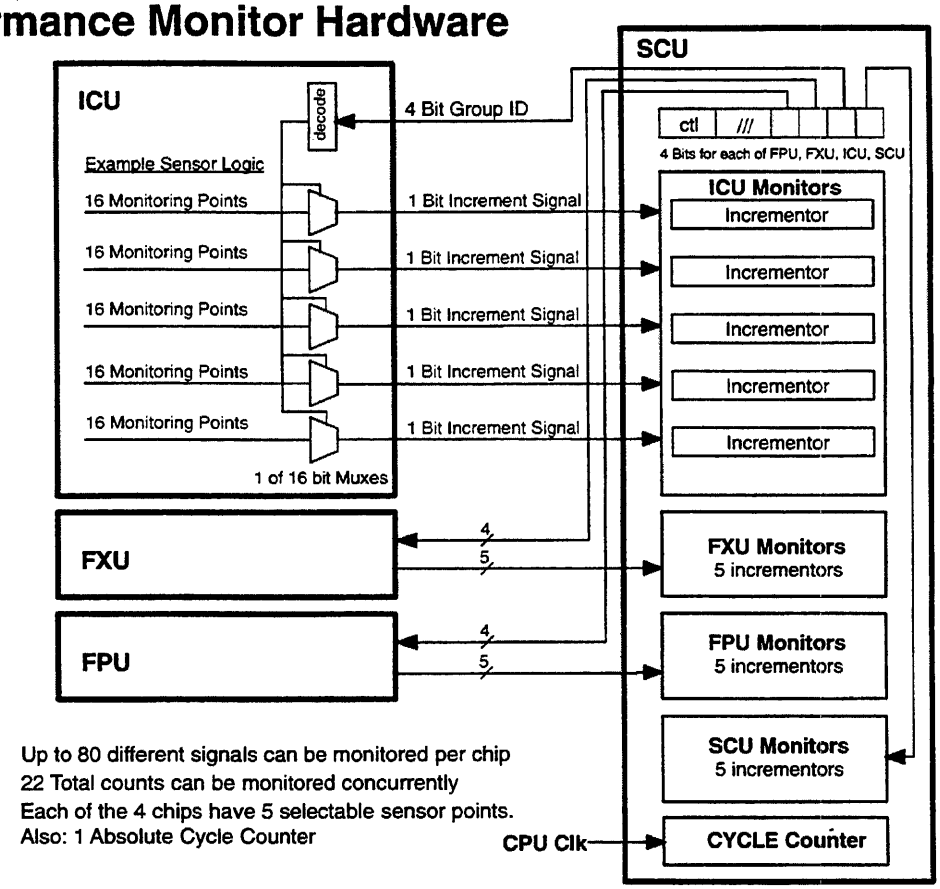


## Multi–Chip Module (MCM) Technology

- 64 x 64 mm
- 44 Total Planes
- 20 Signal Planes
- Maximum power 60 watts
- 512 signal pins



# Performance Monitor Hardware




Up to 80 different signals can be monitored per chip
22 Total counts can be monitored concurrently
Each of the 4 chips have 5 selectable sensor points.
Also: 1 Absolute Cycle Counter



| SAMPLE OF TPC–C RESULTS | 59H (1M L2) | 390 (512K L2) |
|---|---|---|
| Percent FXU instructions | 75.9% | 74.5% |
| Percent ICU instructions | 24.1% | 25.5% |
| Percent FPU instructions | 0.01% | 0.01% |
| Percent FXU ops executed by FXU0 unit | 67% | 68% |
| Percent FXU ops executed by FXU1 unit | 33% | 32% |
| CPI (cycles per instruction) | 1.40 | 1.68 |
| Percent conditional branches | 33% | 34% |
| Percent conditional branches taken | 58% | 58% |
| Average basic block length (instructions) | 4.1% | 4.1% |
| I–Cache miss rate (per instruction) | 2.65% | 2.73% |
| D–Cache miss rate (per instruction) | 0.88% | 1.38% |
| I–TLB miss rate (per instruction) | 0.13% | 0.14% |
| D–TLB miss rate (per instruction) | 0.16% | 0.16% |
| Avg memory references to satisfy TLB miss | 0.61 | 0.78 |
| % hit in L2 per I–Cache L1 miss | 85.4% | 74.6% |
| % hit in L2 per D–Cache L1 miss | 38.1% | 16.6% |

## Low–End Performance

| System | RS/6000 model 375 | RS/6000 model 380 | RS/6000 model 390 |
|---|---|---|---|
| CPU | POWER1 | POWER2+ | POWER2+ |
| Clock rate | 62.5 Mhz | 59 Mhz | 67.0 Mhz |
| SPECint92 | 70.3 | 99.3 | 114.3 |
| SPECfp92 | 121.1 | 187.2 | 205.3 |
| Linpack | 25.9 | 49.7 | 55.1 |

## Mid–Range Performance

| System | RS/6000 model 580 | RS/6000 model 590 | RS/6000 model 59H |
|---|---|---|---|
| CPU | POWER1 | POWER2 | POWER2+ |
| Clock rate | 62.5 Mhz | 66.5 Mhz | 66.7 Mhz |
| SPECint92 | 73.3 | 121.6 | 122.4 |
| SPECfp92 | 134.6 | 259.7 | 250.7 |
| Linpack | 38.1 | 131.8 | 132.0 |
| TPC–C (tpmC) | – | 726.1 | 1122.3 |
| K$/tpmC | – | 1.6 | 1.0 |



## High–End Performance

| System | RS/6000 model 980 | RS/6000 model 990 | RS/6000 model R24 |
|---|---|---|---|
| CPU | POWER1 | POWER2 | POWER2+ |
| Clock rate | 62.5 Mhz | 71.5 Mhz | 71.5 Mhz |
| SPECint92 | 73.3 | 131.0 | 134.1 |
| SPECfp92 | 134.6 | 279.0 | 273.8 |
| Linpack | 38.1 | 141.6 | 141.0 |
| TPC–A (tpsA) | 160.3 | 275.6 | 357.2 |
| K$/tpsA | 10.1 | 7.0 | 7.3 |

## POWER2+ Summary

- High Performance Superscalar RISC Processor
- Optimized L2 Cache subsystem
- High bandwidth buses
- High performance, cost reduced desktop system
- Industry leading Commercial transaction processing system