HOT CHIPS

August 14, 1994 — Memorial Auditorium

Sunday Tutorial Schedule

7:30 – 8:30	**Registration & Coffee at Memorial Auditorium**
8:30 – 12:00	**Algorithms and Hardware for Video Compression**
12:00 – 1:00	**Lunch**
1:00 – 4:30	**Instruction-Set Extensions for Multiprocessor Interconnects**
4:30 – 6:30	**Wine & Cheese Reception in the Dohrmann Grove just north of the Hoover Tower on Serra Street.**

Additional On-Site Registration will be available for an hour before the sessions begin on Monday and Tuesday.

Algorithms and Hardware for Video Compression
Teresa H. Meng, Stanford University

This tutorial will give an overview of the industry standards for video compression, including compression algorithms, performance comparisons and hardware implementations. Fast algorithms to achieve real-time encoding and decoding will be one focus of this tutorial. Besides industry standards, recent developments in compression techniques, such as subband and wavelet filtering and vector quantization will be covered. Finally research activities in the area of low-power implementations for portable video applications will be surveyed.

Instruction-Set Extensions for Multiprocessor Interconnects
David V. James, Apple Computer

Most instruction sets have been optimized for uniprocessor environments. To effectively utilize multiprocessors on scalable interconnects, processors need to support additional capabilities, including 64-bit addressing, a well-defined set of memory-access capabilities (loads, stores, and locks), non-blocking interrupts and synchronized time-of-day clocks. As background, the constraints of a typical high-speed interconnect, ANSI/IEEE Std 1596-1992 Scalable Coherent Interface (SCI), are considered. We show that specialized signals (such as bus-lock and interrupt) as well as eavesdrop or broadcast-based protocols can be avoided, explicit lock instructions (such as fetch&add) scale better than LoadReserved- and StoreConditional-based instruction sequences, and mixed endian data types (big and little) require minimal hardware (but significant compiler) support. We show how these considerations impact the design of processor instruction-set extensions.

Organizing Committee for HOT Chips VI

General Chair
John Mashey, Silicon Graphics
Program Committee Co-Chairs
Donald Alpert, Intel
Alan Jay Smith, UC Berkeley
Vice Chair
Nam Ling, Santa Clara University
Local Arrangements
Alan Johnson
Cary Kornfeld, Interval Research
Registration
Robert Stewart, Stewart Research Enterprises
Publications
David Gustavson, SCI Technical Consortium
Finance
Dennis Reinhardt, Intel
Publicity
S. Diane Smith, Consultant
Tutorials
Qiang Li, Santa Clara University
At Large
Martin Freeman, Philips Research
John Hennessy, Stanford University

Monday

August 15, 1994 — Memorial Auditorium

9:00 - 9:15 **Welcome and Opening Remarks**
John Mashey, General Chair
Don Alpert and Alan Jay Smith, Program Co-Chairs

9:15 - 10:45 **Session 1: CPUs—1**
Session Chair: Norman P. Jouppi, DEC WRL

10:45 - 11:15 **Break**

11:15 -12:45 **Session 2: Multiprocessors and Encryption**
Session Chair: Howard Sachs, Sun Microsystems

12:45 - 2:15 **Lunch**

2:15 - 3:45 **Session 3: Networks, Communications**
Session Chair: Forest Baskett, Silicon Graphics

3:45 - 4:30 **Break**

4:30 - 5:30 **Session 4: CPUs - 2**
Session Chair: Don Alpert, Intel Corporation

5:30 - 7:00 **Monday Evening Buffet Dinner**

7:00 - 9:00 **Evening Panel Session**
The Investor (Venture) Community View of What's Hot
Moderator: Forest Baskett, Silicon Graphics

Panelists:

Cliff Friedman, Senior Managing Director, Bear Stearns
Stephen Shapiro, Portfolio Manager, Tiger Management
Peter Thomas, General Partner, Institutional Venture Partners

Tuesday

August 16, 1994 Memorial Auditorium

9:00 - 10:00 **Session 5: Chipsets**
Session Chair: Allen Baum, Apple Computer

1 0:00 - 1 0:30 **Break**

10:30 - 12:30 **Session 6: Graphics**
Session Chair: Ruby Lee, Hewlett Packard

12:30 - 2:00 **Lunch**

2:00 - 3:30 **Session 7: Video**
Session Chair: Anoop Gupta, Stanford University

3:30 - 4:00 **Break**

4:00 - 6:00 **Session 8: CPUs - 3**
Session Chair: Alan Jay Smith, University of California, Berkeley

6:00 Closing Remarks
