

# PowerPC™ 601 Microprocessor

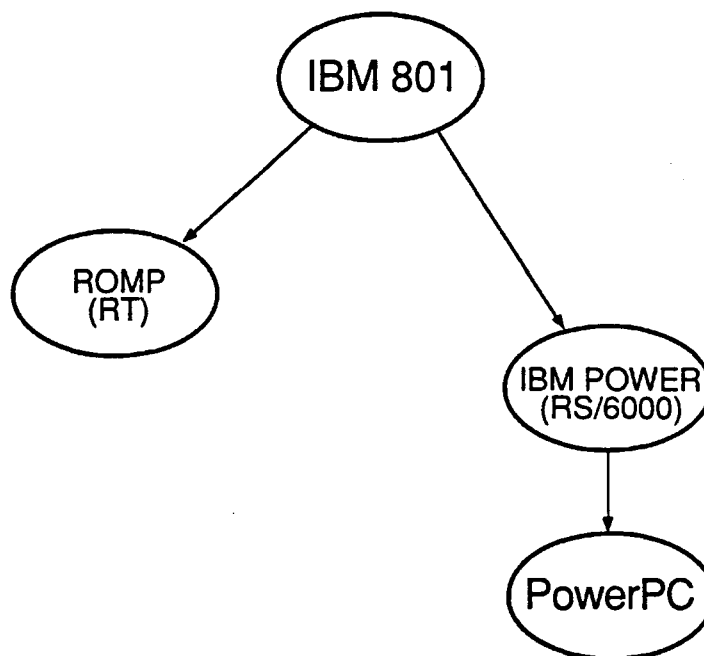
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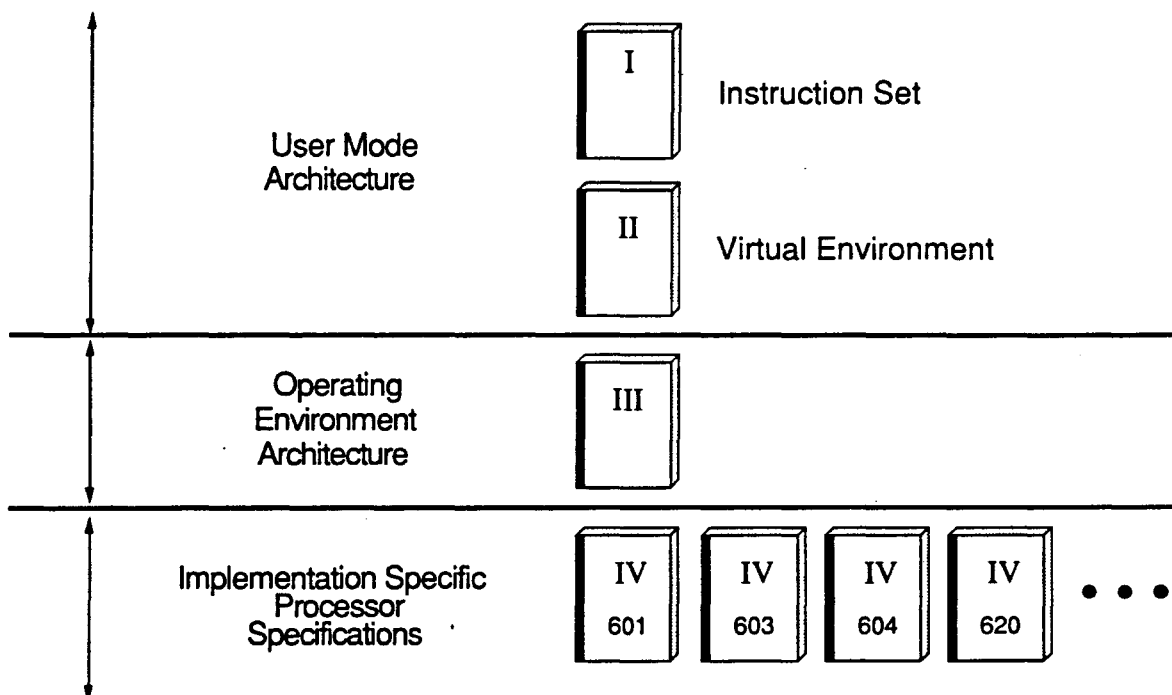
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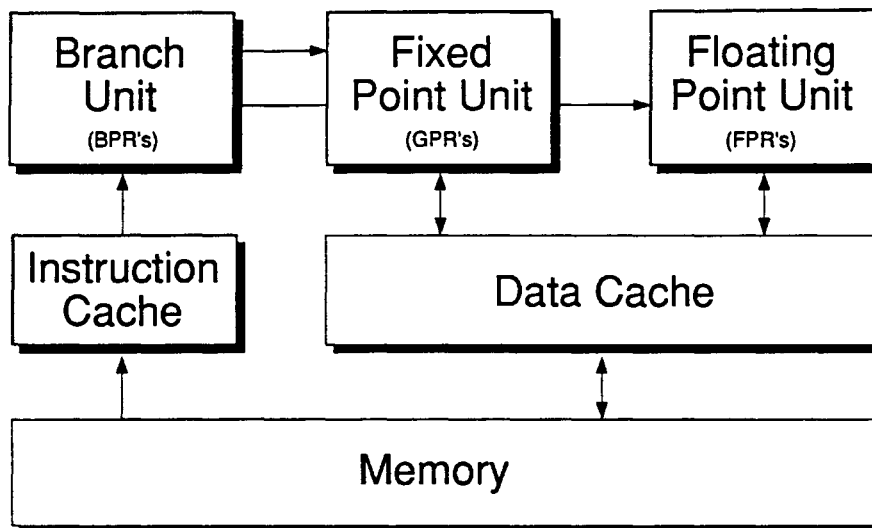
## PowerPC™ Architecture Genealogy



- PowerPC Architecture changes made to:
  - Simplify implementations
  - Support increased clock rates
  - Support more aggressive superscalar designs
  - Extend the architecture to 64-bits
  - Improve multiprocessor support
  - Clean up architectural model
  
- POWER Architecture compatible (old binaries run).
  - Trap and software emulate missing POWER features.

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- RISC instruction set architecture
- Superscalar architectural model
- Fully interlocked pipelines
- Large linear logical address space
- Very large segmented virtual address space
- Weak storage ordering

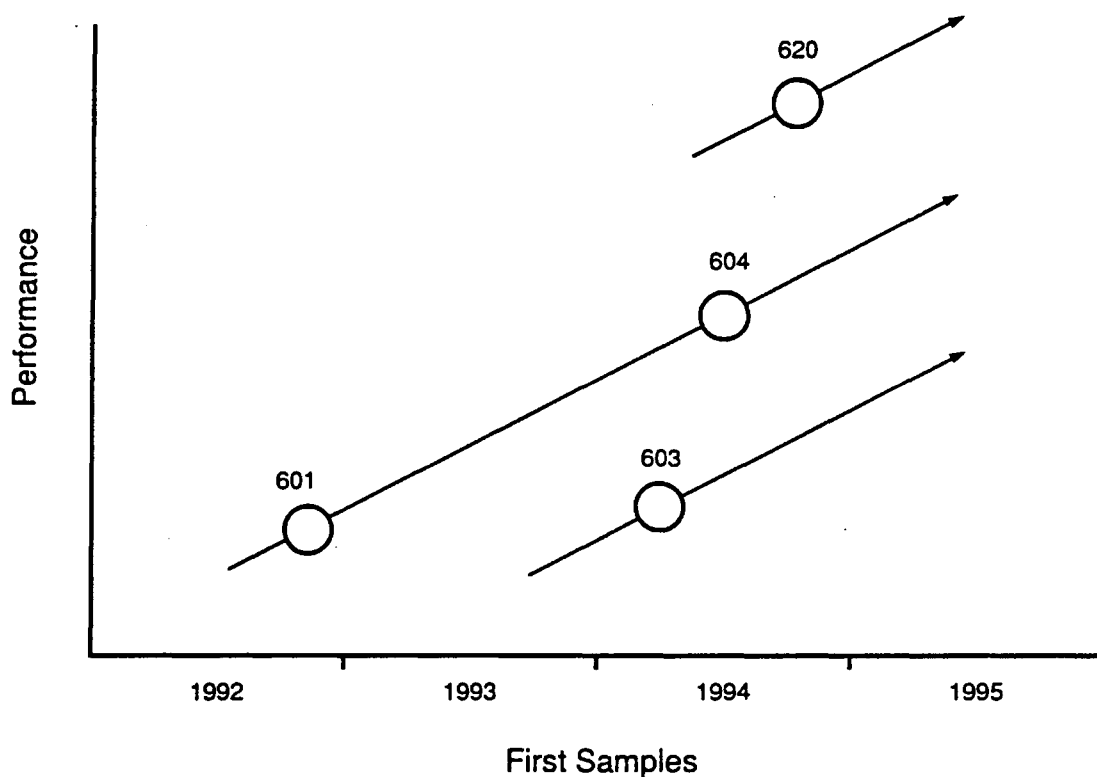
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- True RISC architecture
  - fixed width consistently encoded instruction format
  - register-to-register (load/store) architecture
  - simple operand addressing modes
  - simple instructions
- Compound instructions for path length reduction (update, fmul-add)
- Condition code branch model with optional condition record
- Independent fixed-point, floating-point and branch register sets
- Non-destructive three-operand address formats
- IEEE double precision floating-point
- Big-endian byte addressing
- Weak storage ordering
- User-mode cache control instructions

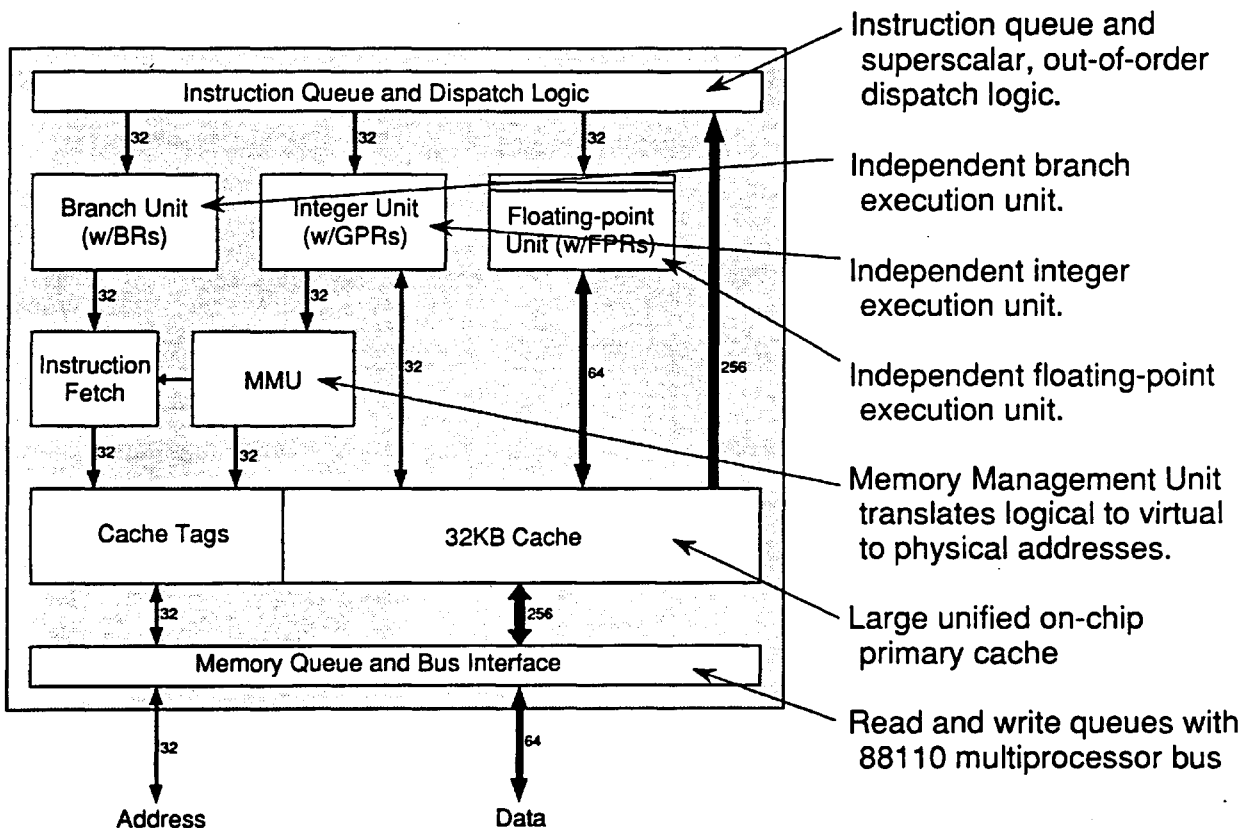
- Removed the MQ register (eliminated extended shifts, reworked mul & div)
- Removed some clock limiting ops.
- Removed LSCBX (complex string-op).
- Removed 3 source operand fixed-point instructions.
- Relaxed unnecessary specifications to simplify implementations.
- Added unsigned integer multiply and divide.
- Added a fixed-point subtract w/o carry and a byte sign extend.
- Added single-precision floating-point and convert-to-integer.
- Added static branch prediction
- Simplified the real-time clock definition
- Improved cache control operations.
- Defined the cache consistency model.
- Defined weakly ordered storage model and synchronization primitives
- Added multiprocessor storage locking instructions.
- Added little-endian addressing mode switch.
- Extended architecture to full 64-bits (with 32-bit compatibility).

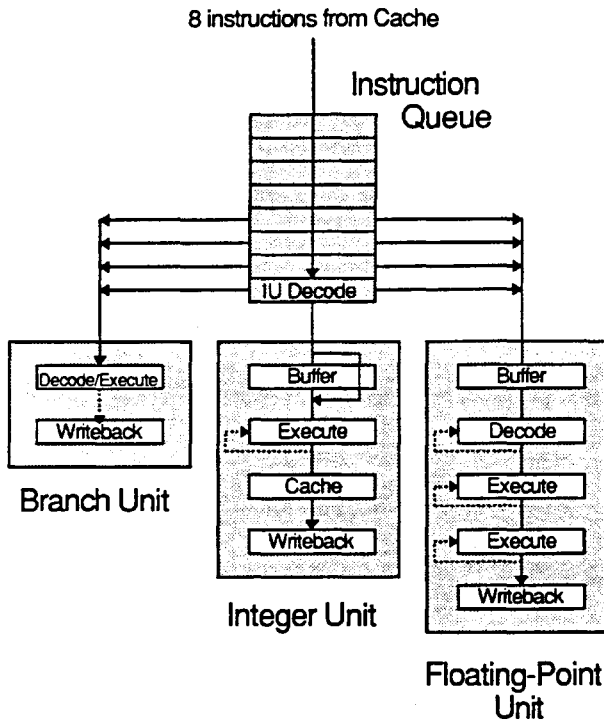
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- Quick time-to-market
  - Early PowerPC software development
  - Accelerate PowerPC system availability
- Provide POWER -> PowerPC architecture bridge
  - Superset architecture - both POWER and PowerPC features
  - Run existing POWER (RS6000) binaries at full speed
  - Provide platforms for PowerPC software development
  - Allow time for compiler reoptimization to PowerPC architecture
- Provide competitive performance at a low cost point
  - Enable early development of high-volume platforms
  - 32-bit subset of the full 64-bit PowerPC Architecture
- Provide multiprocessor features not present in current RS/6000 chipsets

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**Instruction Queue**

- 8-deep queue with 8-wide fetch
- Superscalar dispatch of 3 IPC (br, int, flt)
- Out-of-order dispatch to branch and float

**Branch Unit**

- Dedicated branch address registers
- Register renaming on link register
- Condition register lookahead
- Static branch prediction
- Branch folding, zero-cycle branches

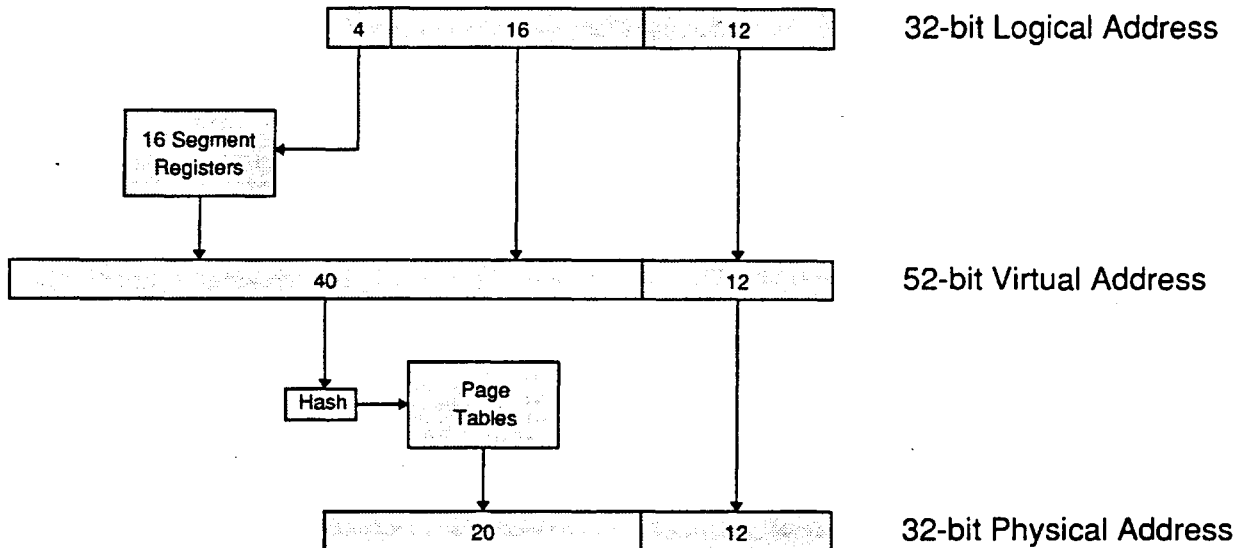
**Integer Unit**

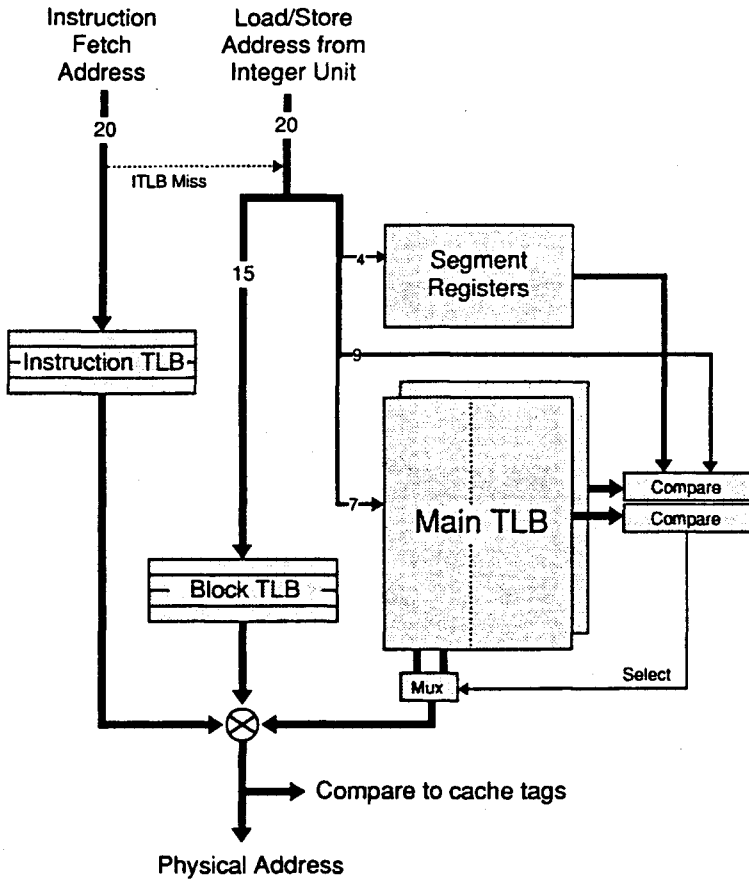
- 32-entry, 32-bit wide register file
- 4-stage (F,D,X,W) pipeline (5-stage ld/st)
- Full data forwarding
- Precise exceptions

**Floating-Point Unit**

- 32-entry double-precision register file
- IEEE-754 Single and Double float with all values and rounding modes in hardware
- Single rounding error on multiply-add
- 4-cycle latency, single cycle throughput (5/2 on dp multiply and multiply-add)

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**16 Segment-registers**

- Selected by 4 bits of logical addr.
- Produce 52-bit virtual address

**Main TLB**

- 256-entry, 2-way set-associative
- LRU replacement
- 4KB page size
- Supervisor/User, R/W protection
- Cache control
- Hardware refill from memory based hashed page tables

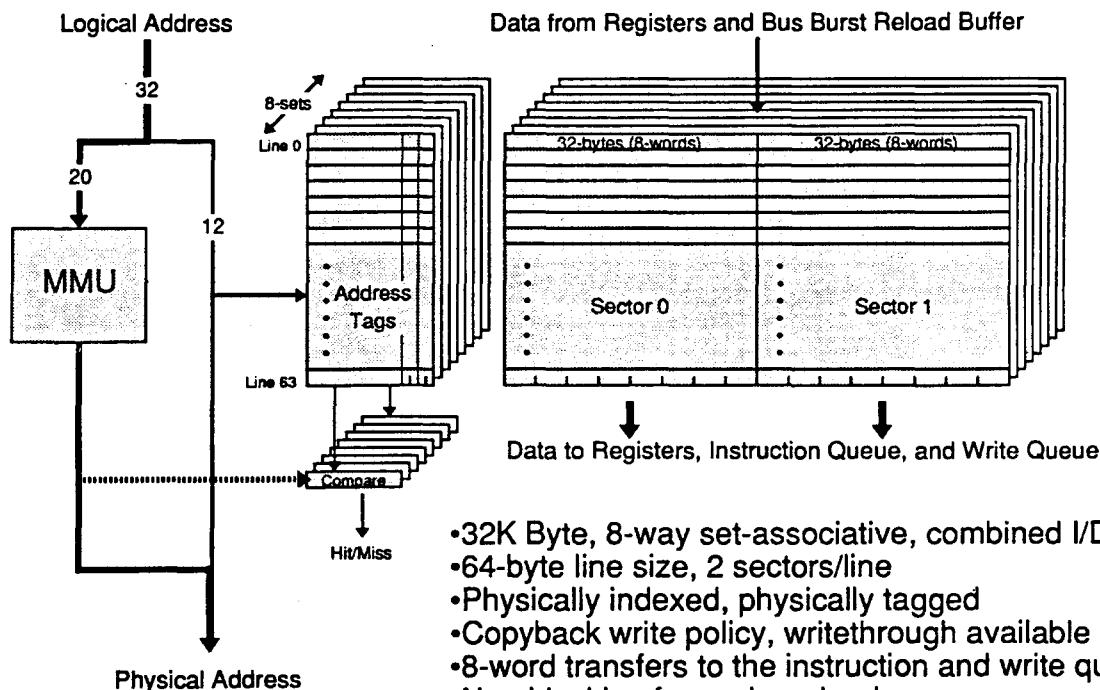
**Block TLB**

- 4 variable size blocks, 128K-8MB
- Fully associative
- Supervisor/User, R/W protection
- Cache Control

**Instruction TLB**

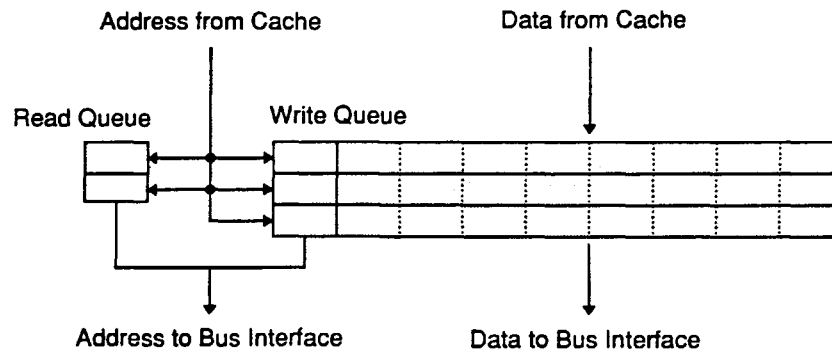
- Separate path for instr. addresses
- 4-entry, fully associative
- LRU replacement
- Always a subset of Main or Block

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- 32K Byte, 8-way set-associative, combined I/D cache
- 64-byte line size, 2 sectors/line
- Physically indexed, physically tagged
- Copyback write policy, writethrough available per page.
- 8-word transfers to the instruction and write queues
- Non-blocking for cache reloads
- Access in parallel with address translation
- Arbitration logic prioritizes access to the cache
- Dynamic reload of next sector in line when idle
- Coherency via 4-state MESI with separate snoop port
- User mode cache control instructions

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**Memory Unit**

- 2-deep read queue and 3-deep write queue
- Dynamic reordering of reads and writes
- Each write queue entry holds 1 cache sector
- One write queue entry for snoop copybacks
- Write-queue snooped for coherency
- Load & store instructions are "complete" for purposes of execution after translation and before entry onto the queues

**Bus Interface Unit**

- Adapted from Motorola MC88110
- Independent address and data busses.
- 64-bit data bus
- Burst-mode line fills & copybacks
- Pipelined addresses
- Split transactions
- Critical word forwarding
- Cache coherency maintained by snooping

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- 0.6µm CMOS Technology
- 4 levels of metal
- 10.95mm x10.95mm die
- 2.8 million transistors
- 3.6 volts
- 50 and 66MHz
- 9 Watts @ 50MHz
- TTL or CMOS levels compatible
- C4 in 304 pin QFP, 184 signal pins
- 60 SPECint92, 80 SPECflt92 (estimated @66MHz)