HARP-1 :
A 120 MHz Superscalar PA-RISC Processor

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HARP Project

- develop Hitachi Advanced RISC Processors

HARP-1 Design Goals

- Competitive Performance
- 0.5 μ m BiCMOS Technology
- PA-RISC Architecture

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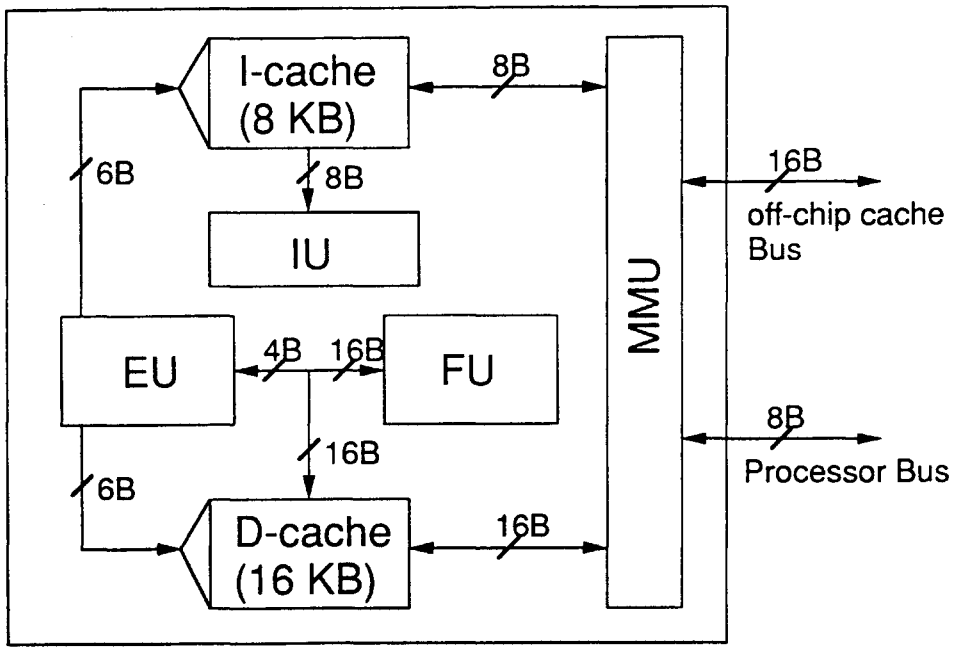
Chip Block Diagram



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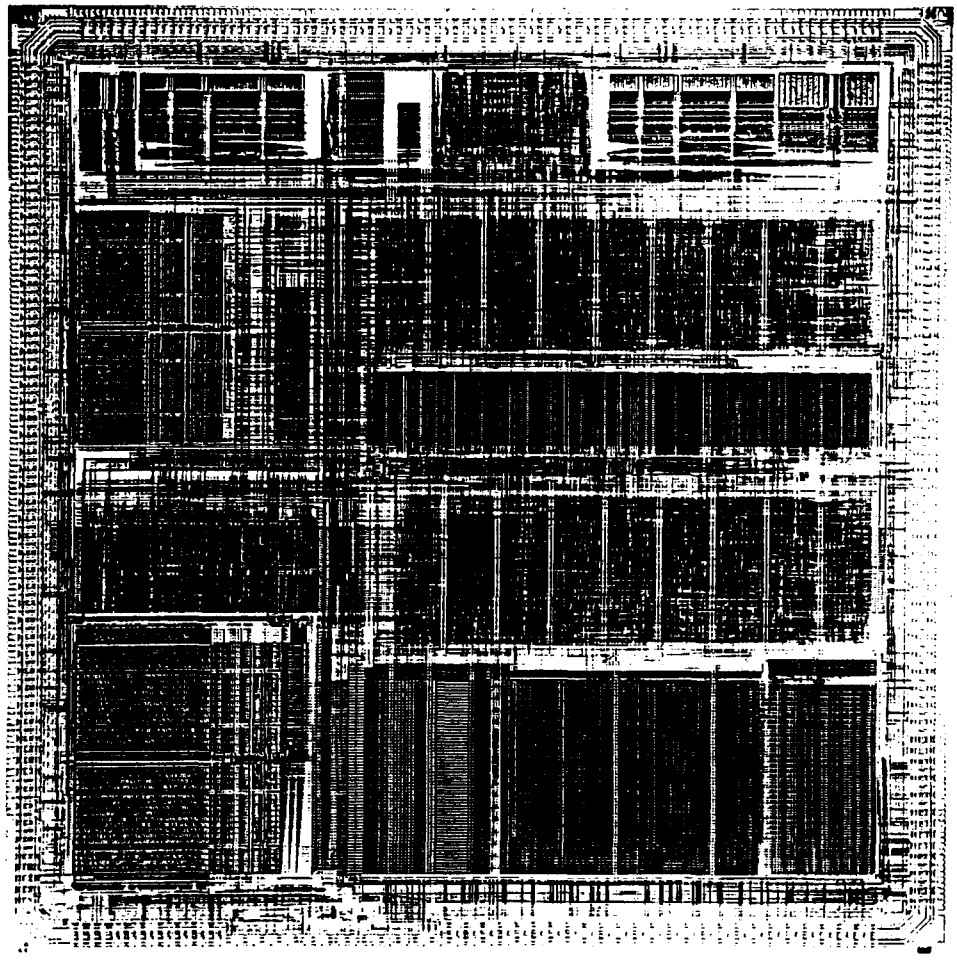

EU (execution unit)

- 2 ALUs
- 2 Shift/Merge units
- 1 PC-relative branch adder
- 7 port Register File (4 read + 3 write)
- 2 instructions execution per cycle
  (peak performance : 240 MIPS @ 120 MHz)

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FU (floating-point unit)

- fully pipelined Multiplier and Adder
- latency
  multiply : 4 cycles
  add : 4 cycles
  divide : 19 cycles
- 7 port Register File (4 read + 3 write)
- 2 instructions execution per cycle
  (peak performance : 240 MFLOPS @ 120 MHz)

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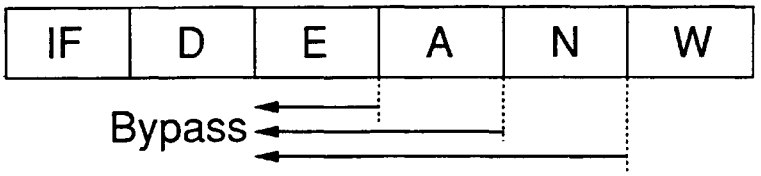
Integer Pipeline



IF : Instruction Fetch
D : Decode
E : Execution
A : Cache/TLB Access
N : Nullification / Interruption
W : GR Write

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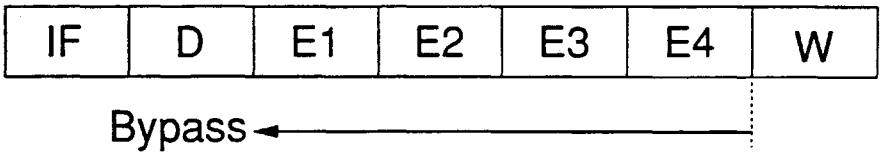
Floating-point Pipeline



IF : Instruction Fetch
D : Decode
E1– E4 : Execution
W : FPR Write

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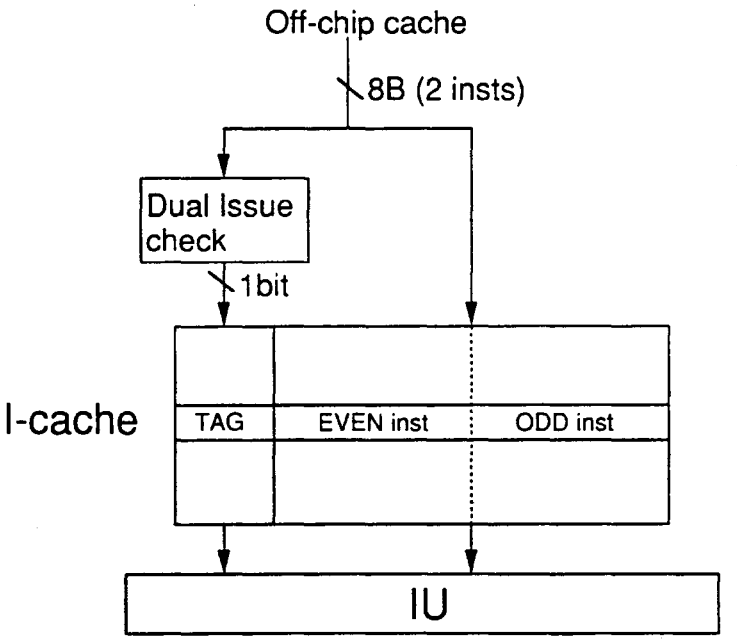
Superscalar Implementation



- 2 instructions aligned on 8B-boundary
- A tag bit in I-cache to indicate dependency between two instructions

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Dual Issue Rules

Even \ Odd	Integer	Floating	Branch	LD/ST
Integer	*	*	*	*
Floating	*	*	*	*
Branch				
LD/ST	*	*	*	

- No Register dependency
- No Resource conflict

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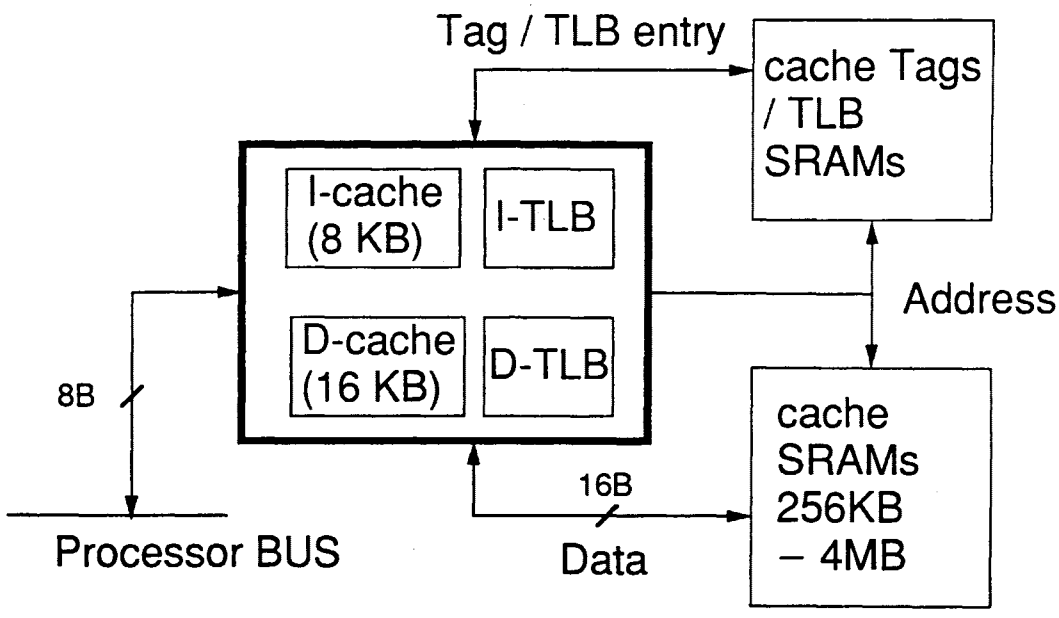
Cache/TLB Configuration



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Cache/TLB Features

On-chip Cache
- I-cache 8KB / D-cache 16KB , Direct mapping
- Store-through
- Error detection with parity

On-chip TLB
- I-TLB 128 page entries + 2 block entries , Direct mapping
- D-TLB 128 page entries + 2 block entries , Direct mapping
- Error detection with parity

On-chip Store Buffer
- 6 entries (16B/entry)

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Cache/TLB Features (cont'd)

Off-chip Cache
- 256KB – 4MB (I/D combined) , Direct mapping
- Store-in
- Error detection/correction with ECC

Off-chip TLB
- 2K – 32K page entries (I/D combined) , 2-way set-associative
- combined with cache Tags
- Error detection with parity

Processor Bus
- 8B wide
- 1/2 x processor frequency

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Logic Verification

- Event driven simulation of entire chip
  (gate level description)
- S/W Simulator with H/W accelerator on Supercomputer
  Hitachi S-820
- Number of simulated gates : apporx. 850K
- Design errors detected : 27 % of total design changes

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Physical Characteristics

Process Technology	0.5 μm BiCMOS
Cycle Time	120 MHz (8.3 ns)
Die Size	16.2 mm x 16.5 mm
Number of Transistors	2.8 million
Package	595 pin PGA
Number of Signal Pins	381
Power Dissipation	20 W @ 120 MHz
Power Supply	3.3 V

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BiCMOS Device Characteristics

Bipolar Circuit

• emitter size	0.6 μm X 4.0 μm
• h_{fe}	100
• f_t	16 GHz

CMOS Circuit

• Leff length	0.5 μm
• Tox	9 nm

Interconnection

• Layers	4 Metal layers (1 W + 3 AL)
• pitch	2 μm (W, AL1, AL2)
	4 μm (AL3)

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Performance

This slide shows Benchmark Performance.

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Conclusion

- Fast clock rate : 120 MHz (8.3 nsec)
- Selective use of 0.5 μ m CMOS and BiCMOS technology
  High density : CMOS
  Critical paths : BiCMOS
- Superscalar implementation of PA-RISC

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