Stanford Ultra Low Power CMOS

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Outline

- Motivation
- Approach
- Results
- Challenges
- Conclusions

Motivation

- Original objective: Match biological energy efficiency.
- Overall energy is minimized when leakage energy ***equals*** switching energy.
- Minimum energy is too slow for many applications: Minimize energy×time.

Energy and power

	AC	DC	SC
Power, watts (W)	aCV^2f	$I_{off}V$	$Q_{sc}Vf$
Energy, joules (J)	aCV^2	$I_{off}V/f$	$Q_{sc}V$

- Energy = "power-delay product"
- $E = Pt = P/f$
- Joules = watt·sec, watt/Hz
- 1nJ = 1mW/MHz

Reducing energy

$$E = aCV^2 + I_{off}V/f + Q_{sc}V$$

- Reduce I_{off}: Already small (1mA typ).
- Reduce Q_{sc}: 1/2 of clock, 1/8 of total; transistor sizer can make small
- $\rightarrow$ Most of the energy is in E_{ac}.

Reducing E_{ac}

$$E_{ac} = aCV^2$$

- Reduce a: Power management of inactive circuits.
- Reduce C: Circuit design, clocking.
- Reduce V: Quadratic improvement.
- V: 5 $\rightarrow$ 0.5V reduces energy by 100$\times$.
- Also makes chip run ***slow***: 100KHz typ.

Our approach

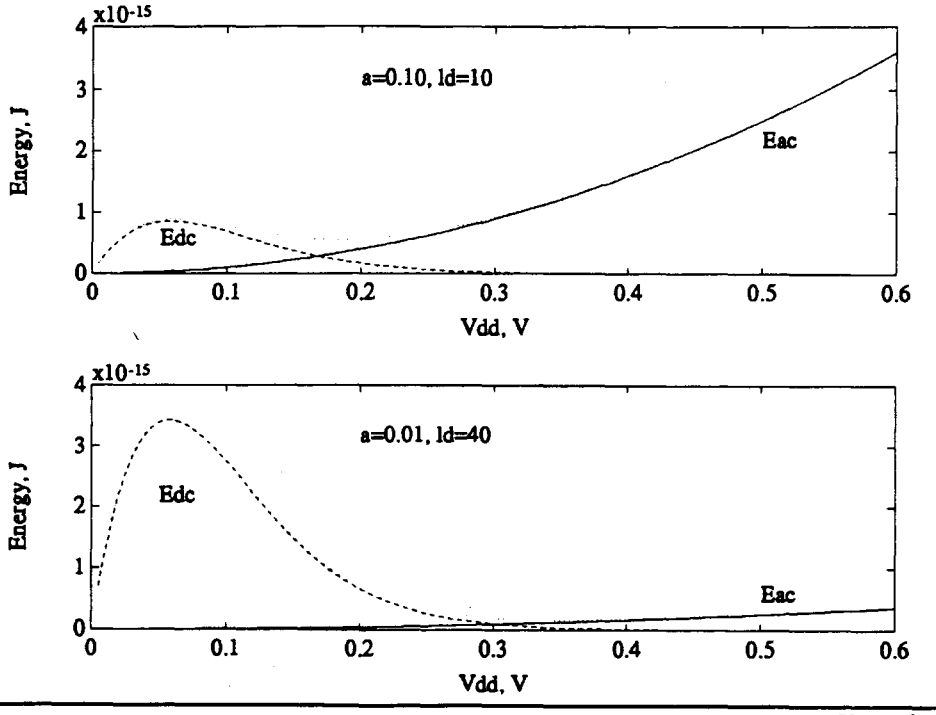
- Modify the ***process*** to achieve good performance at low voltage.
- How? Reduce threshold voltage.
- Wait: Increase leakage?!
- Key idea: Energy is minimized when $E_{ac} = E_{dc}$.
- Example:

Process	P_{ac}	P_{dc}
std CMOS	20W	2mW
ULP CMOS	200mW	200mW

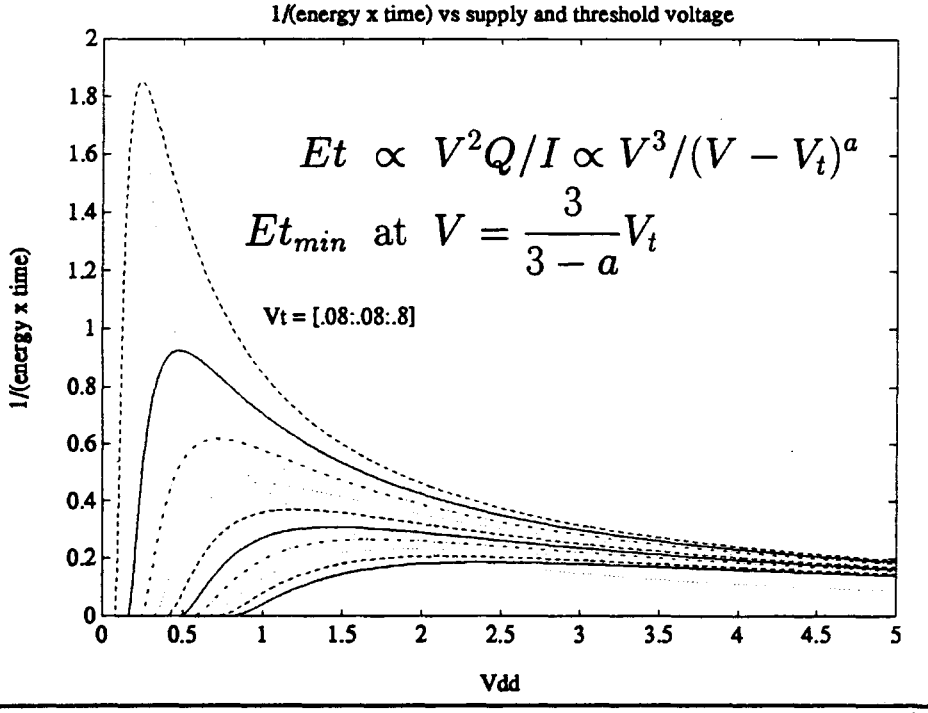
Tunable thresholds

- ULP CMOS has 1/100 the power but 100× the leakage in active circuits.
- Problem: Inactive circuits require low leakage.
- Solution: Use substrate bias to adjust device thresholds.
- $V_t = nV_T ln(ld/a)$ minimizes energy, where n is gate coupling, V_T is thermal voltage, ld is logic depth, and a is activity.
- This works out to a threshold of 120mV for active logic circuits at room temperature.

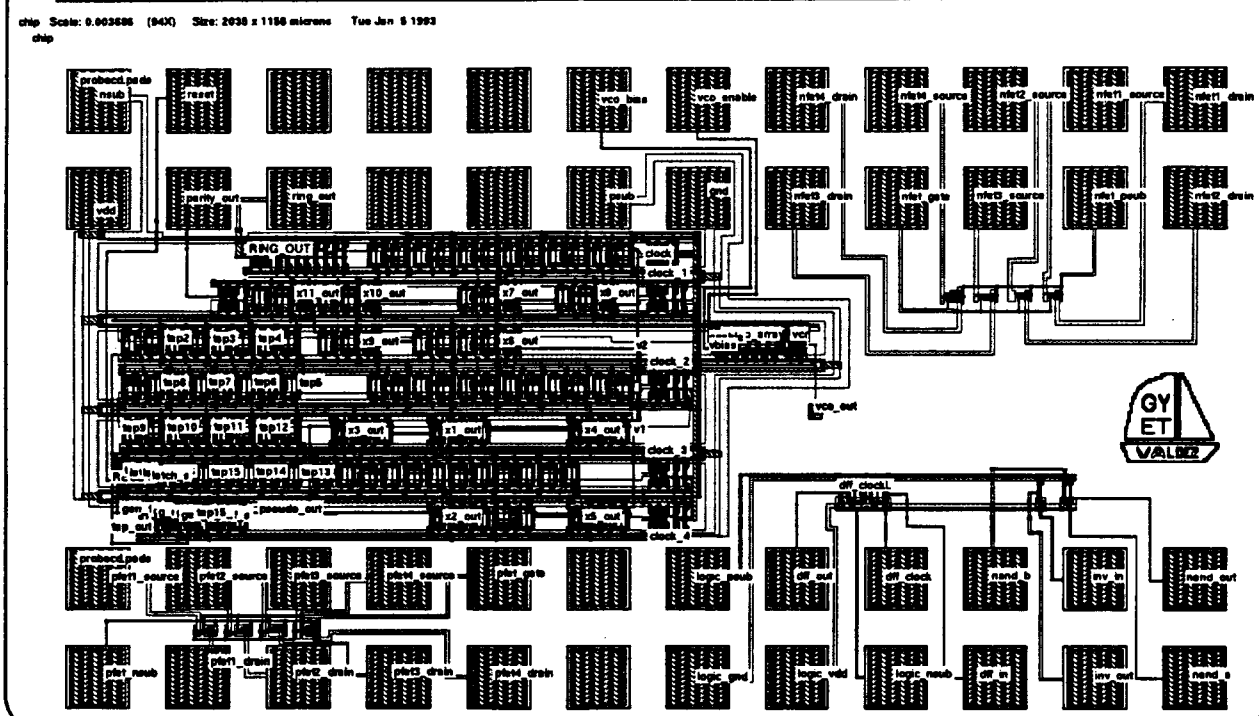
Minimum energy



Minimum energy×time

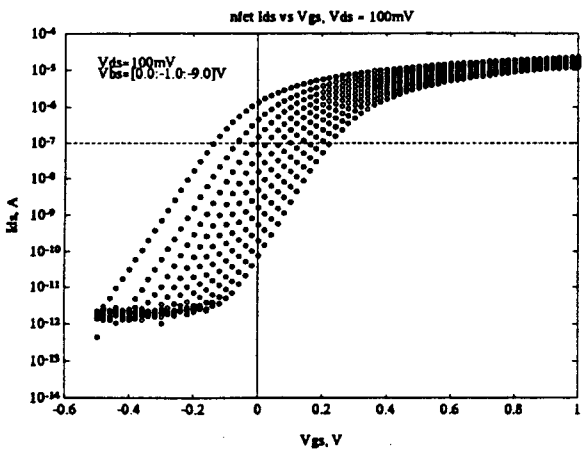


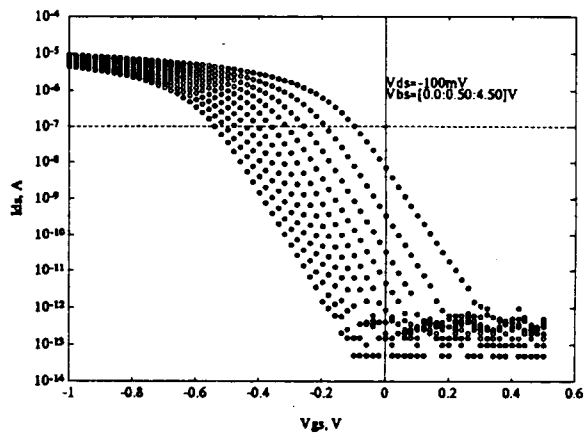
CIS1 test chip



ULP CMOS-11

Fet current





nfet

V_{t0} = -130mV

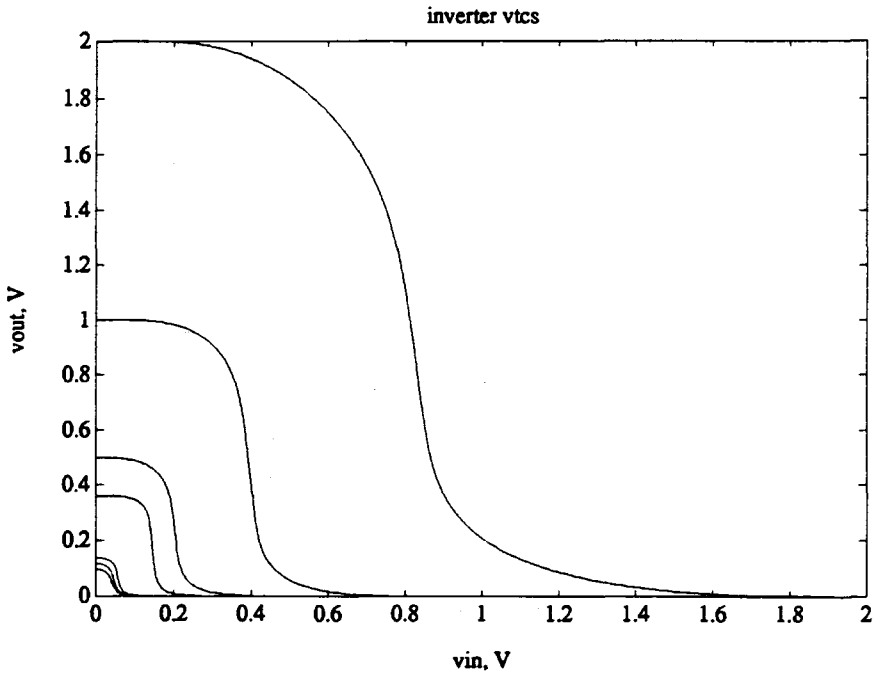
dV_{t0}/dV_b = -70mV/V

pfet

V_{t0} = -70mV

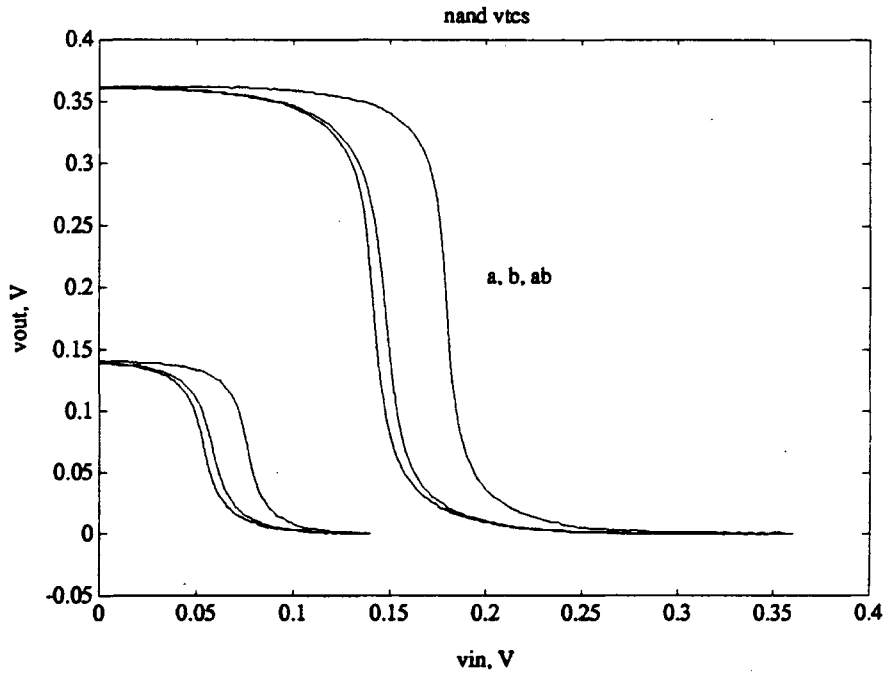
dV_{t0}/dV_b = -200mV/V

Inverter VTCs



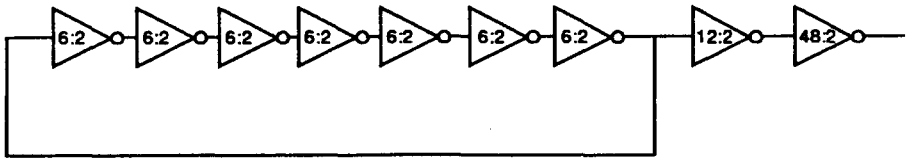
ULP CMOS-13

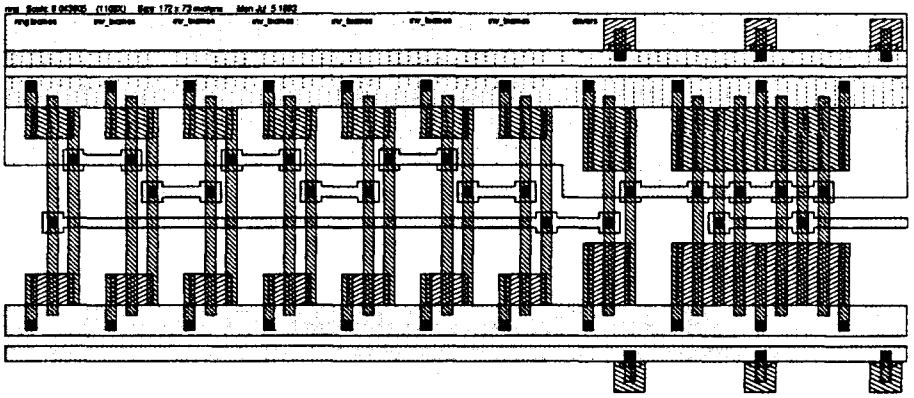
Nand VTCs



ULP CMOS-14

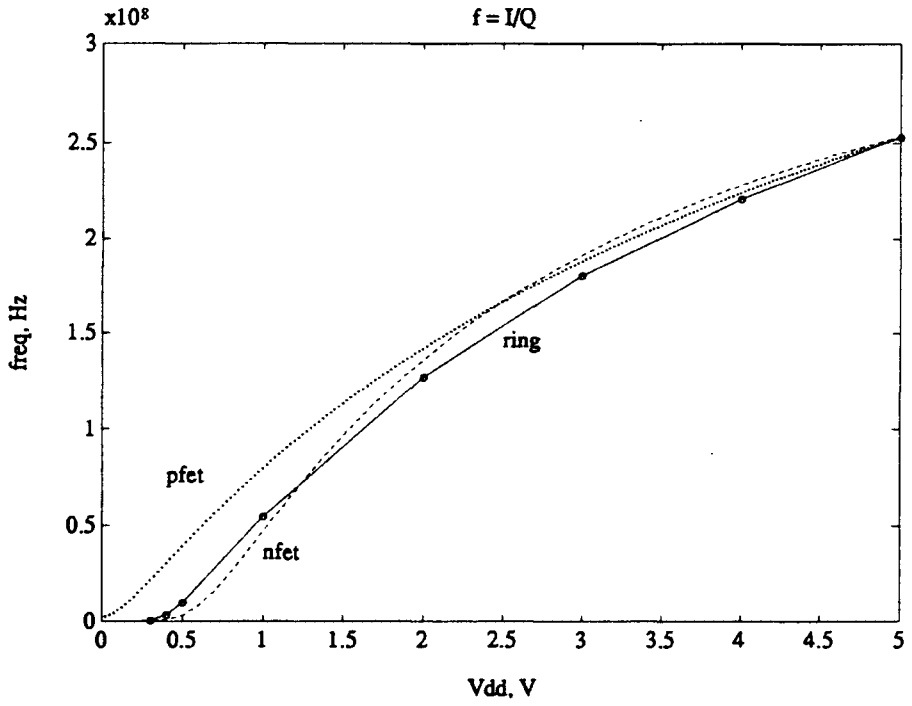
7-stage ring oscillator





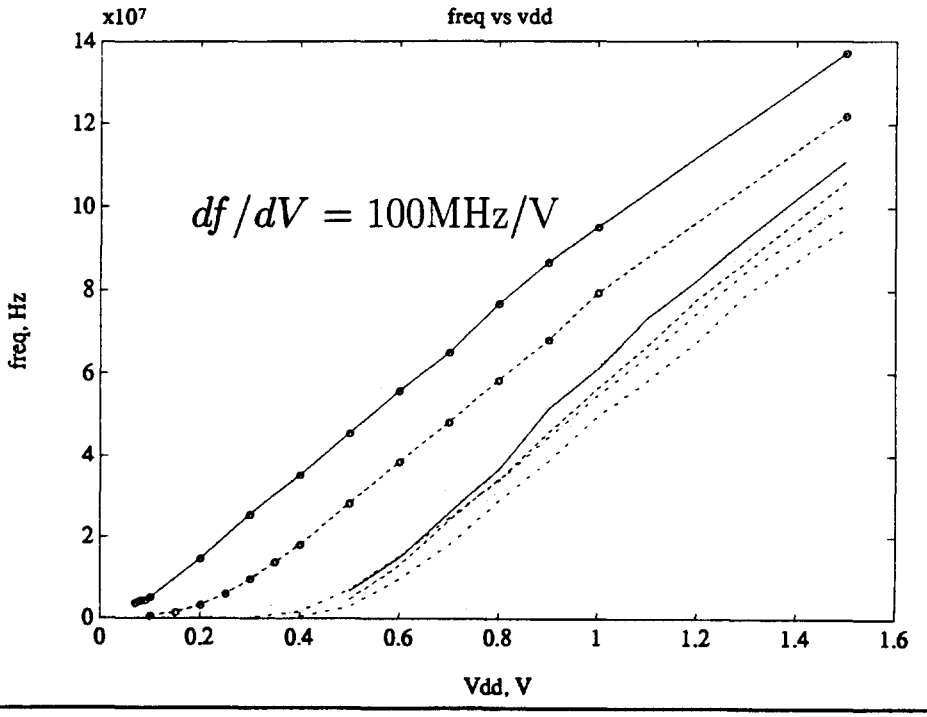
ULP CMOS-15

Ring oscillator $f = I/Q$



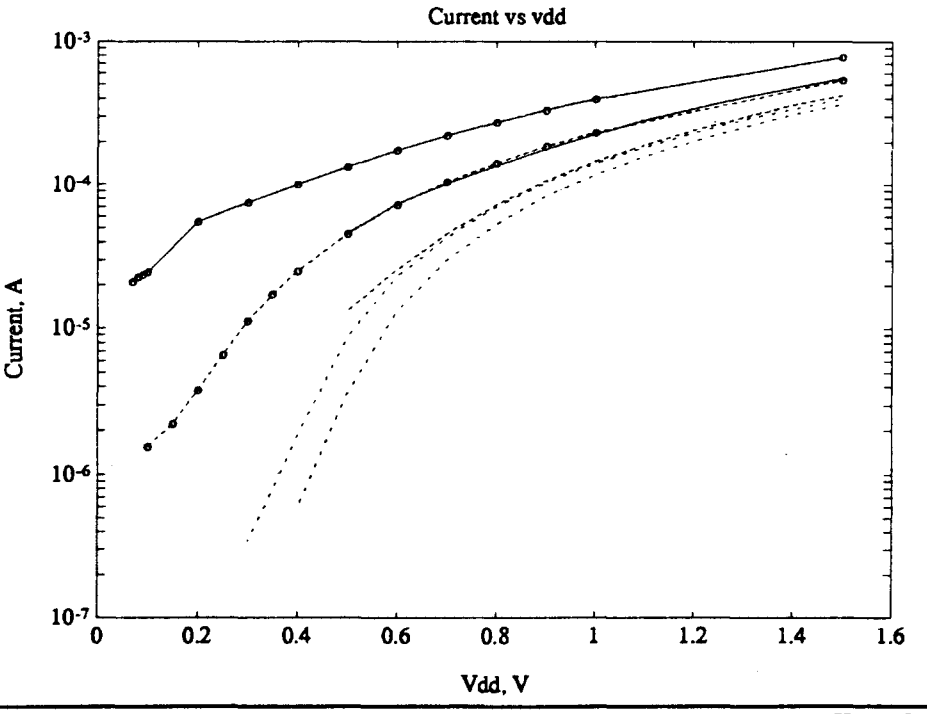
ULP CMOS-16

Low voltage performance



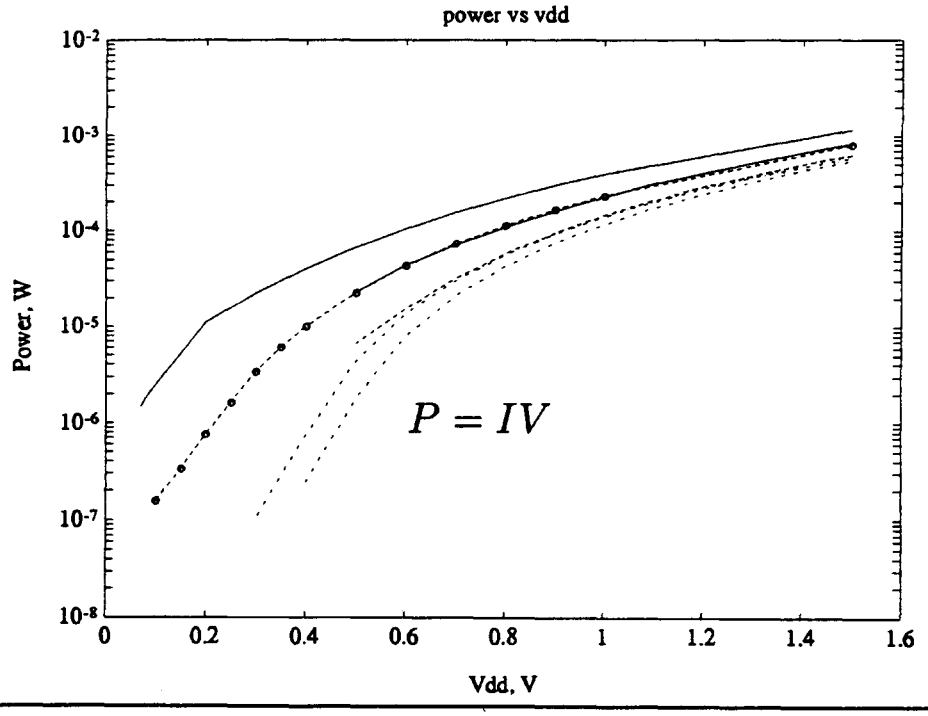
ULP CMOS-17

Chip current vs V_{dd}



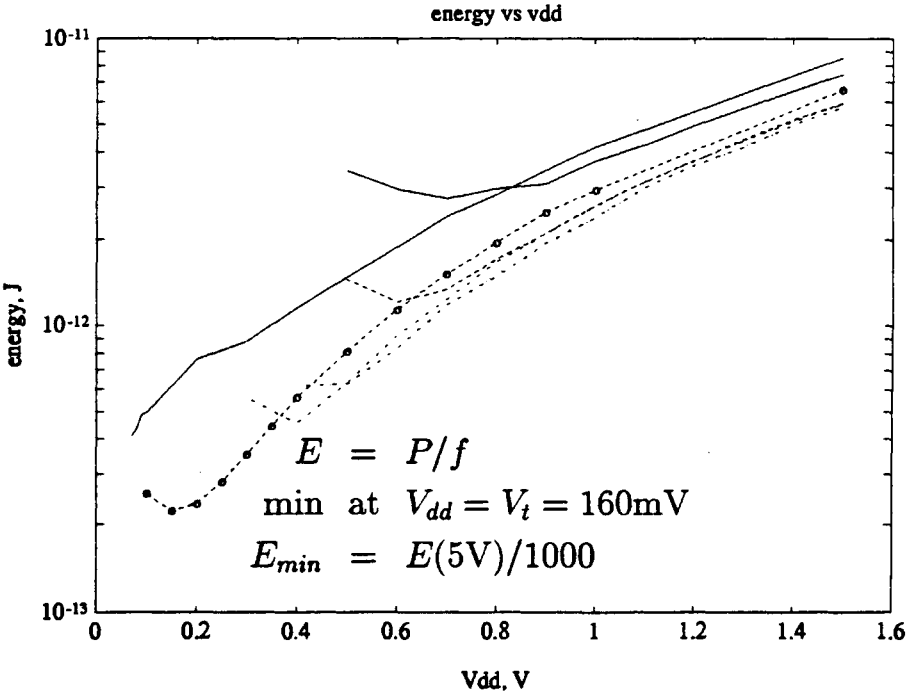
ULP CMOS-18

Chip power vs V_{dd}



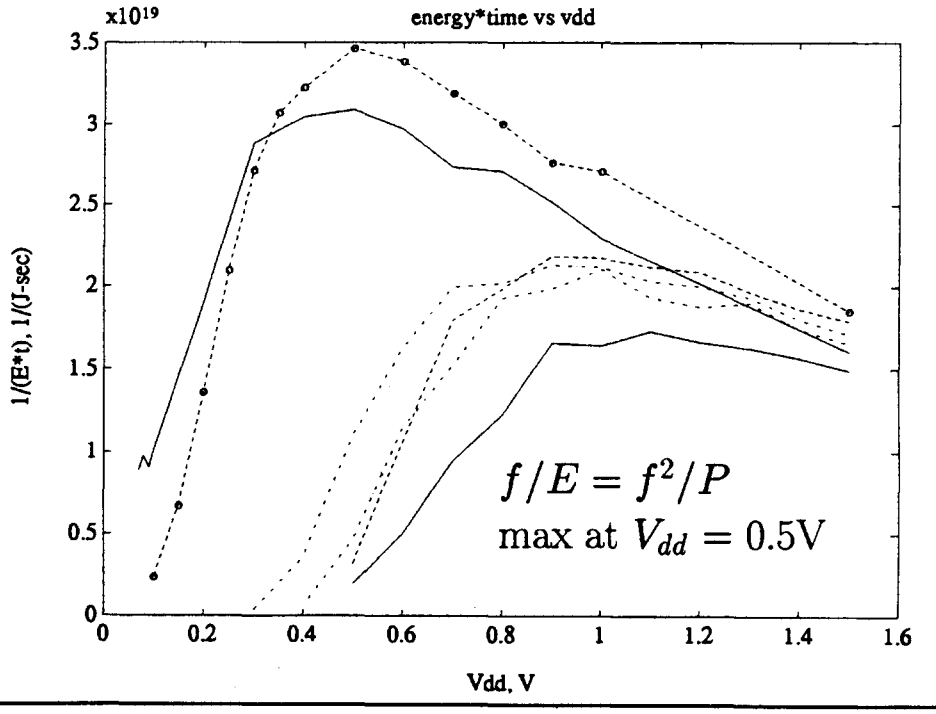
ULP CMOS-19

Ring oscillator minimum energy



ULP CMOS-20

Ring oscillator minimum energy×time



Challenges

- Controlling V_t
- Environment monitoring and control
- Noise margins and isolation
- Power supply design: 1W = 10A at 100mV
- Soft errors
- Interface circuits
- Critical subsystems: SRAMs, register files
- Test equipment infrastructure

Conclusions

- Modifying the process to accommodate low, tunable thresholds can improve the energy efficiency of CMOS circuits by 100×.
- Need to relax leakage from 1pA/μm to 1-10 nA/μm.
- Electrically tunable thresholds are key to accommodating a wide range of applications and activity levels in the system.
- Key concept: Minimum energy balances the leakage power of inactive circuits with the switching power of the circuits doing the work.