

AMULET1 - An Asynchronous ARM Processor

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Motivation and background

- Low power applications are becoming more important
- Fast synchronous chips use a lot of power
- Asynchronous units dissipate only when doing useful work

Therefore..

- Investigate the benefits of asynchronous logic by developing an asynchronous ARM chip
- Funded by ESPRIT in the OMI-MAP project

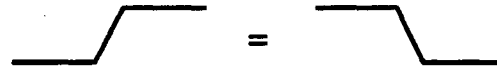
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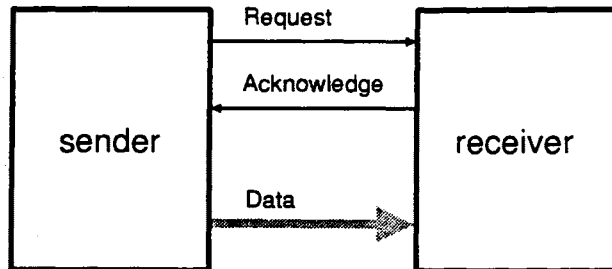
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Micropipelines

Transition signalling:

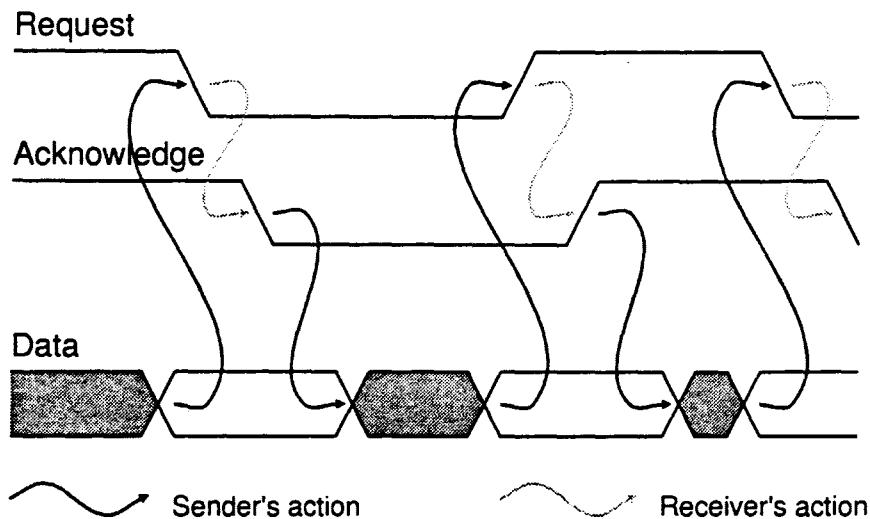


Bundled data:

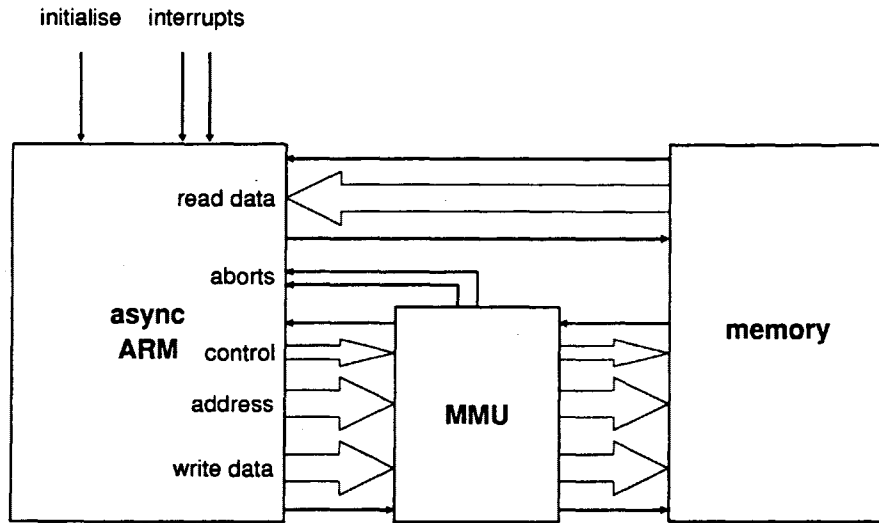


(I E Sutherland, Comm ACM, June 1989)

2-phase bundled data protocol



Top-level processor interface

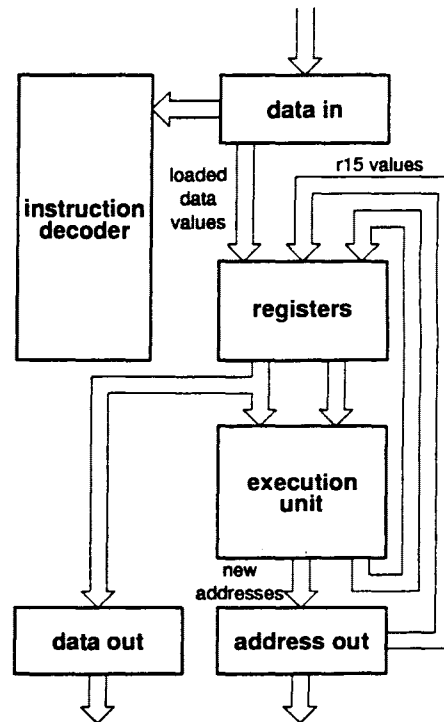


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CPU organization

- independent units
- operate concurrently
- synchronize only to exchange data

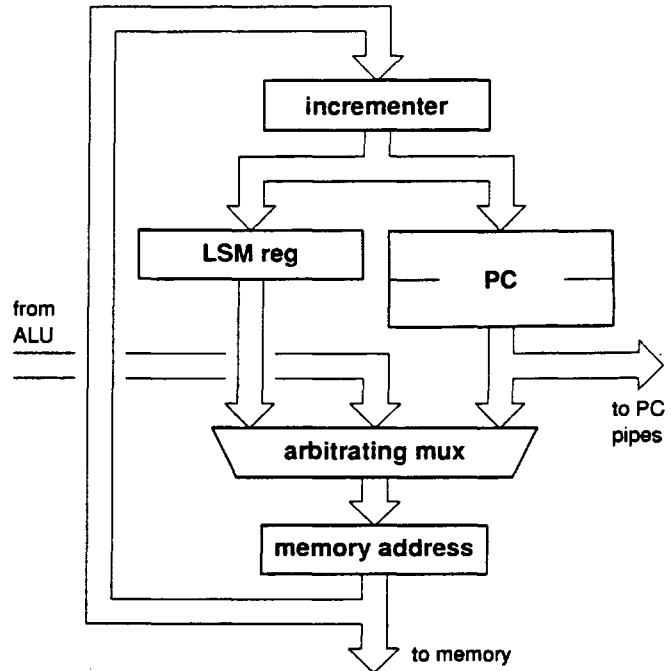


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Address unit

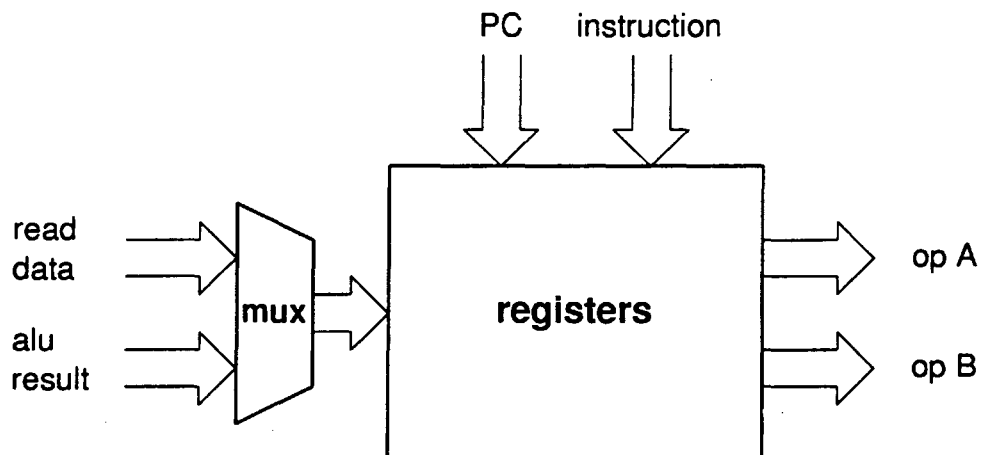
- ❑ autonomous incrementing PC loop
- ❑ ALU breaks into loop
- ❑ load/store multiple also uses loop



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Register bank



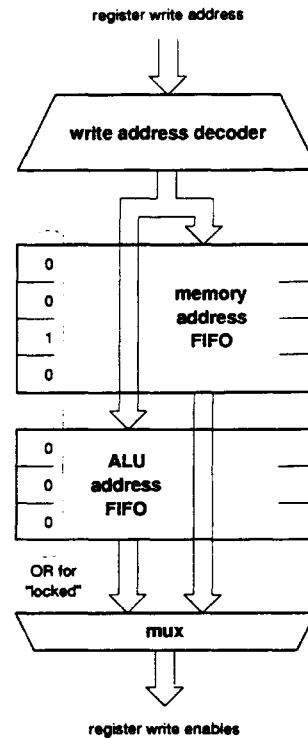
7.1.4

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Locking mechanism

- FIFO stores decoded write addresses
- a '1' in a column signifies a pending write to a register
- logical OR of a column is used to lock register
- separate internal and external FIFOs remove some memory waits

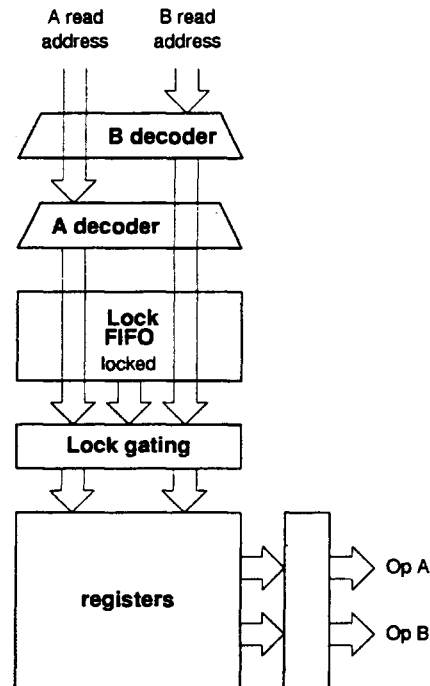


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Read operation

- lock signal is gated with read word line
- read is stalled until lock clears
- self-timed data availability signal waits for read data

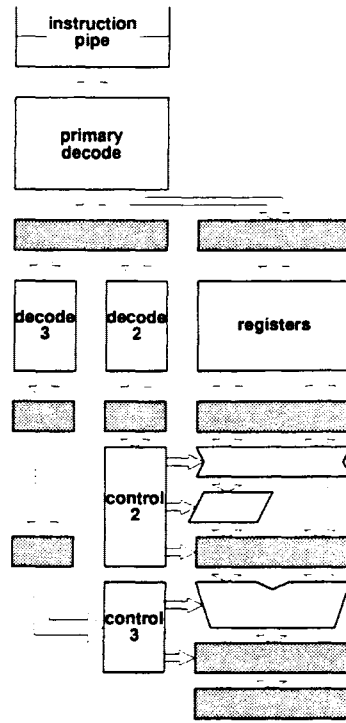


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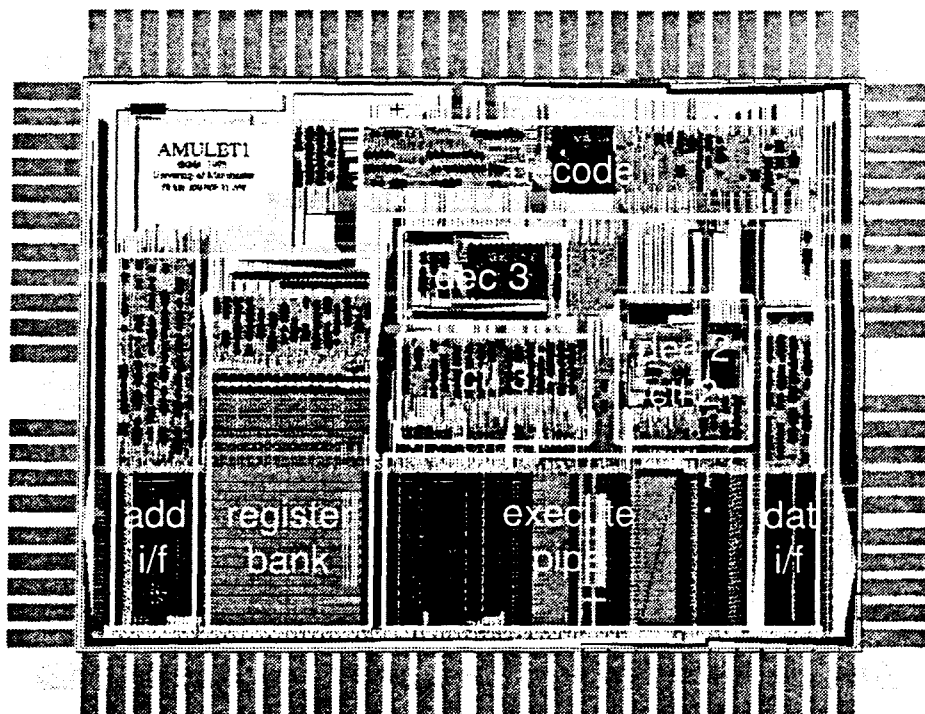
Execute pipe control

- ❑ parallel data and control pipelines
- ❑ synchronize only where they converge
- ❑ pipelines matched for optimum throughput



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Results

Compared with the synchronous ARM6 on the same technology:

- chip area 2x, mainly due to more sophisticated organization
- similar performance, with very conservative engineering
- similar power consumption
- similar design effort

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Conclusions

- Complex asynchronous designs are feasible - this design supports exact exceptions and backwards instruction set compatibility.
- The area cost of 'bundled data' asynchronous designs is probably around 10-20% over clocked styles. (Other asynchronous styles have an overhead of up to 100%.)
- The performance/power advantage still has to be demonstrated, though we are within a factor of 2.

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