System Design Verification of the HP Model 735 VLSI

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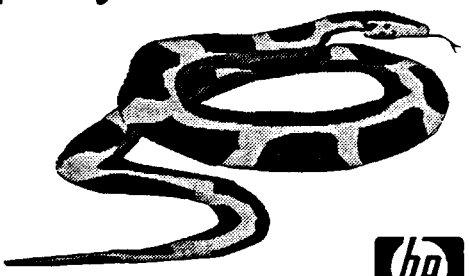

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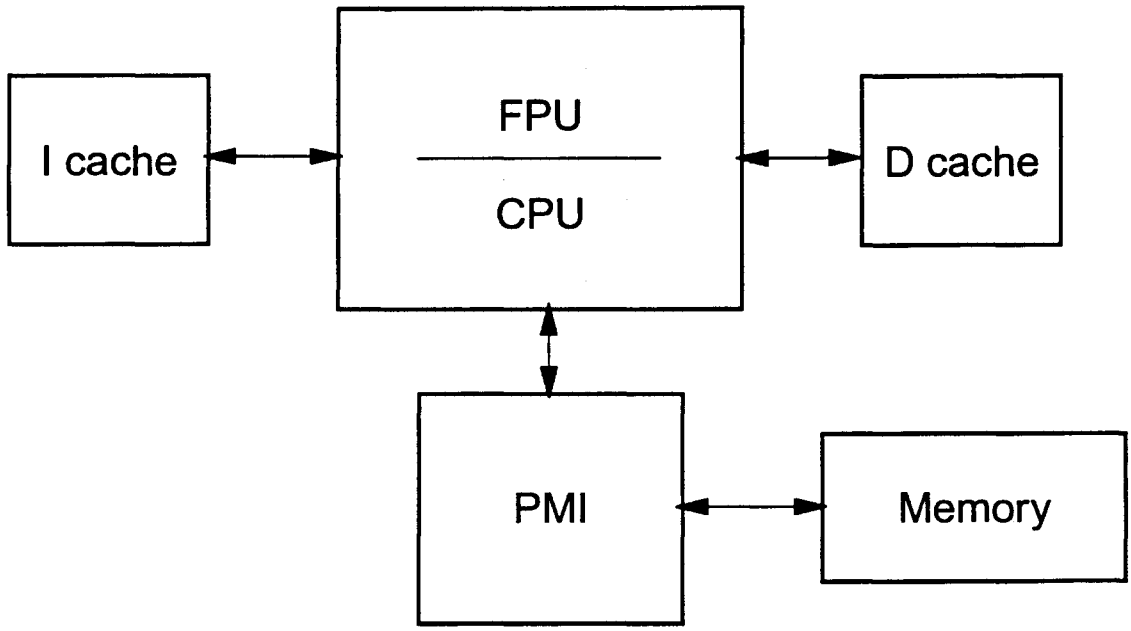
Presentation Outline

- System Verification of Processor Core
- System Verification of I/O Subsystem
- Bus-oriented Verification of I/O Subsystem
- Conclusions

735 Processor Core



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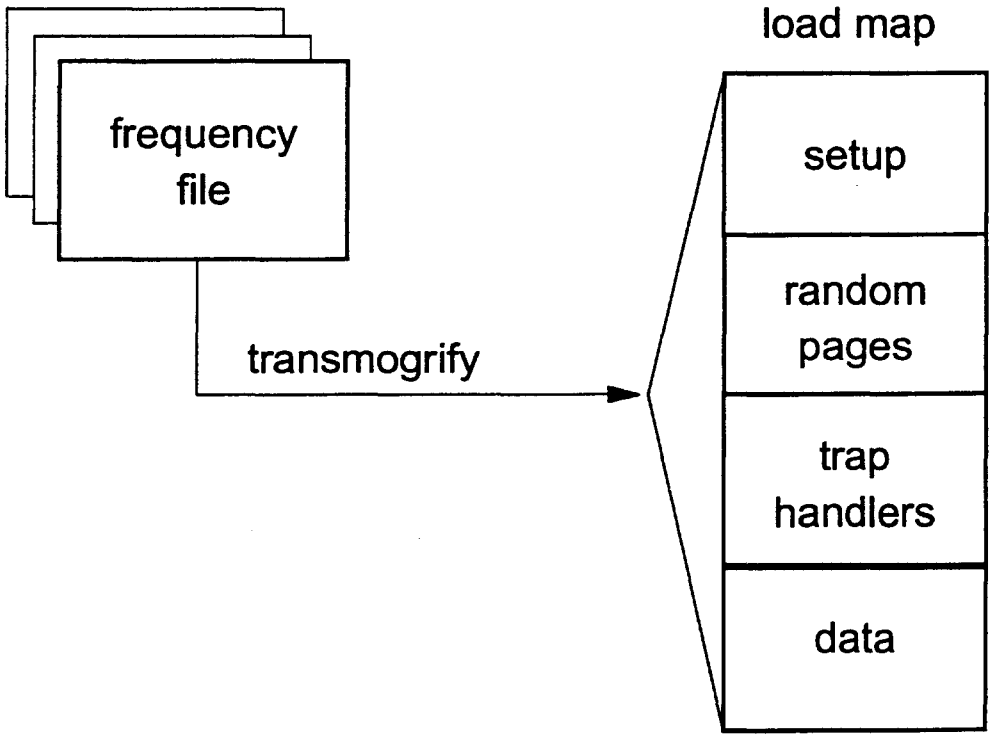
BPS Program Structure



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Frequency Files

- weighted, parameterized sequence of instructions
- parameters include immediate values, registers, completers
- typically targeted at specific functionality

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Frequency File Example

```
icount 1024
#
200.fmpyadd,DBL {rm1=0 4~7 rm2=0 4~7 tm=4~7
ta=11}
100.fadd,SGL {fr1=0 18~21R fr2=0 18~21R ft=18~21R
100.fstds {s=1~3 r=0 10~30 d=-16 -8 0 8 fr=4~7
11}
100.add {r1=0 10~30 r2=0 10~30 t=0 10~30}
```

BPS System Utilities

- system initialization
- trap handlers
- memory management
- floating-point retry
- seeded error cleanup
- temporary bug workarounds

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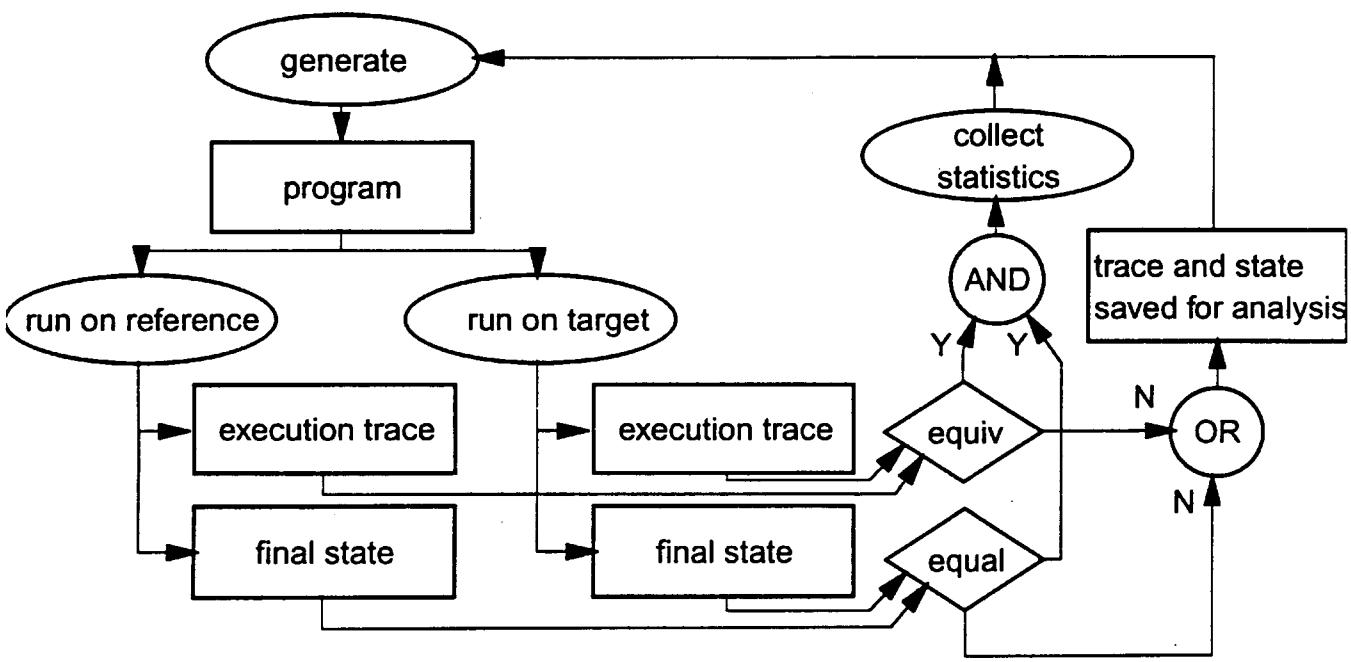
Micro Process Flow



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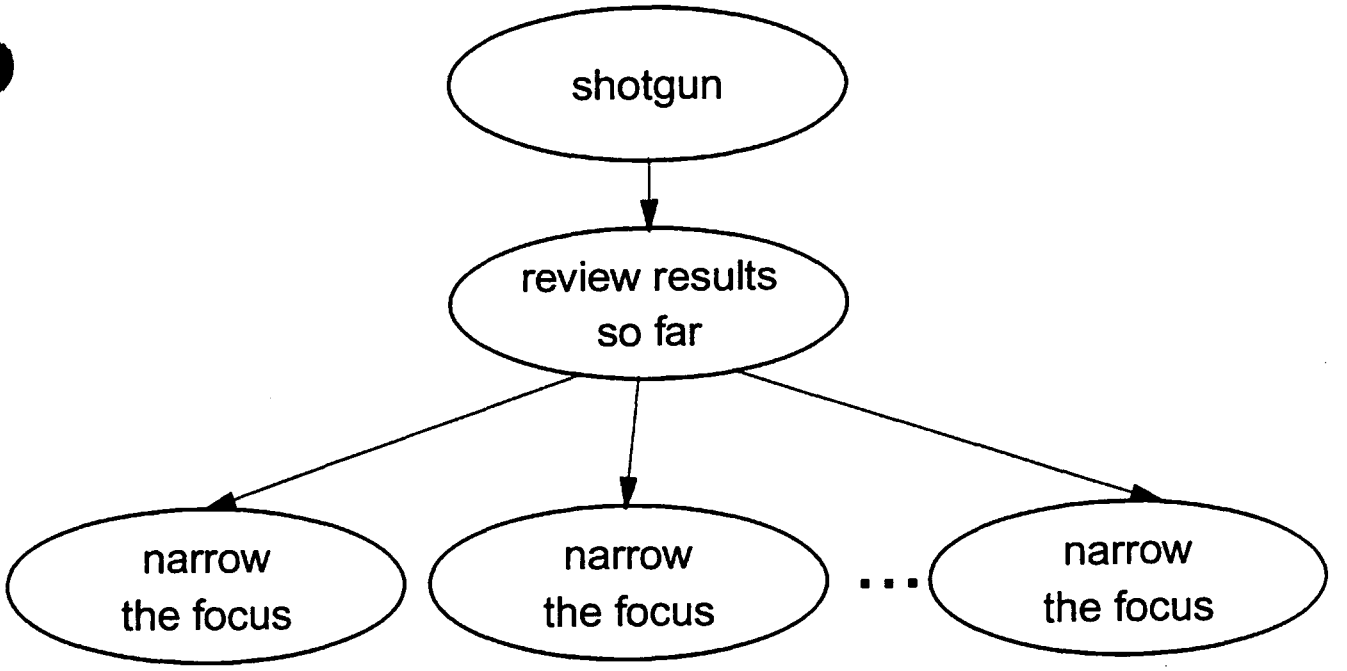
Macro Process Flow



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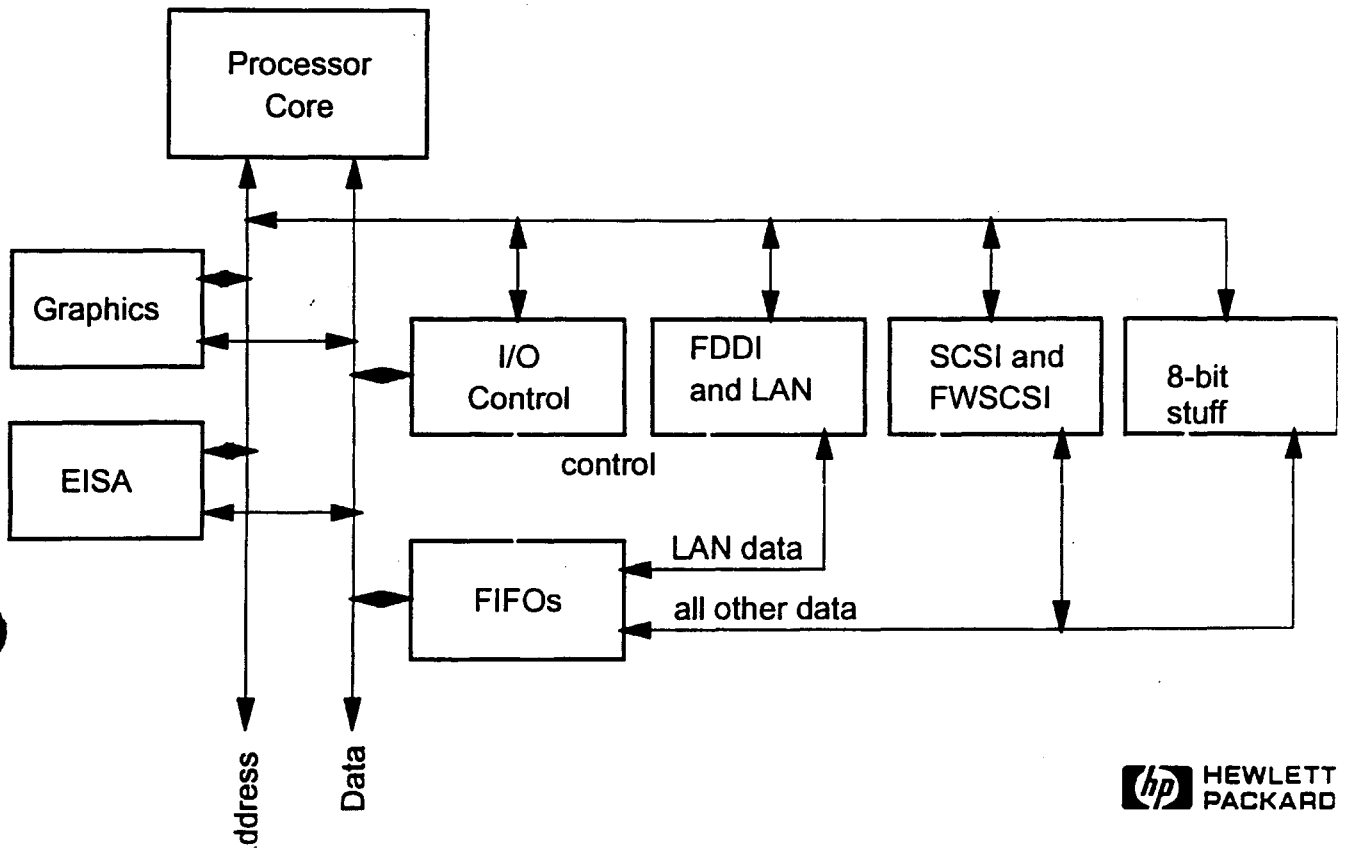
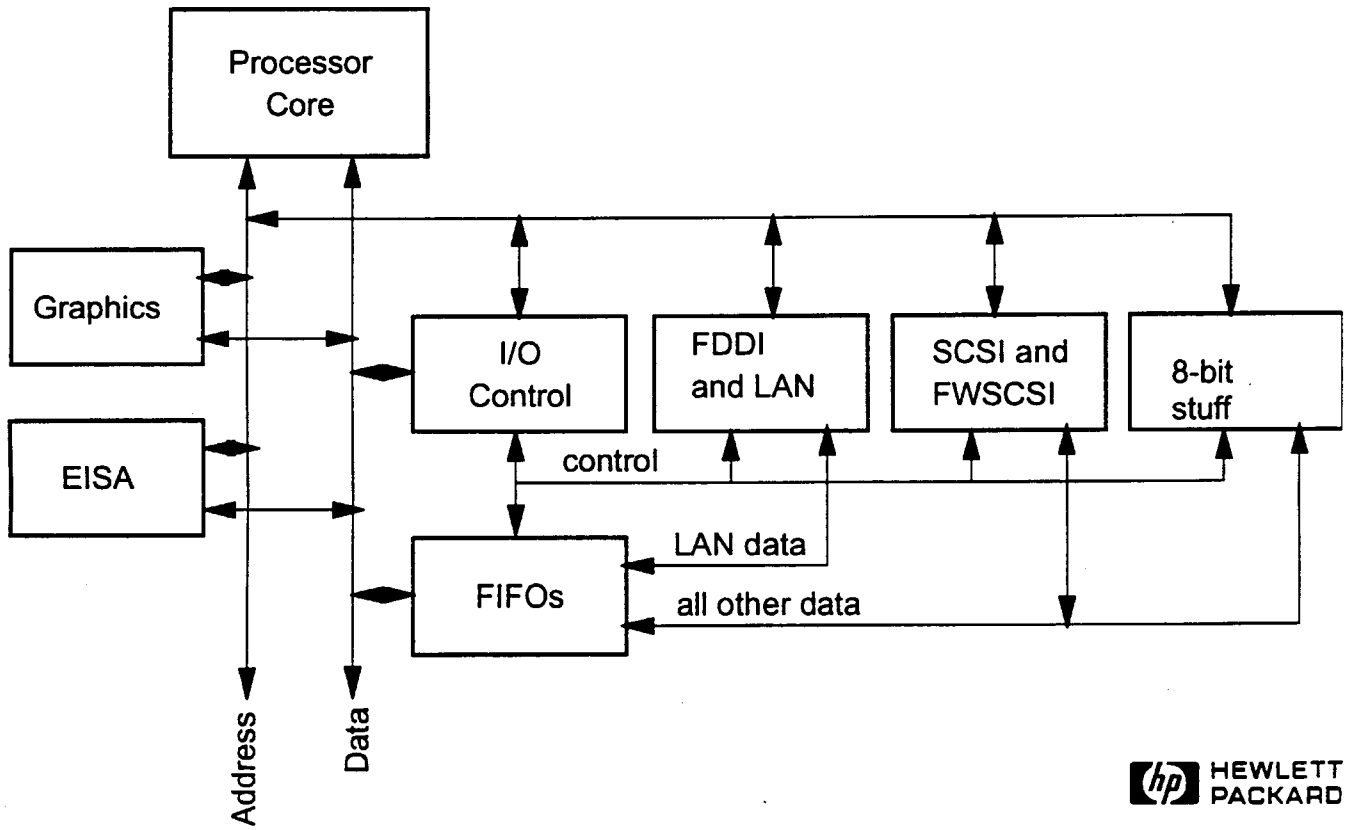
735 Processor and I/O Subsystem



735 Processor and I/O Subsystem



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I/O "Roundtrip"

Outbound

Init	Setup	Launch	Wait	Interrupt

Setup	Launch	Wait	Interrupt	Check

Inbound

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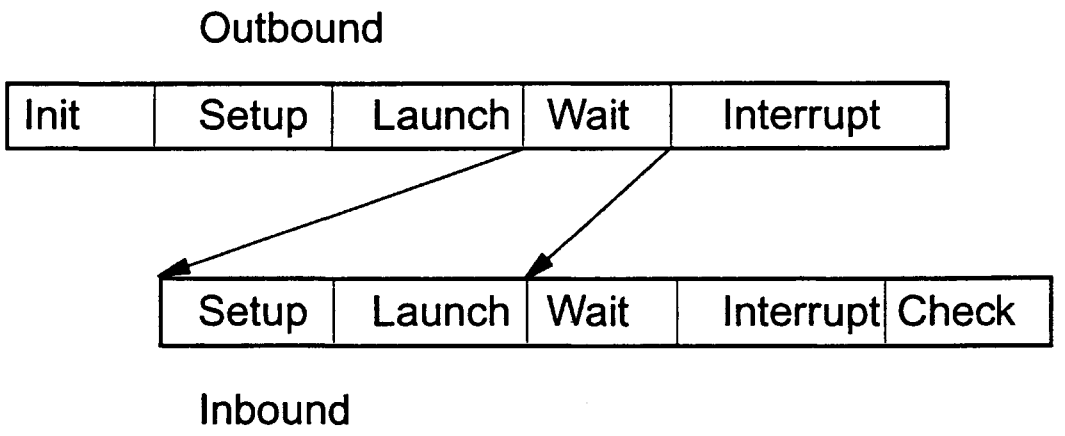
I/O "Roundtrip" Interleaving



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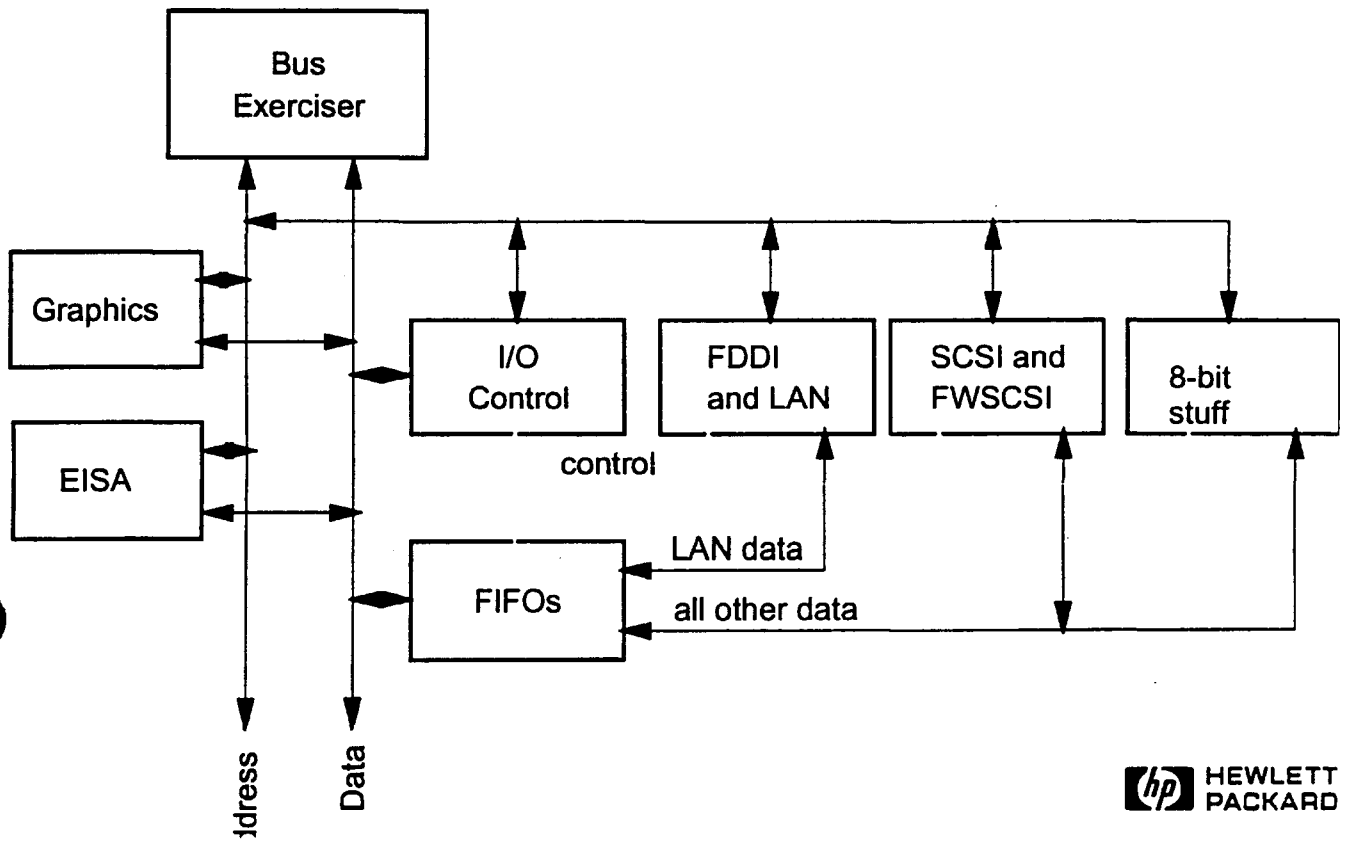
Reduced I/O Subsystem



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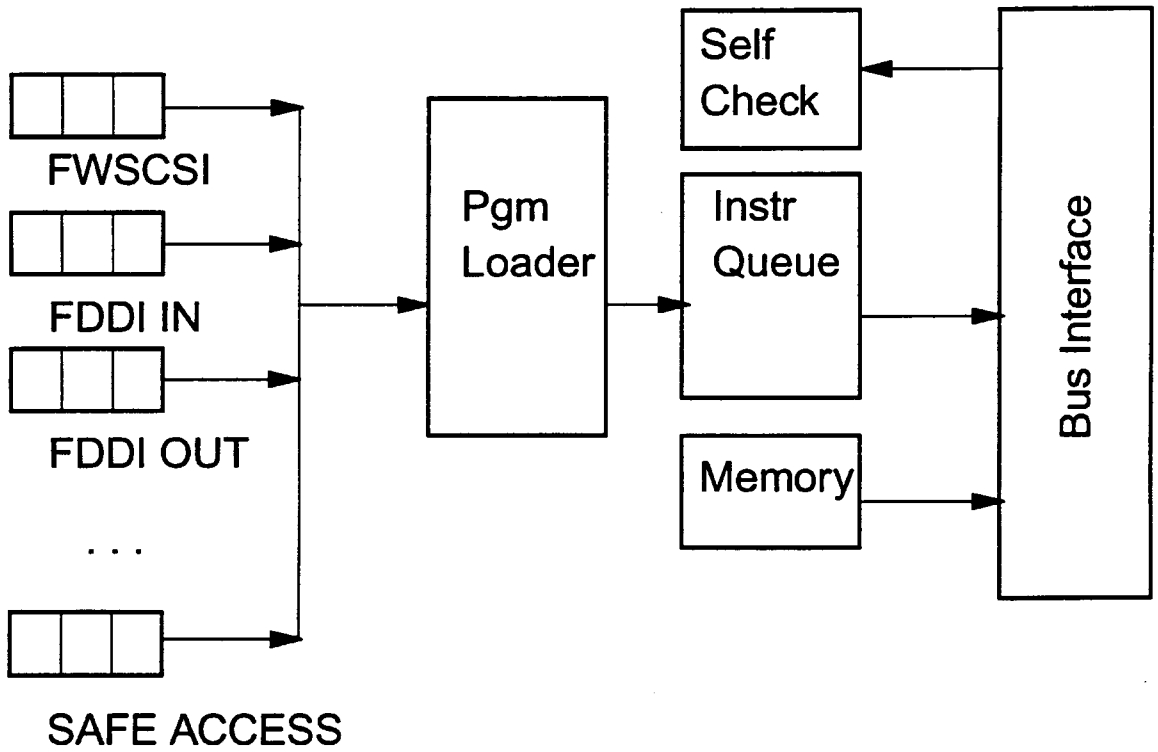
The Bus Exerciser



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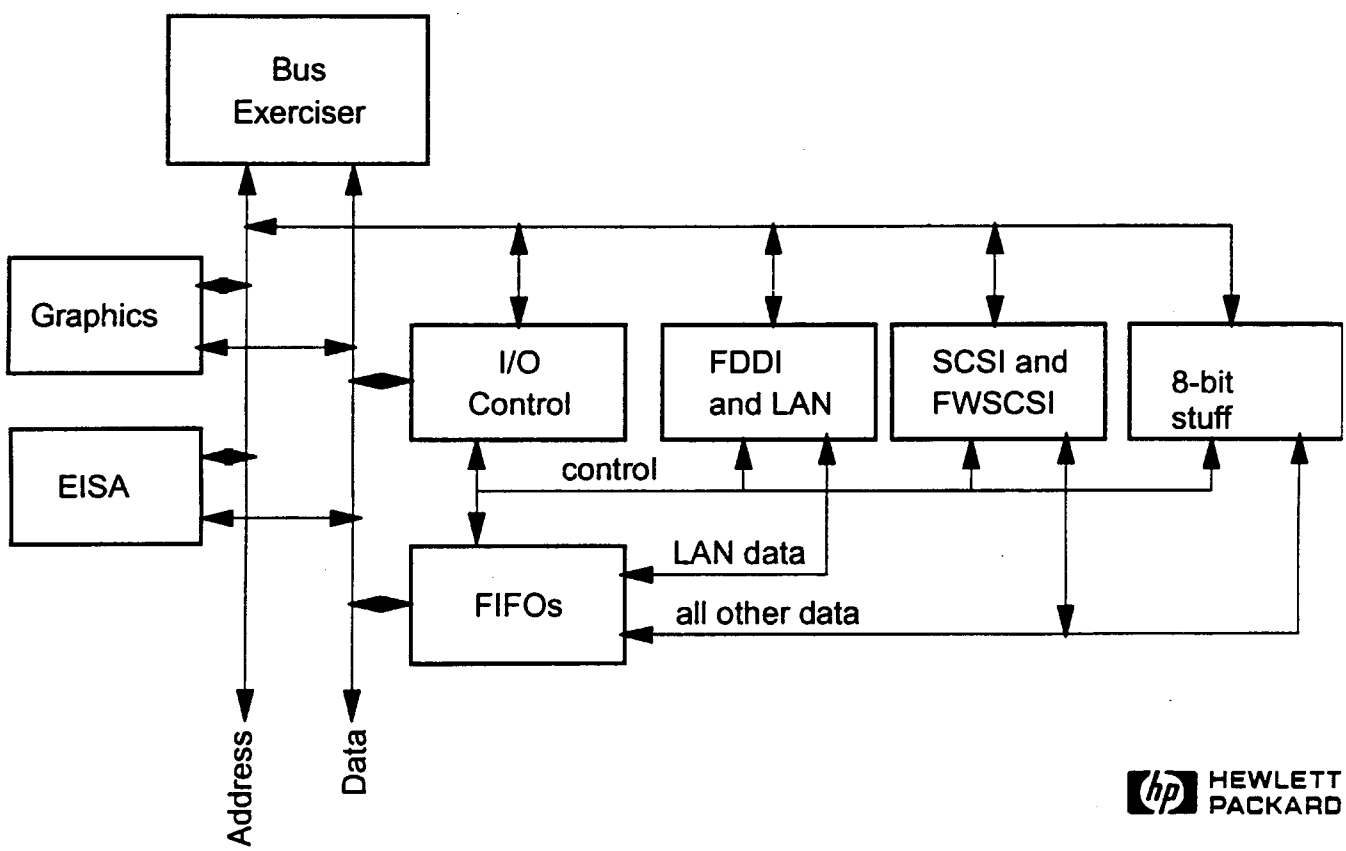
Reduced I/O Subsystem



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Case Analysis and Metrics

- arbitration coverage
- parallelism on 5 internal buses
- protocol monitoring

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Results

- about 2 seconds of simulated real-time operation with BPS on CPU (~200,000,000 processor cycles)
- about 3 seconds of simulated real-time operation with bus exerciser on I/O subsystem
- arbitration coverage
- first silicon on all parts booted operating system
- first silicon on I/O controller chips shipped in product
- all bugs seen in bus exerciser model