A Family of MPEG Video Encoder and Decoder Chips

optimized for consumer applications

Martin Bolton

SGS-Thomson Microelectronics
Grenoble, France

Summary

• Design Strategy : Architecture, Hardware/Software Partitioning

• MPEG Video Overview

• The generic architecture

• MPEG1/H.261 decoders

• MPEG1 encoder

• MPEG2 decoder for TV applications

Design Strategy

- **Architecture**

  - goal is to minimize area and power consumption by:

    - keeping clock frequencies as low as possible
    - distributing control, only clocking operators when necessary
    - constraining programmability to the needs of a single application

- **Technology**

  - ASIC methodology: standard cells and application-specific macrocells

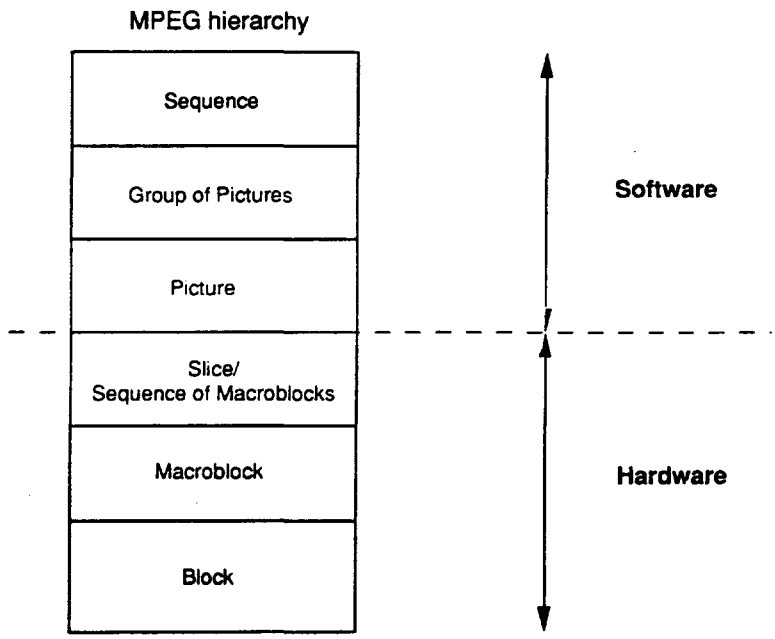
  - Synthesis used where advantageous

  - CMOS 0.7 micron technology, direct migration path to 0.5 micron/3.3V

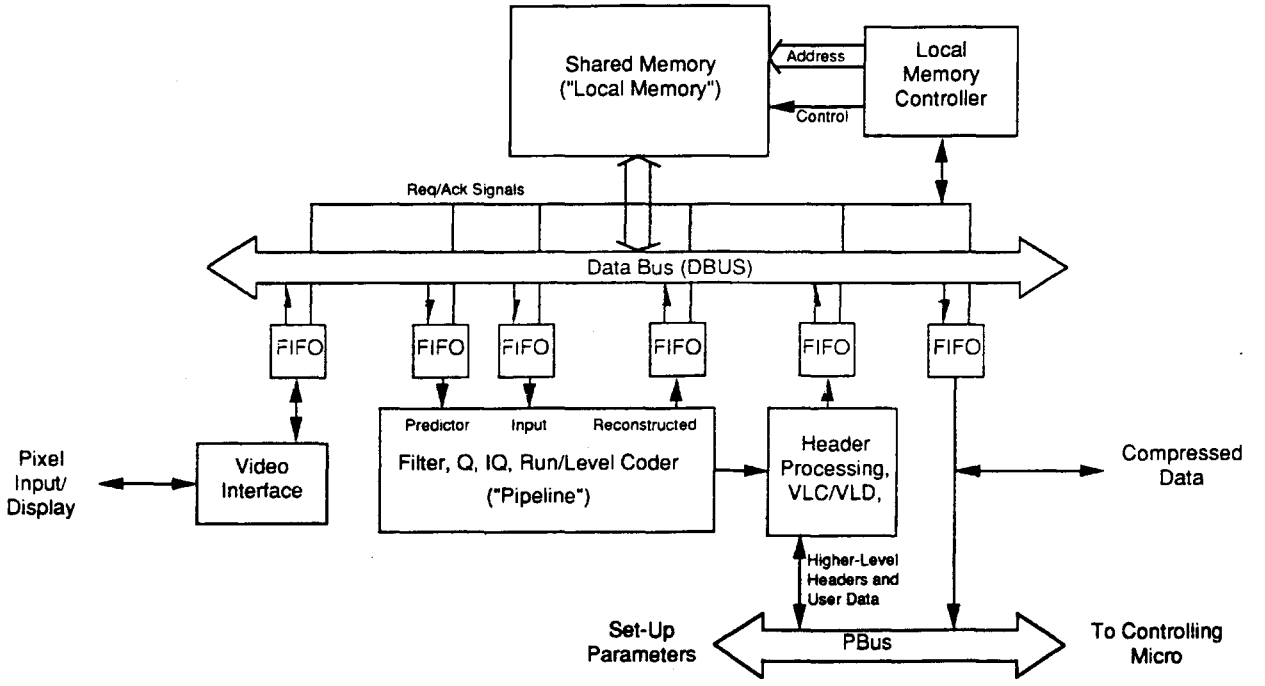
- **Hardware/Software Partitioning Criteria**

- on chip:	high compution rate (high-rate operations) limited flexibility (fixed by standard) real-time constraints
- in standard microcontroller:	low compution power (low-rate operations) high fexibility (application-dependant) lower real-time constraints

Hardware/Software Partitioning



Generic Architecture



MPEG/H.261 Video Decoders

Main Features

- Real-time decoding for MPEG1 SIF and H.261 ("p X 64")

  SIF: 352 X 240 @ 29.97 Hz. 352 X 288 @ 30 Hz
  H.261 CIF: 352 X 288 @ 29.97 Hz

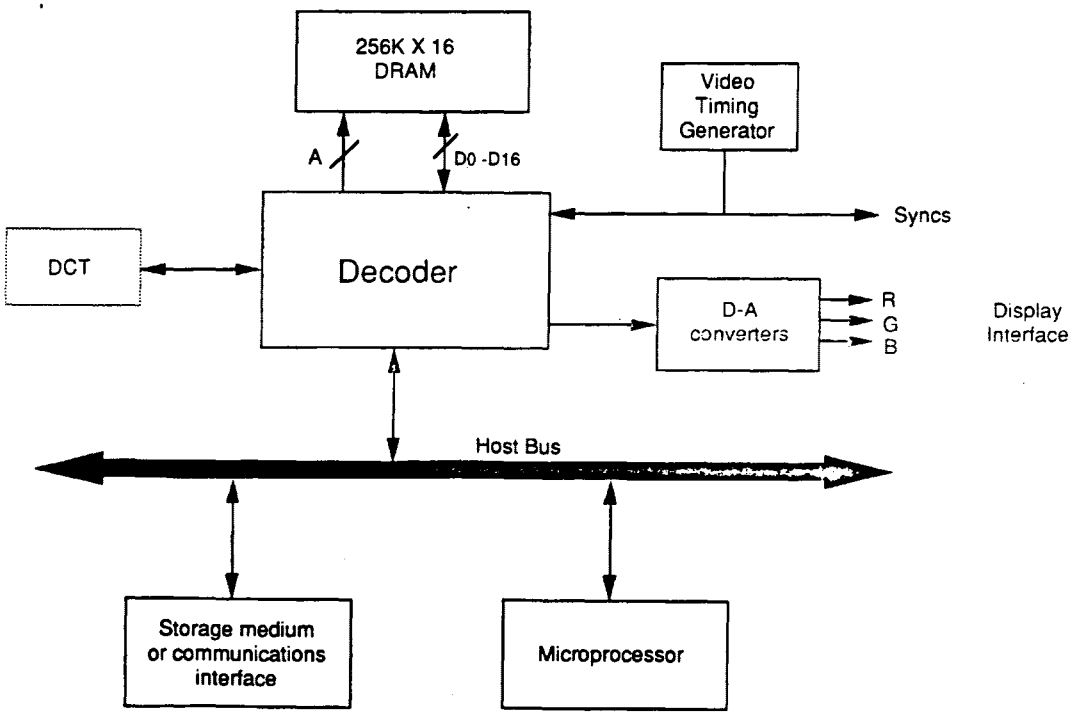
- Die size 72 sq mm (no DCT). 86 sq mm (with DCT)

- Power consumption 0.25 W, max ext clock freq 48/50 MHz, 144-pin PQFP package

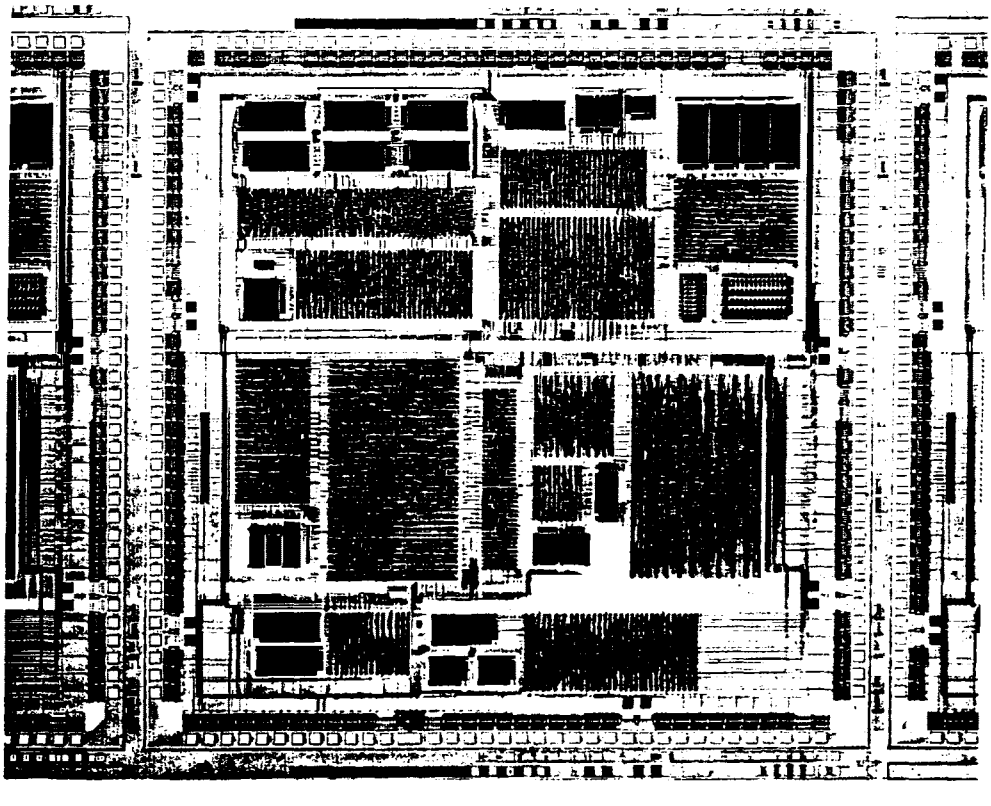
- Single external memory (DRAM) holds picture buffers and bit buffer

- Low demand on controlling micro (5% of standard 16-bit micro)

Decoder System Block Diagram



MPEG1 Decoder Die Photograph



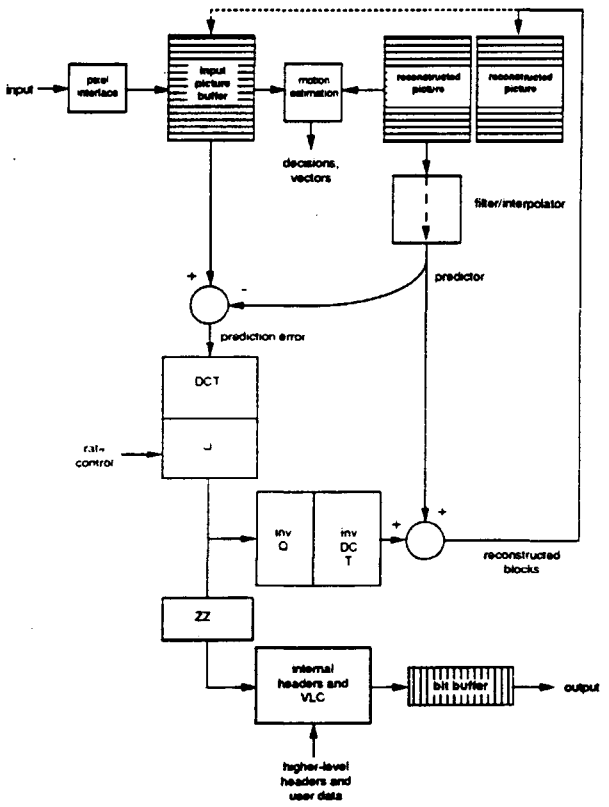
MPEG/H.261 Video Encoder

Main Features

- Real-time decoding for MPEG1 SIF and H.261 ("p X 64")

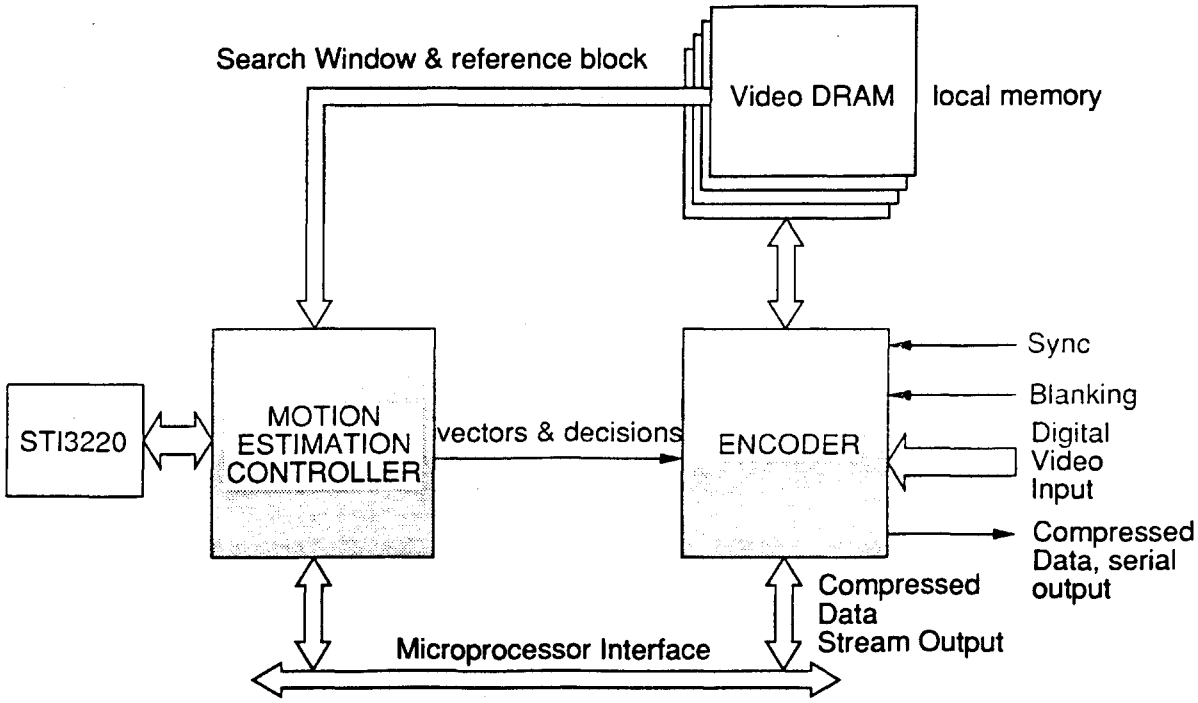
  SIF: 352 X 240 @ 29.97 Hz, 352 X 288 @ 30 Hz
  H.261 CIF: 352 X 288 @ 29.97 Hz

- Designed to support range of encoder applications, from minimum cost to highest quality
- "Two-pass" encoding possible
- Bit-rate control system gives many user options
- Single external memory (DRAM) holds picture buffers and bit buffer

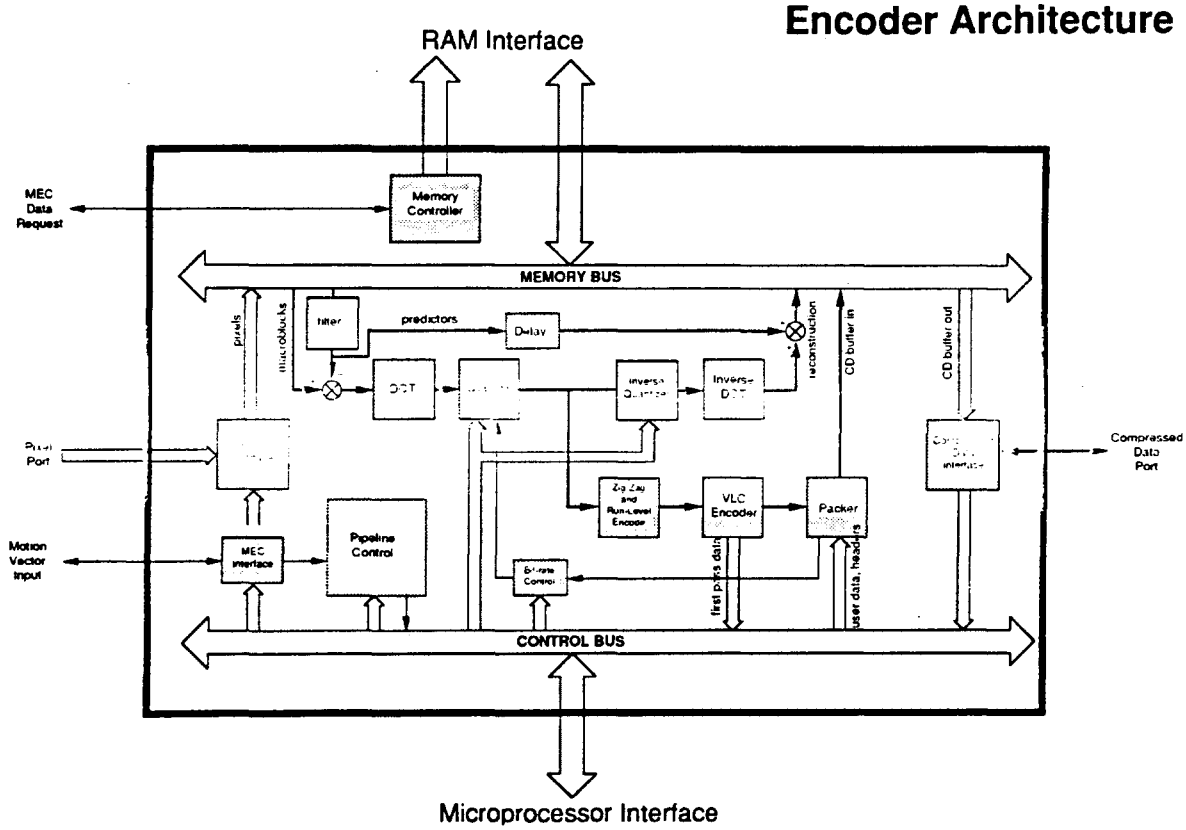


The Encoding Process

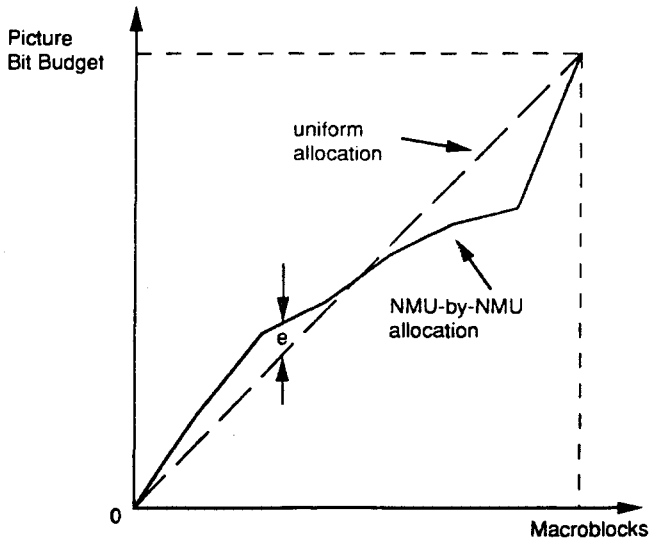
Encoder System Block Diagram



Encoder Architecture



Bit Rate Control Principle

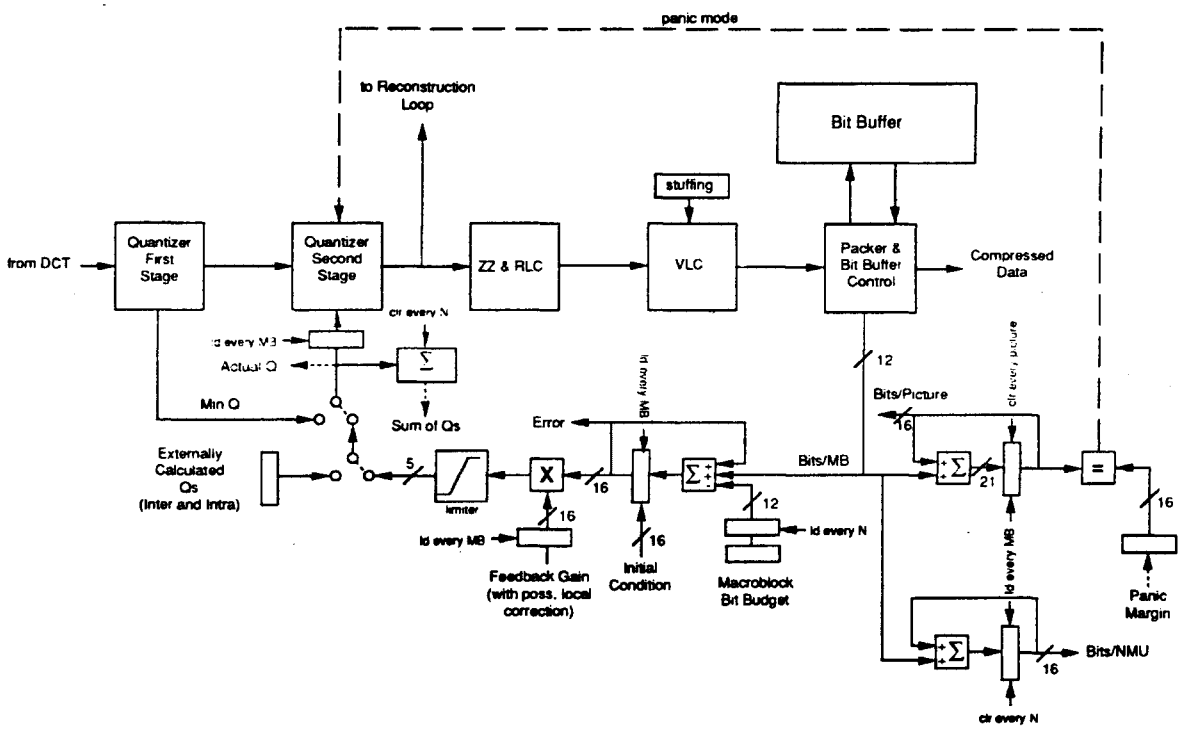


e = bit eror

NMU = N-macroblock unit

Quantizer = k X e

Bit-Rate Control Loop



MPEG2 Video Decoder

- Architecture is a scaled version of the MPEG1 decoder

  Memory bus extended from 16 bits to 64
  External clock 55 MHz

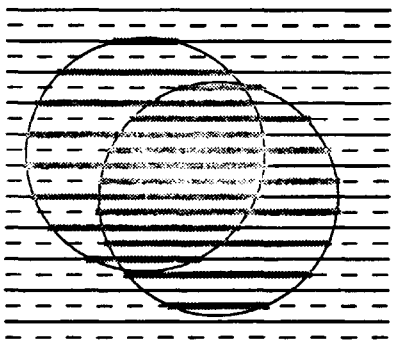
- Real-time decompression of CCIR 601 (720 X 480/576) interlaced pictures

- Power consumption < 1 W, 144-pin PQFP package

Additional Features

- Field- or frame-based prediction
- On-screen display
- Horizontal interpolation for format conversion
- Error concealment

MPEG2 Handles Interlaced Pictures



- Second field can be predicted from first

- A DCT performed on blocks from one field can often give fewer high frequency components than a DCT performed on blocks containing data from both fields.

——— field 1
– – – field 2

MPEG2 Decoder Die Photograph