A 200M Pixels/sec Graphics Accelerator with Multimedia Expansion

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Outline

1) **Design objective**
2) **Key features**
3) **Graphics system block diagram**
4) **Chip architecture**
5) **Performance**
6) **Methodology and Tools**
7) **Chip Features**
8) **Conclusion**

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Design Objectives

- State-of-the-art performance running industry leading 2-D GUI and CAD software
- Cost effective solution for high volume desktop computers
- Optimized for high color depths (16, 24, 32 bit-per-pixel)

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State-of-the-Art Performance

- 4, 8, 16, 24, 32 bit-per-pixel acceleration
- Advanced drawing engine:
  - Host-To-Screen BitBlt
  - Screen-to-Screen BitBlt
  - Line Draw
  - Quadrilateral Fill
  - Text
  - Clipping
- On-chip pattern RAM and full 256 Raster-Ops
- Up to 1600 x 1200 x 16, 1280 x 1024 x 24 resolutions

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High Integration

- Zero-glue connect to VESA Local and PCI buses
- Integrated on-chip SVGA
- 32-bit interleaved VRAM
- 1, 2, 4MB directly supported
- 128K x 8, 256K x 4, 8, 16 VRAMs
- 50MHz with -70 VRAMs (200 MB/sec)
- Shared frame buffer interface for multimedia coprocessor(s)
- 208 PQFP

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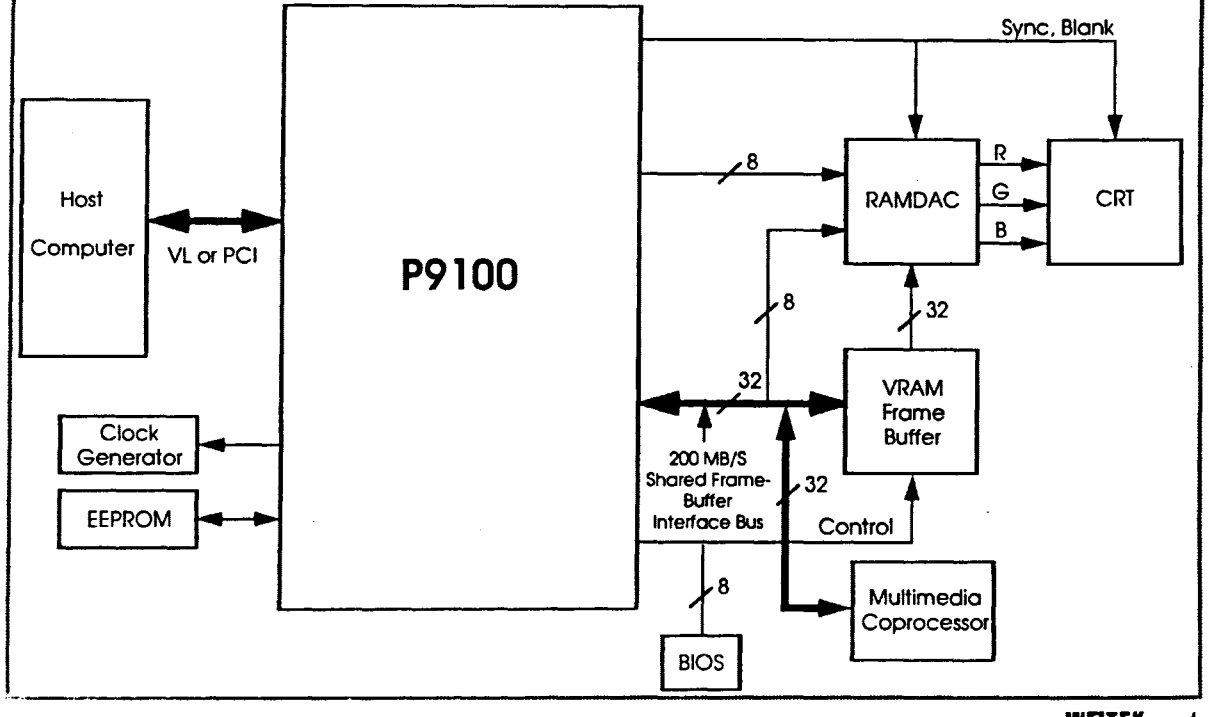
System Block Diagram



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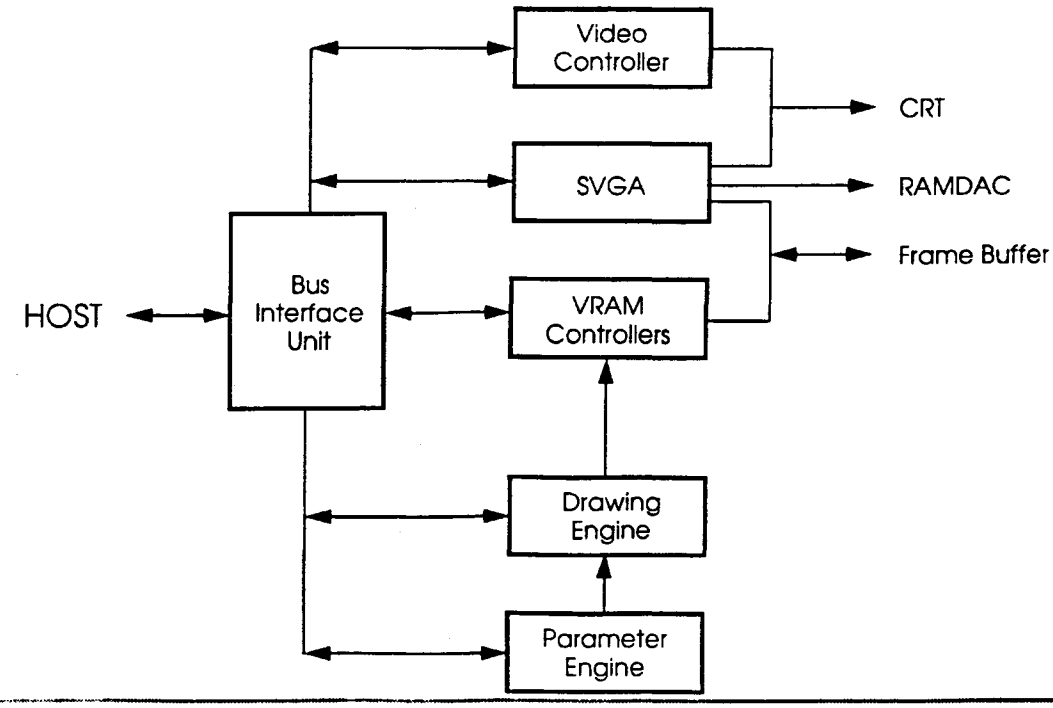
P9100 Block Diagram



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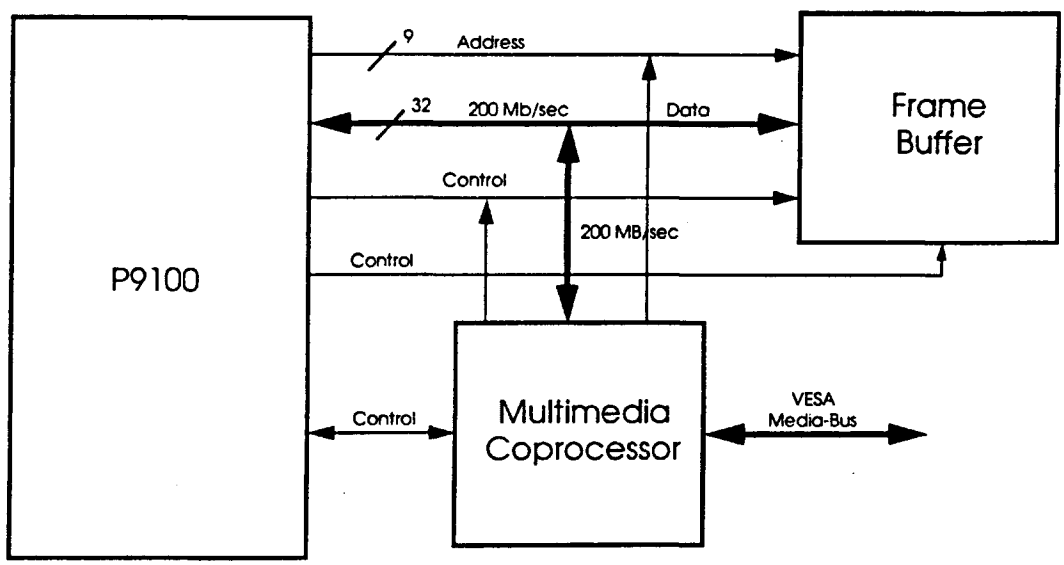
Multimedia Coprocessor Interface



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Performance

- Advanced pipelined architecture matches drawing engine performance with 32-bit interleaved VRAM bandwidth
- Host interface matched to peak CPU speed
- On-chip 200 MHz clock edges for fine-grained RAM control allows one-cycle writes and two-cycle reads

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Performance

(8 bit-per-pixel)

• Screen-to-screen BitBlt	50 MPixels/sec
• Quadrilateral Fill - Peak	200 MPixels/sec
- 10x10 pixels	1.0 MQuads/sec
• 10-pixels lines random orientation	2.0 Mlines/sec
• Host-to-screen BitBlt	50 MPixels/sec
• Text (9 x 11 characters)	877 Kchar/sec

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Methodology and Tools

- Full-custom design for data-paths
- Behavioral model written and simulated using in-house tools
- Control logic synthesized with Synopsys
- In-house tools for timing verification and control logic layout
- Cadence tools for global routing and layout verification

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Chip Features

• Technology	0.8μm CMOS
• Chip Size	11.3mm x 11.3mm
• No. of Transistors	350K
• Pin Count	208 (164 signal pins, 44 power and ground pins)
• Power Dissipation	2.0W Max at 50 MHz

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Conclusion

- State-of-the-art 2-D graphics accelerator
- Optimized for full 8-, 16-, 24-, and 32-bit acceleration
- Accelerates memory and screen BitBlt, text, line and quadrilateral fills
- Fully VL and PCI compliant
- Operates at the full VRAM bandwidth of 200M bytes/sec
- Interface to multimedia coprocessor

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