A Compact 3D Graphics Chip Set

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Outline

Design goals, objects, target markets/applications

3D graphics architectural approaches

Leo (ZX) system overview

The individual Leo chips: LC, LF, LD, LX

Design environment

Performance

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Leo Deign Goals

- **Complete single board subsystem solution for complex 3D graphics applications: mechanical CAD, bioCAD, scientific visualization, animation, entertainment, and virtual reality**
- **Acceleration of 3D Z-buffered rendering primitives: shaded triangles, antialiased vectors and dots, depth cueing**
- **Acceleration for X11 Windowing operations**
- **1280×1024 76Hz display, double buffered 24-bit color with 24-bit Z-buffer, 8-bit overlay**
- **Full stereo video support**

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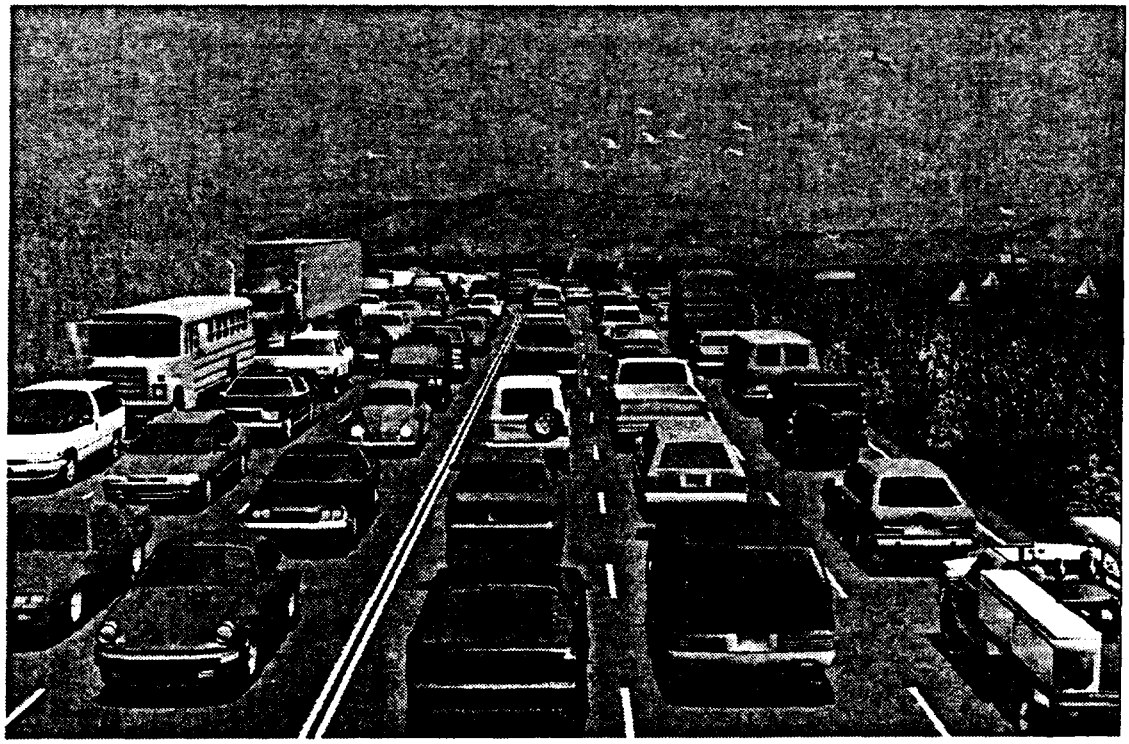
Example rendering: "Traffic Jam to Point Reyes"



Objects courtesy of Viewpoint Animation Engineering

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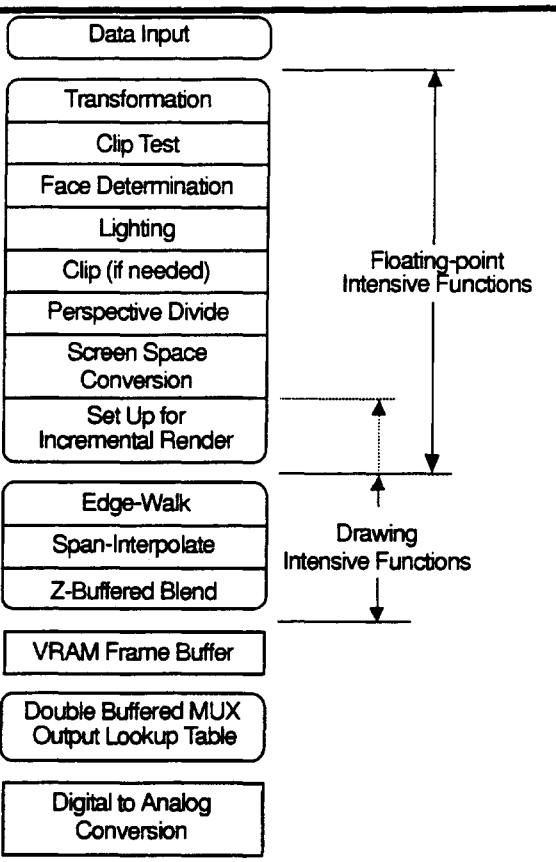
Generic graphics pipeline



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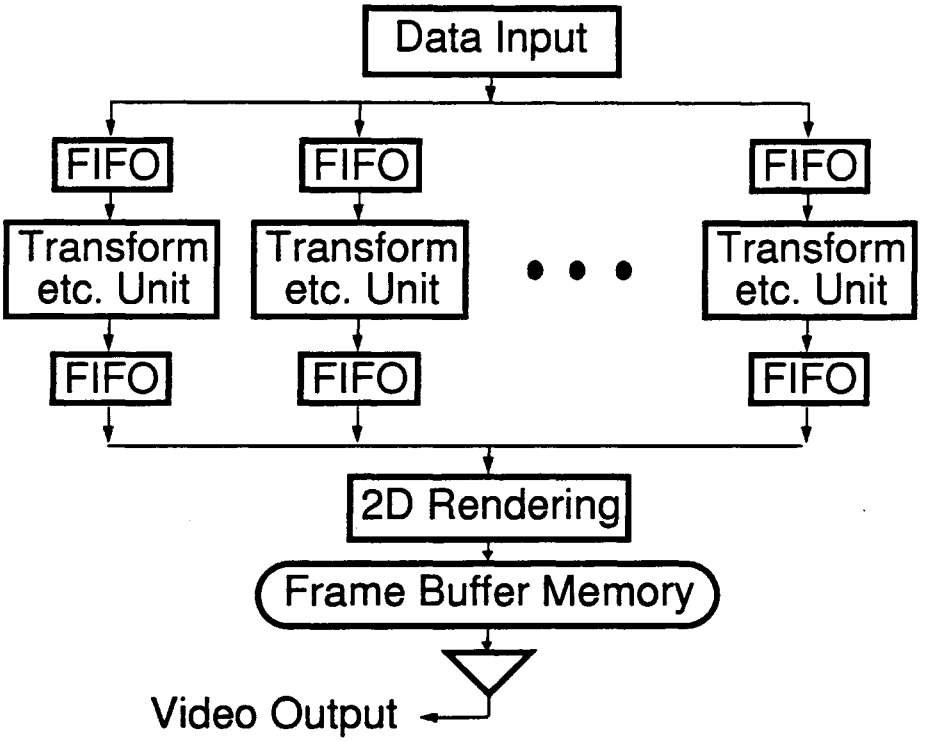
Generic parallel graphics pipeline implementation



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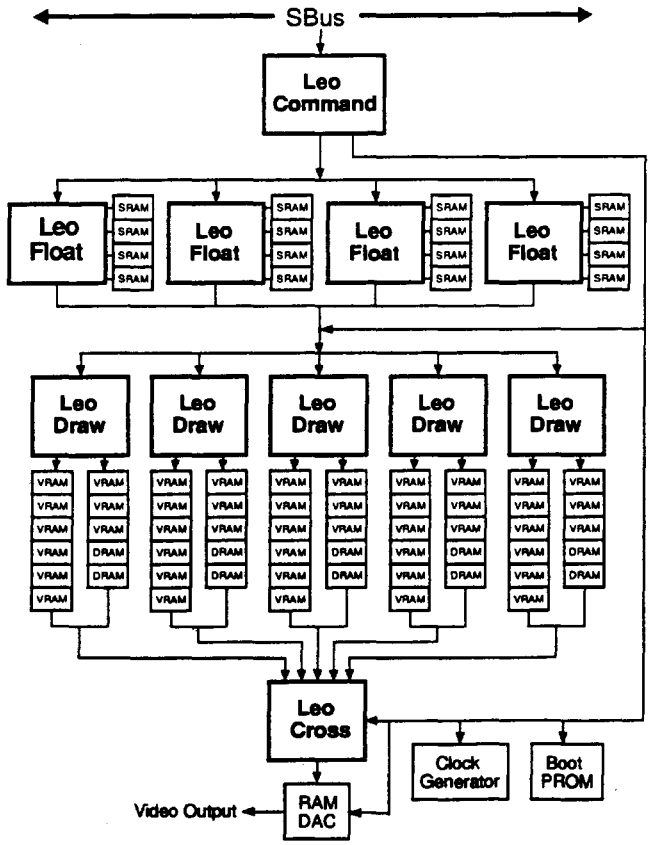
Leo Block/ Chip Diagram



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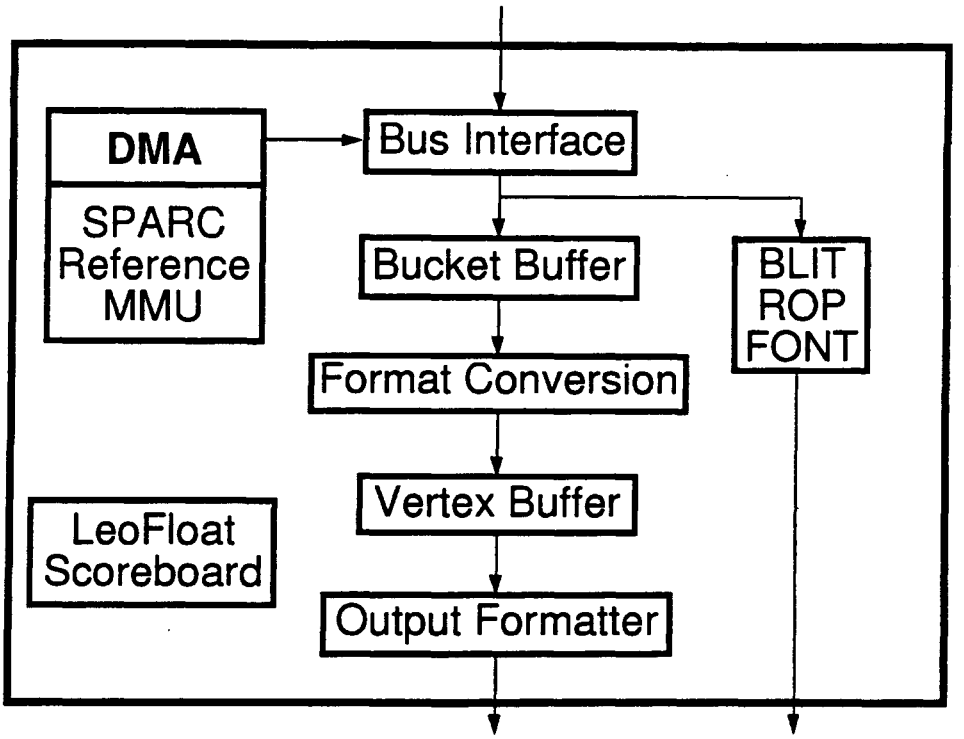
LeoCmd Block Diagram



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LeoCmd Feature List

- **SBus DMA master**
- **SBus memory device**
- **Numerical format conversion of input data**
- **Converts chained graphics primitives to isolated graphics primitives**
- **Parallel X11 2D graphics port: BLIT, ROP, FONT**
- **Subsystem controller, scoreboards LeoFloat Array**

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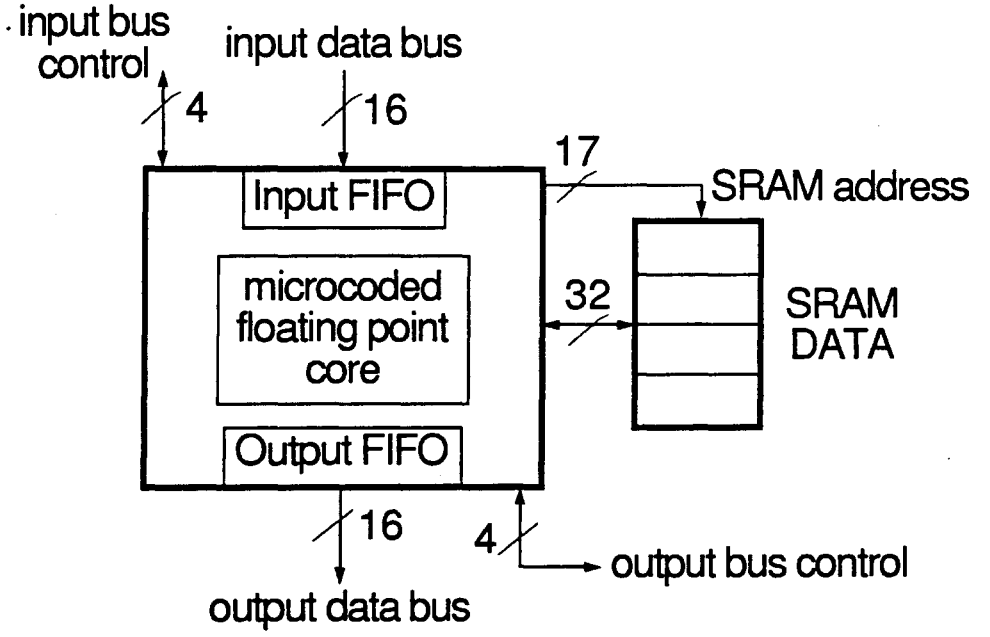
LeoFloat



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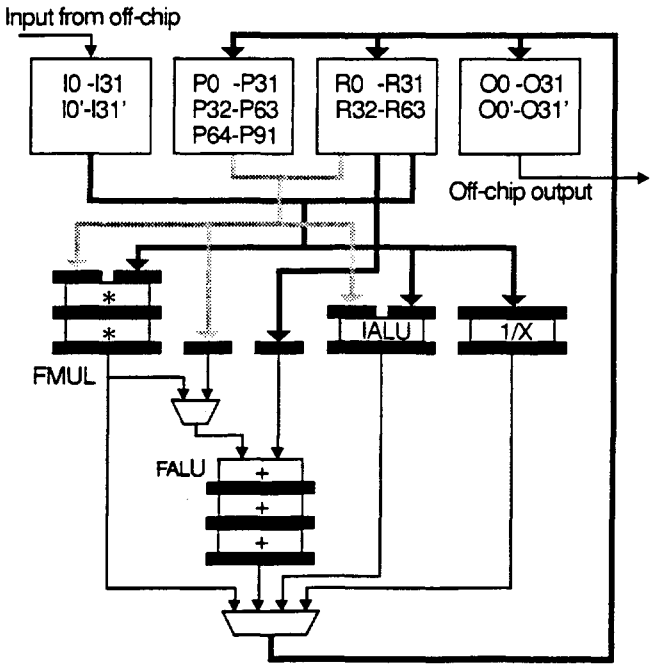
LeoFloat Function Units, Register Files, and Data Paths



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LeoFloat Execution

Inst Fetch	Inst Decode /branch	Register Fetch	ALU Functions (1-11 clks)	Register Store

Execute Pipeline

majorOP (4-bits)	Dbus (7-bits)	D S	A S	C-bus (6-bits)	B-bus (6-bits)	A-bus (7-bits)

Typical micro instruction word fields

d = a*b+c;

Micro assembler syntax

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LeoFloat Features

- **Double Buffered I/O register files**
- **288 Internal Registers**
- **Parallel IEEE FMul, FALU, 1/X, IALU**
- **Special 3D clip test instructions**
- **Dozens of specialized Condition code bits**
- **Dozens of specialized branch instructions**
- **Y-sort register instructions re-orders R registers**
- **Software pipeline scheduling**
- **128K 32-bit word external microcode SRAM**

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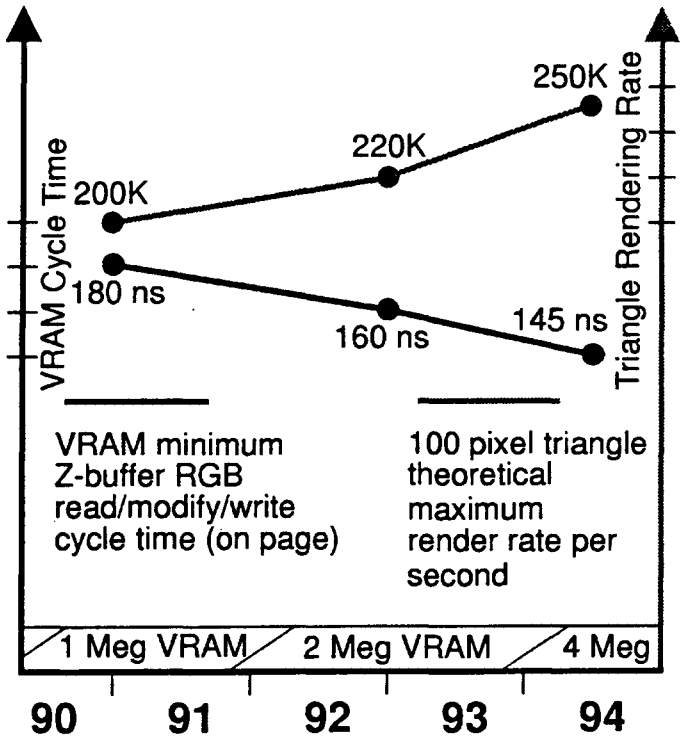
The VRAM Bottleneck



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LeoDraw Features

- Renders Triangles
- Renders aliased and anti-aliased lines
- Renders aliased and anti-aliased dots
- Variable alpha blend & screen door transparency
- Per-pixel depth-cueing of all 3D primitives
- 3D pick box, DMA pick support
- 2D BLIT, ROP, FONT, pixel support
- Very fast screen clear, optimized vertical scroll
- Controls VRAM and DRAM

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LeoCross Features

- Multiple color look-up tables
- "Cross bar" channel switching
- 32×32 cursor
- Video Timing, VRAM shift control
- Stereo and Virtual Reality device support

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Design Environment

Genisil 8.1 for LeoCommand, LeoFloat, LeoDraw

.8μ double metal one poly CMOS

LSI 100K master slice for LeoCross

25 MHz target for Genisil chips, 67 MHz for LeoCross

Complete high level simulator written in C

Zycad gate level simulation for individual chips & whole system

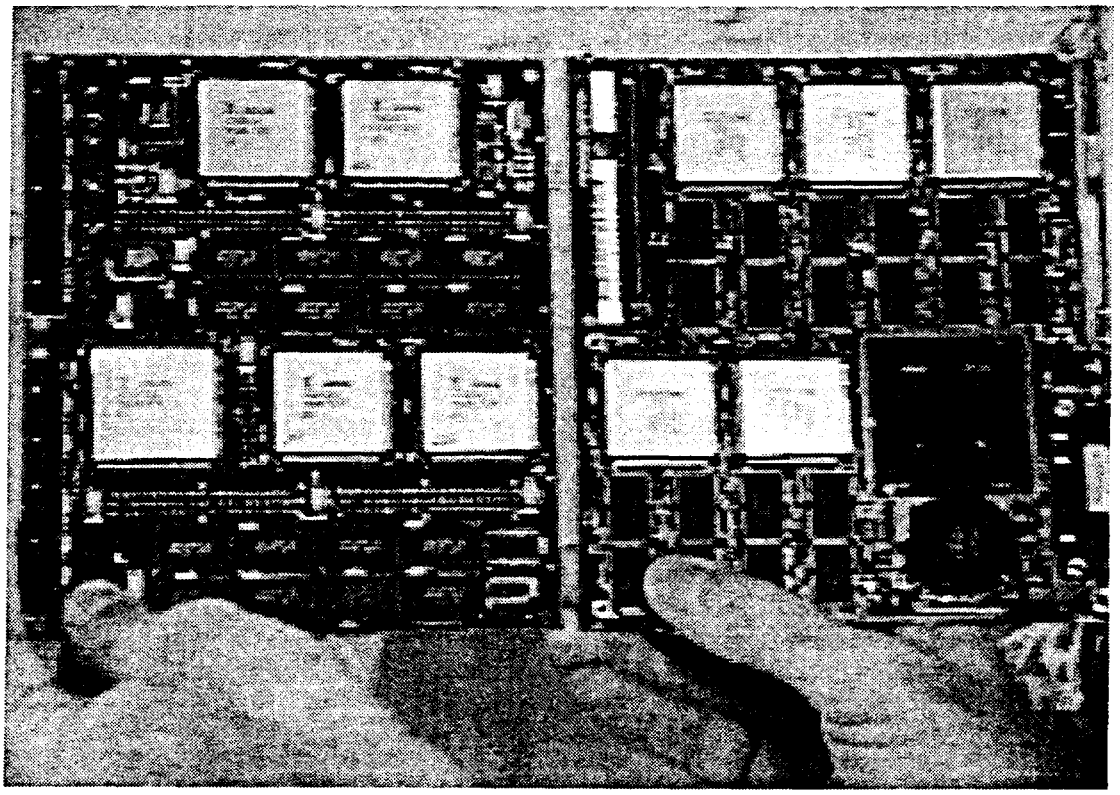
3 of 4 chips completely functional first pass

Board up and rendering 3D images within days of receipt of chips

IC Details

Chip	#gates	#transistors	die size mils/side	#pins
LeoCmd	83K	294K	580	240
LeoFloat	80K	280K	575	160
LeoDraw	77K	270K	520	208
LeoCross	35K	-	460	416

The Leo board set: 5.7" × 6.7" × 0.6"



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Performance

The Leo system achieves:

- **310K chained, un-lit, Gouraud shaded, Z-buffered 50 pixel depth-cued 3D triangles per second**
- **250K isolated, lighted, Gouraud shaded, Z-buffered, 50 pixel depth-cued 3D triangles per second**
- **750K chained, Z-buffer 10 pixel depth-cued 3D vectors per second**
- **450K antialiased, isolated, Z-buffered, 10 pixel depth-cued 3D vectors per second**
- **1.1M antialiased depth-cued 3D dots per second**
- **143K 8×10 raster characters per second**
- **under 200ns window clear time**

Note: all 3D performance benchmarks are averaged over many different orientations of the primitive.

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