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CDMA Mobile Station Modem (MSM) ASIC

Architecture, Design Approaches, Goals and Methodology

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Jurg Hinderling Tim Rueth Ken Easton
Dawn Eagleson Jeff Levin Daniel Kindred
Richard Kerr

QUALCOMM Incorporated
10555 Sorrento Valley Road
San Diego, CA 92121

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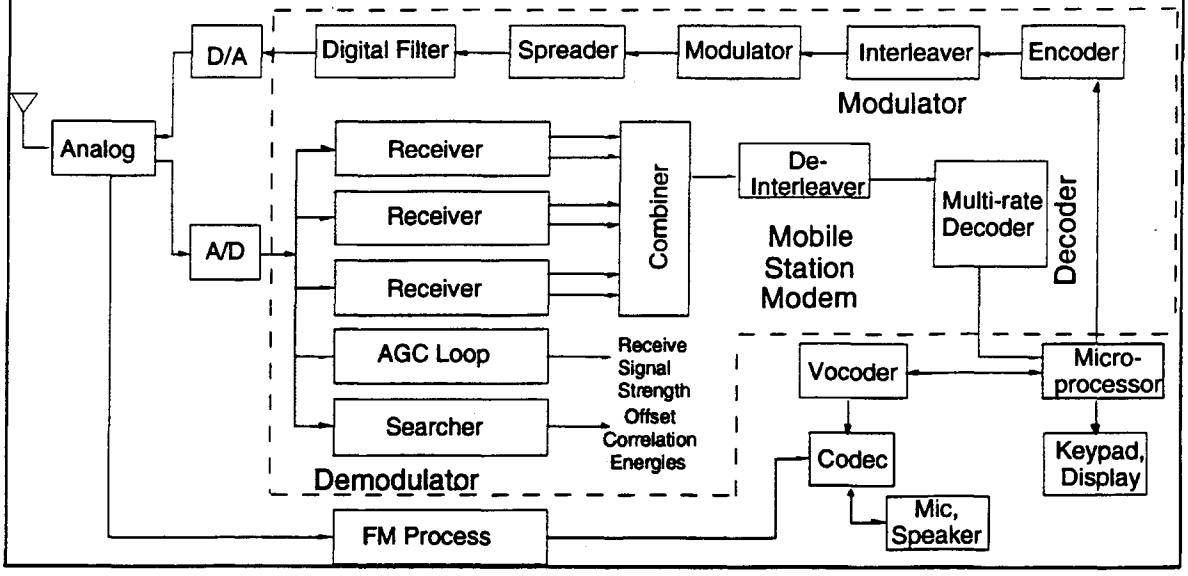
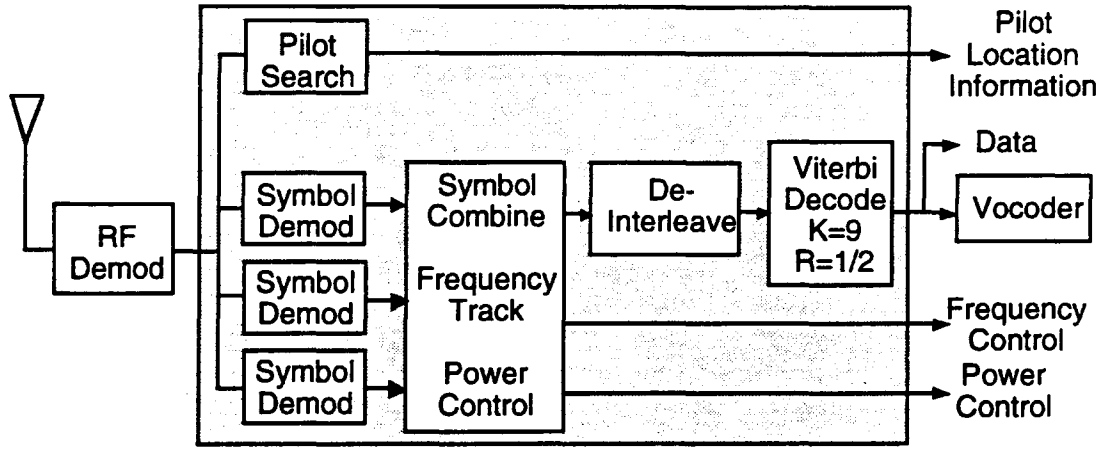
Overview

- Overview of MSM system architecture
- Design goals of the MSM project
- System and circuit design approaches
- Future goals and improvements for ASIC development
- MSM chip statistics

System Block Diagram



Forward Link Processing



Forward Link Processing: Symbol Demodulation

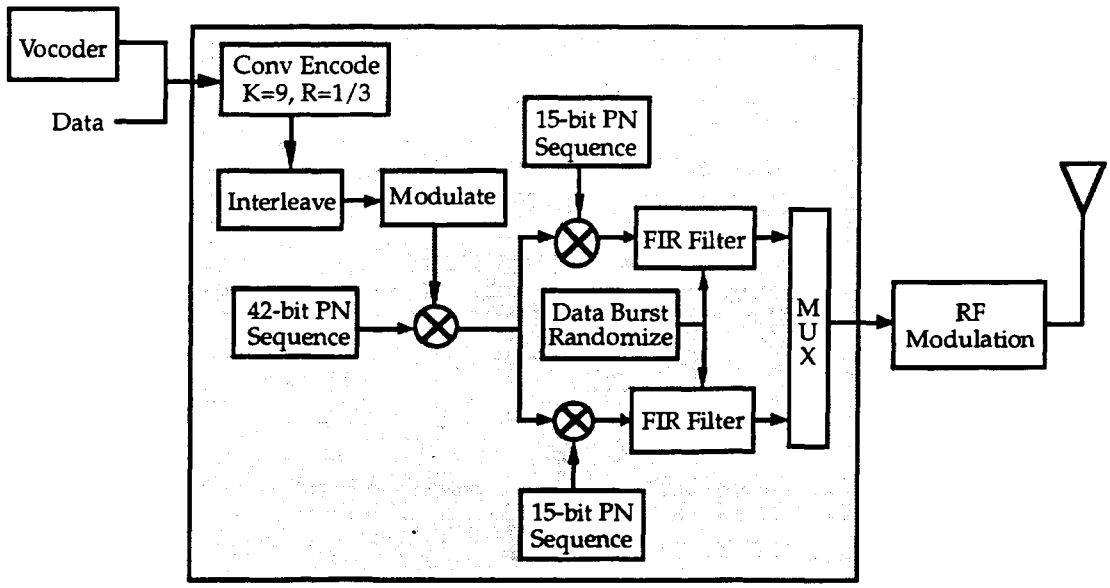
- Three main functional blocks:
  - three-finger rake receiver
    - demodulation
    - time tracking
    - soft decision symbol demodulation
  - combine data of locked fingers for
    - frequency tracking
    - final soft decision symbol generation
    - reverse-link power control
  - pilot searcher engine
    - energy computation for various pilot hypotheses

Forward Link Processing: Deinterleaving, Decoding

- Deinterleaving:
  - block deinterleaving
  - block interval dependent on forward link data rate
  - timing is derived from Symbol Combiner

- Serial Decoding:
  - implements classical Viterbi algorithm with one ACS pair
  - decodes at various effective code rates (1/2 - 1/16) without knowledge of actual code rate. This is due to the cell transmitting at different symbol repetition rates and symbol energy levels
  - based on data frame quality reported by decoder, the correct code rate is selected

Reverse Link Modulation



Reverse Link Processing: Encoding, Interleaving

- **Vocoder packets are convolutionally encoded for reverse link transmission at rate 1/3, constraint length k=9; the actual data transmission rate is voice-activity dependent**
- **Block interleaving over one 20 ms vocoder frame**
- **64-ary orthogonal modulation (Walsh functions). The Walsh function transmitted is determined by the information being sent (different from forward channel).**

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Reverse Link Processing: Encoding, Interleaving
continued

- BPSK-modulation with a user PN code and QPSK-spreading with the zero-offset pilot PN code
- Randomized data burst transmission at lower data rates to average actual traffic load on reverse link
- FIR filtering of the I and Q channel with 48-tap filter

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MSM Design Goals

- Lower production cost of CDMA modem function by integrating existing three chips into a single chip
- Allow design of a portable CDMA telephone in short time period
  - reuse existing logic, layout and test vectors as much as possible
- Integrate enhanced functionality
- Achieve lower power consumption by shrinking to 0.8-um process and increased level of integration
- Stay multi-foundry-based through broad technology specification
- Maintain testability of the three sub-circuits as separate blocks

System Design Approach

- General system simulations by means of
  - system-level C code and spreadsheets
- Hardware emulator was designed with existing three mobile ASICs and surrounding FPGA circuitry to prove system concept and to allow software development to proceed independently
- Quick transition into actual ASIC functional simulations by
  - hierarchical partitioning of ASIC into functional sub-blocks
  - running system simulation stimuli through mixed-mode simulator to provide data comparison between model database and actual circuit database
  - replacement of verified circuit-level netlist by high-level functional model to reduce top-level simulation time

System Design Approach
continued

- Top Level ASIC simulation only possible with a large set of functional models and very little actual transistor-based circuitry (netlists)
- Generation of simulation database will serve as production test vectors for ASIC. Production test vectors are ready at time of tape-out of ASIC
- Quick prototype evaluation on in-house IC testers, quick release of engineering samples into portable phone prototypes and to outside customers

Circuit Design Approach

- Several design methodologies were employed:
  - custom design library composed of handcrafted leaf cells and custom module compilers
  - HDL-based logic synthesis
  - hybrid
- Simple two-phase non-overlapping clock scheme
- Standard ratioed five-transistor latch cell used chip-wide

Circuit Design Approach
continued

- Microprocessor bus interface
  - provides a software method to write control and read status
  - scan path read and write –> good test vector density
  - adds circuit and bus-routing complexity
- Block-to-block routing strictly in metal for low resistance
- Top-level connectivity was established by a block router driven by schematic-derived netlist and controllable by limited set of router directives

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Future Goals and Improvements for ASIC Development

- do a higher degree of logic synthesis
  - approaching custom layout densities
- improved top-level electrical and timing analysis
  - accurate RC extraction
  - accurate simulation of AC and DC power consumption
- use ATPG to generate production-level vectors
- enforce a gate-level equivalent model be written for every block
  - allows hardware acceleration
  - much easier to fault grade
  - already supported when doing synthesis

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Future Goals and Improvements
continued

- achieve higher level of digital and analog sub-system integration
- design for testability
  - ensure that the state of each block can be completely defined after executing a limited number of test vectors
  - JTAG interface for improved board-level testability
  - more elaborate Built-In-Self-Tests (BIST)
    - move test vectors onto silicon itself
    - layout complexity must be kept simple

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MSM Chip Statistics

- 450,000 transistors: 28 kbytes RAM and 70,000 equivalent gates
- Main clock rate: 10 MHz, fastest clock rate: 20 MHz
- First silicon was fabricated in 0.8 micron fully static CMOS
- Die size: 418 mil x 424 mil (177k square mils)
  10.6 mm x 10.8 mm (114 square mm)
- Max power consumption 300 mW @5 V
- 144-pin thin quad-flat package
- Design time of original 3-chip set: 240 man-months, MSM chip integration/enhancement cycle took another 24 man-months
- Total number of test vectors is approximately 500k
- Computing hardware: workstations and servers in the 15 - 50 MIPS range with typically 64 Mbytes RAM and 600-900 Mbytes of local disk storage

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<MSM ASIC die slide>