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Optimized Pentium™ Processor 82430 PCIset for High Performance Local Bus Designs

Hot Chips Symposium
August 8-10, 1993
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Intel Corporation

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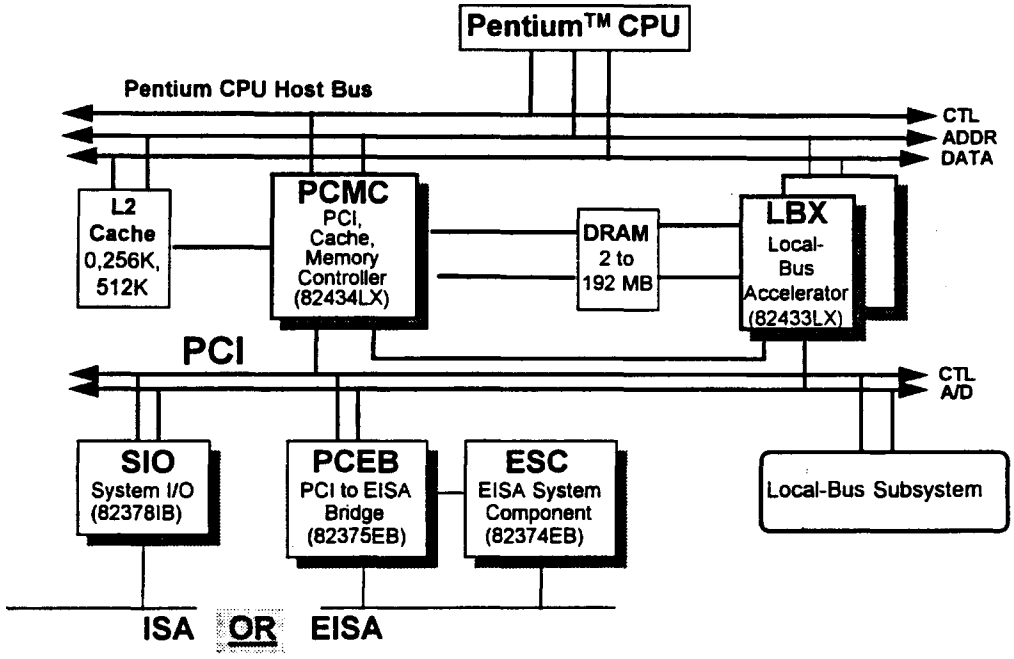
Agenda

- Design Goals
- Architecture Overview
- Implementation Details
- Benchmark Results
- Summary

Design Goals

- Highest Performance 66MHz Pentium Processor Desktop Systems
- Flexible L2 Cache and DRAM Options for Optimized Price/Performance
- Enable Graphics Performance Second to None
- High Performance PCI Local Bus
  - ➢One Clock Burst Performance
- Optional Expansion Bus (ISA, EISA)

82430 PCIset



Uncompromised CPU and PCI Local-Bus Performance

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82430 PCIset Overview

- **Integrated PCI for Highest Speed Local Bus**
  - Highest graphics bandwidth
  - Multiple local bus peripherals and masters
  - 4-deep buffering eliminates system bottlenecks
- **Sophisticated Cache Controller**
  - Multiple cache sizes (0, 256KB, 512KB) with Standard or Burst SRAM
  - Integrated Tag RAM
  - Write-through or Write-back design
- **ISA or EISA Standard Bus**
  - ISA in one integrated component
  - High-performance, two-component, EISA bridge
- **Designed for the Pentium™ Processor Family**
  - Supports Pentium processor to 66 MHz with full 64-bit data paths
  - 82430 PCIset will support future Pentium CPU family members

Balanced System Power for a New Class of Pentium Processor Machines

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PCI Local Bus Features

- ❑ Processor Independent
- ❑ Multiplexed, Burst Mode (Read & Write) Operation
- ❑ Synchronous at Frequencies up to 33 MHz
- ❑ 120 MB/s useable throughput (132 MB/s peak) for a 32-bit Data Path
- ❑ Capable of Full Concurrency with Processor/Memory Subsystem
- ❑ Full Multi-master Capability Allowing any PCI Master Peer-to-Peer Access to any PCI slave
- ❑ Low Pin Count (45 slave, 47 master)
- ❑ Address and Data Parity
- ❑ Support for Autoconfiguration

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82430 PCIset
Implementation Details

- ❑ PCIset Partitioning
- ❑ Optimized Host Bus Interface
- ❑ Optimized L2 Cache Subsystem
- ❑ Integrated DRAM Controller
- ❑ CPU - to - PCI Bridge Functions
- ❑ ISA or EISA Expansion Bus

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PCIset Partitioning

Host Bus to PCI Bridge

- ❑ PCI/Cache/Memory Controller (PCMC)
  - 208-Pin QFP Package
  - 5V CMOS Technology
- ❑ Local Bus Accelerator (LBX)
  - ½ Slice of Host Address and Data Bus
  - 160-Pin QFP Package
  - 5V CMOS Technology

PCI-to-ISA Bridge

- ❑ System I/O (SIO)
  - 208-Pin QFP Package
  - 5V CMOS Technology

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PCIset Partitioning (con't)

PCI-to-EISA Bridge

- ❑ PCI/EISA Bridge (PCEB)
  - 208-Pin QFP Package
  - 5V CMOS Technology
- ❑ EISA System Controller (ESC)
  - 208-Pin QFP Package
  - 5V CMOS Technology

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Optimized Host Bus Interface

- ❑ 64-bit Data Path, 32-bit Address Bus with Pipelining
- ❑ Synchronous Operating Frequencies of 60MHz and 66MHz
- ❑ Burst Read and Write Transfers
- ❑ Support for First Level and Second Level Caches
- ❑ Capable of Full Concurrency with the PCI and Memory Subsystems
- ❑ Byte Data Parity

Optimized Host Bus Interface

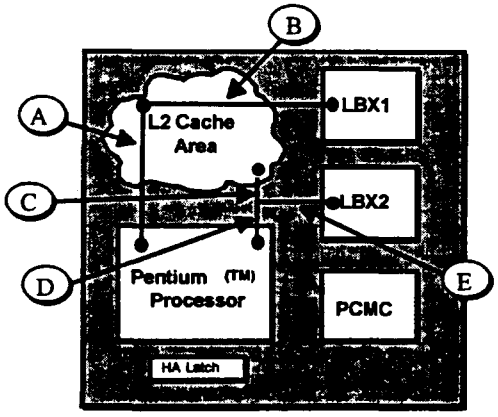
- 66MHz Design Issues
  - Optimized pinout for minimum chip-to-chip interconnect
  - Reference Design Films available
  - "EZ Route" Layout Guidelines
    - ➢ >5000 Hours of Interconnect Simulation and Correlation
  - Pioneered "IBIS" Modeling Concept
    - ➢ Supported by leading simulation vendors
    - ➢ Cadence, Contec Micro., Hyperlynx, Integrity Engr., IntuSoft, Meta-Software, MicroSim, Quad-Design, Quantic Labs

Signal Integrity Designed In for 66MHz

EZ Route Layout Guideline Sheet

Chipset: 82430 PCIset
Interface: Host Data Bus
Signals: HD [63:0], HP [7:0]

Revision: 0.9



Length Guidelines				
Route	Connection	Min	Max	Unit
A	Pentium(tm) to L2	0.5	3.0	Inch
B	L2 to LBX	0.5	3.1	Inch
C	L2 to T-point	0.5	1.7	Inch
D	Pentium(tm) to T-point	0.5	1.7	Inch
E	LBX to T-point	0.5	1.7	Inch

Flight Times				
Code	Connection	Min	Max	Unit
hdpent\1,t	Pentium(tm) to LBX	0	2.3	ns
hdpent\1,t	Pentium(tm) to L2	0	3.0	ns
hdsram\1,t	L2 to Pentium(tm)	0	2.1	ns
hdsram\1,t	L2 to LBX	0	2.6	ns
hdlbx\1,t	LBX to Pentium(tm)	0	2.2	ns

Notes: Organize L2 cache Components so signals flow logically from Pentium(tm) CPU pinout to both LBXs. When this is done, routes will generally be much shorter than the inch limitations given above. The longest routes will be those to the top of LBX1. There are two route styles: A/B or C/D/E. Signals can choose either route style.

PCB Fabrication Assumptions				
Param	Description	Min	Max	Unit
Zo	Fabricated Impedance	50	80	Ohms
Td	Propagation Velocity	0.15	0.2	ns/in
Er	Dielectric Constant	4.8	5.2	-

This information is very preliminary and subject to change.

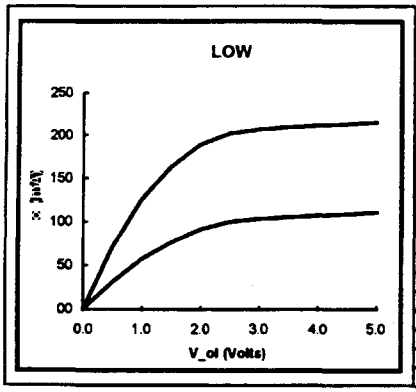
Host Data Bus

IBIS

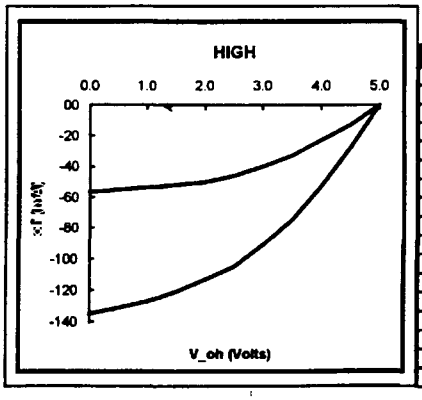
I/O Buffer Information Sheet

Component: S82374EB ESC **Buffer Type:** O

Signals: BALE, BE#[3:0], CHRDY, CMD#, EX16#, EX32#, EXRDY, IORC#, IOWC#, LA[31:2], M16#, MRDC#, MSBURST#, MWTC#, M/IO#, NOWS#, REFRESH#, RSTDRV, SA[1:0], SBHE#, SD[7:0], SMRDC#, SMWTC#, SPKR, START#, W/R#, EOP (Note: EXRDY, EX16#, CHRDY, EX32#, M16#, and NOWS# are open drain signals, and can only be driven low.) **ESC2 Revision:** 1.0



V_ol	I_ol min	I_ol max
-5.0	-110	-216
-4.0	-107	-212
-3.0	-103	-207
-2.0	-91	-189
-1.0	-57	-126
0.0	00	00
0.5	31	71
1.0	57	126
1.5	76	163
2.0	91	189
2.5	100	202
3.0	103	207
3.5	105	210
4.0	107	212
4.5	109	214
5.0	111	216
10.0	120	230



V_oh	I_oh min	I_oh max
-5.0	-65	-155
0.0	-57	-135
0.5	-55	-131
1.0	-54	-127
1.5	-52	-121
2.0	-50	-113
2.5	-46	-105
3.0	-40	-91
3.5	-33	-75
4.0	-23	-53
4.5	-13	-28
5.0	00	00
6.0	23	53
7.0	40	91
8.0	50	113
9.0	54	127
10.0	57	135

Beyond the Rail Info

Diode to GND		Diode to Vcc	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	0	5.4	0
-0.5	0	5.5	0
-0.6	0	5.6	0
-0.7	-5	5.7	4
-0.8	-35	5.8	30
-0.9	-70	5.9	52
-1.0	-110	6.0	74
-5.0	-1725	10.0	970

Packaging Characteristics

	min	max	unit
R_pkg	226	405	mOhm
L_pkg	8.5	15.1	nH
C_pkg	1.9	2.8	pF
C_comp	2	7.2	pF

Ramp Time (into 0pF, no pkg)

	min	max	unit
Rise	5.25 / 0.45	4.75 / 1.45	volt / ns
Fall	5.25 / 0.44	4.75 / 1.61	volt / ns

Simplified Output Resistance

	min	max	unit
Low	7.4	19.4	ohms
High	19.9	56.1	ohms

Optimized L2 Cache Subsystem

- Optional 256KB or 512KB Second Level Cache
- Direct-Mapped Organization
- Integrated Cache Tag RAM
  - Cost and Board Space Savings
  - Minimize Host Bus Loading
- Burst SRAM for Highest Performance Cache
  - 3-1-1-1 Cache Hit Read and Write Timing
- Standard SRAM for Lowest Cost Cache
  - 3-2-2-2 Cache Hit Read Timing
  - 4-2-2-2 Cache Write Timing

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Optimized L2 Cache Subsystem (Con't)

- Programmable Write-Through and Write-Back Modes
- Concurrent Cache Line Replacement
- Cache Snoop Filter
  - ➢ Snoop Only when PCI Master Crosses Cache Line Boundary

Flexible L2 Cache for Optimized Price/Performance

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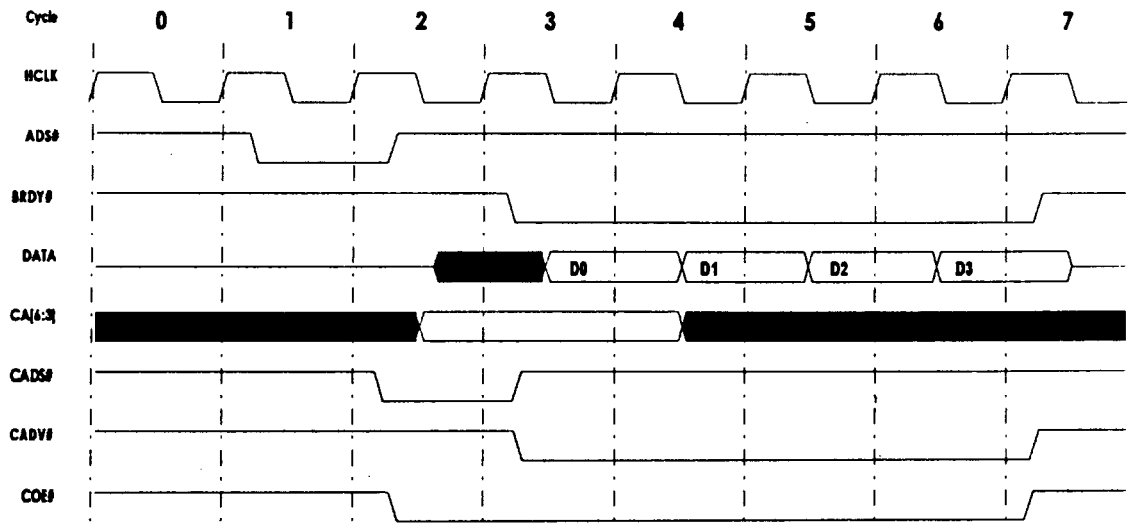
Burst Read, Burst SRAM



- **Burst SRAMs internally count through the Pentium™ burst order**

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Integrated DRAM Controller

- 2 MBytes to 192 MBytes of Cacheable Main Memory
- Programmable Attribute Map Registers
  - Cacheability
  - Read/Write Status
- Memory Space Gap Register
  - Logical Hole for Memory Mapped Add-in Cards
- Frame Buffer Range Register
  - Byte Merging for CPU-to-PCI Writes
  - 0 Waitstate PCI Burst Cycles
  - Read-Around-Writes
  - CPU-to-PCI Prefetch
  - Transparent Buffer Writes - Write Buffers Not Flushed

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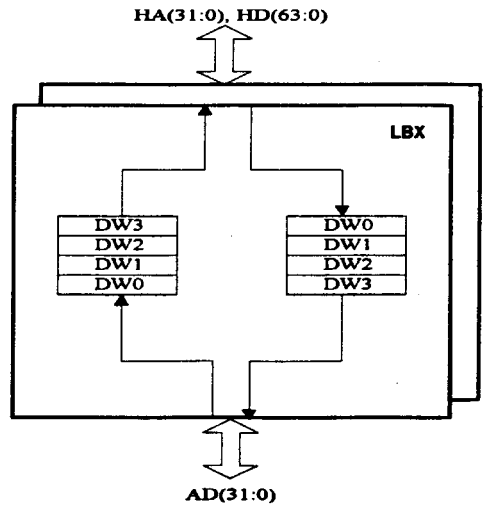
CPU-to-PCI Bridge Function (Con't)

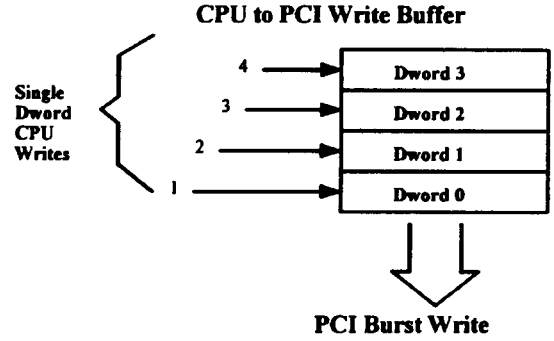
- Posted Write Buffers
  - CPU-to-PCI
  - CPU-to-Main Memory
  - PCI-to-Main Memory
- Prefetch Buffers
  - CPU Reads of PCI
  - PCI Reads of Main Memory

CPU/PCI Bridge Buffers



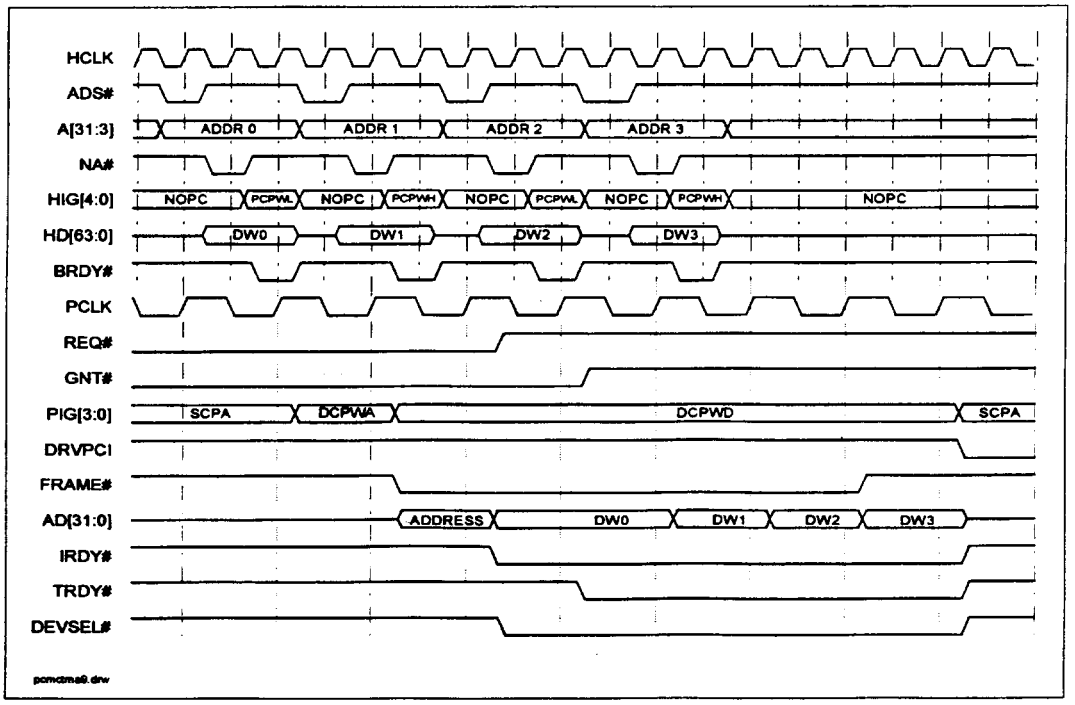
- Four Dword Posted Write Buffer
  - •Dword Packetizing
  - •Byte Merging
- Four Dword Read Prefetch Buffer

Dword Packetizing



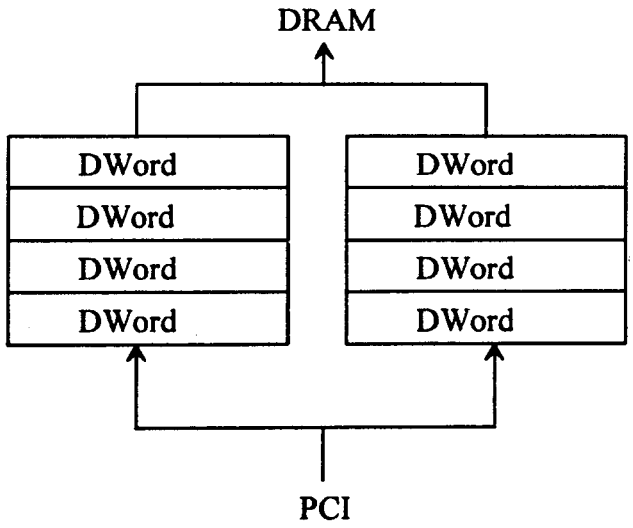
- As the CPU writes sequential incrementing Dwords, the PCMC/LBXs burst data to PCI at 2-1-1-1.....
- Fast memory to screen transfers!

CPU Memory Writes to PCI



PCI-to-Memory Posted Write Buffer

- Two buffers, 4 DWords each. Each Buffer allocated on new transaction request.



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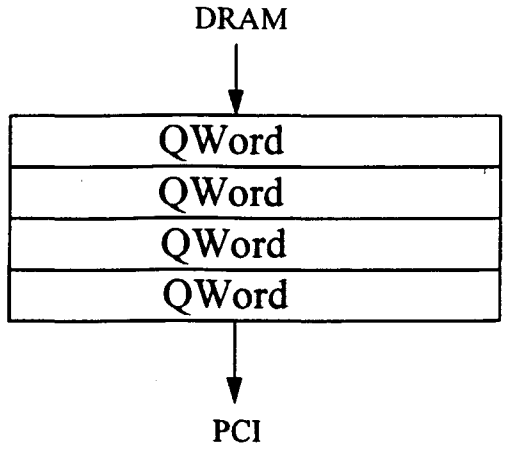
Memory-to-PCI Read Buffer

- One Line Buffer, 4 QWords
- Data is Read from Memory as QWord, Driven on PCI as DWord



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ISA or EISA Expansion Bus

EISA Bridge
- 4-Deep, 16 Byte Line Buffers for EISA Bursts
- PCI and EISA Bus Concurrency
- 4-Deep, 4 Byte Posted Write Buffers
- Scatter/Gather DMA
- Supports 8 EISA Masters/Slots

ISA Bridge
- PCI-to-ISA Buffers
- ISA-to-PCI Buffers
- Scatter/Gather DMA
- Fast DMA Type A, B, and F
- Supports 6 ISA Slots/2 Masters
- High Integration Single Chip

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Benchmark Results

This slide will list the performance results of several standard benchmarks.

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Summary

- 82430 PCIset Enables High Performance Pentium Processor Desktop Systems
- Offers Design Flexibility and Price/Performance Tradeoffs
- Provides High Performance PCI Local Bus with 1 Clock Burst Write Capability
- Frame Buffer Features Offer High Performance Graphics