Hummingbird:
A Low-Cost Superscalar PA-RISC Processor

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Hot Chips V

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Presentation Outline

- Introduction
- Design Goals
- Processor Overview
- Cost Reduction
- Performance
- Scalability
- Power Reduction and Test
- Summary

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Design Goals

- Minimize **System** Cost
- Meet or Exceed Current Mid-Range Workstation Performance in an Entry-Level System
  - Integer
  - Graphics
  - Multimedia
- Scalability
- Low Power Consumption
- Fully Compliant with PA-RISC Architecture
- Design for Manufacturability

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Processor General Features

- Core Technologies and Features From PA7100
- High Integration
  - Floating Point and Integer Processors
  - On-chip Instruction Cache
  - Off-chip Cache Controller
  - Memory and I/O Controller
- 2-Way Superscalar
- 2 Integer ALUs
- Architectural Extensions

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Architectural Features

- Support for Little-Endian Processes
  - PC Emulation and Other Software
- Support for Uncacheable Memory Pages
  - Enhances Performance of I/O Subsystems
- Support for Multimedia Processing
  - Improves Most Multimedia Applications
  - Addition / Subtraction with Saturation
  - Arithmetic Averaging
  - Shift-and-Add for Multiplication by Constant
  - Pixels, Audio Samples, Text
  - 4X Speed Up

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Technology

- HP's CMOS26B Process
  - 0.8 micron FET's
  - 3-level Metal Interconnect
- 0-75+ MHz
- 900,000 Transistors
- 14mm x 14mm Die Size
- 432 Pin Cost-Reduced PGA
  - 1.8" x 1.8"
  - 50 mil Interstitial Pin-Grid
  - High-Speed Operation w/o Bypass Caps
- 5V Vdd, TTL Compatible I/O Levels

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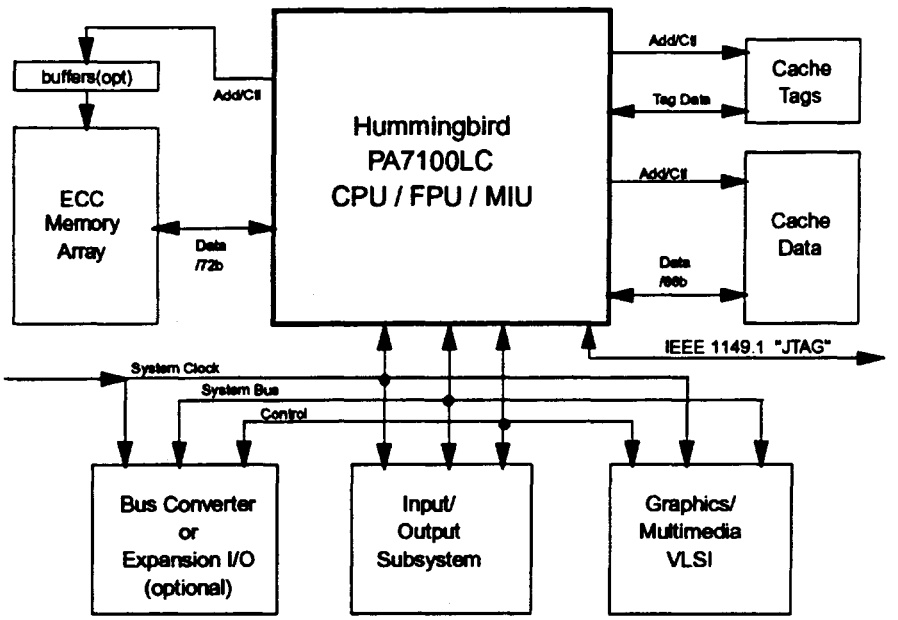
System Block Diagram



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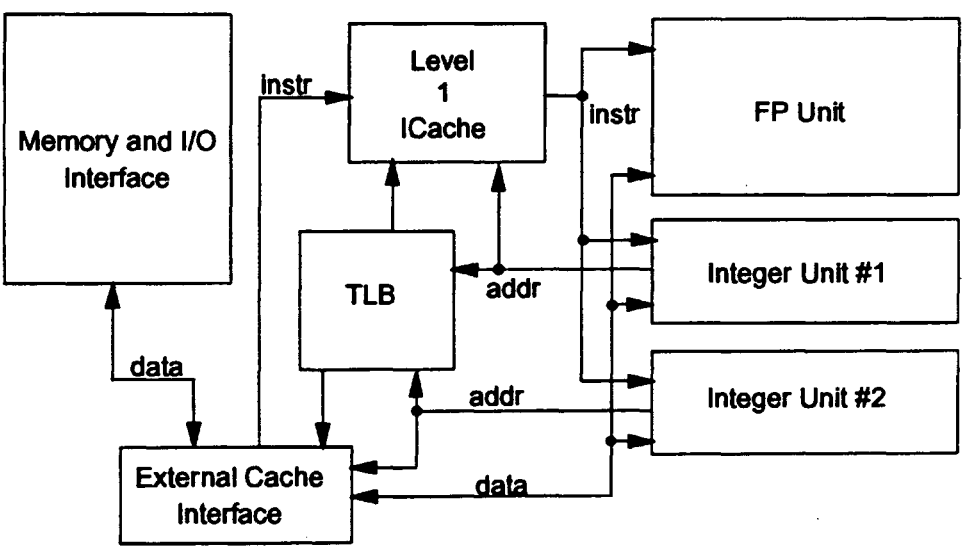
Hummingbird (PA7100LC)



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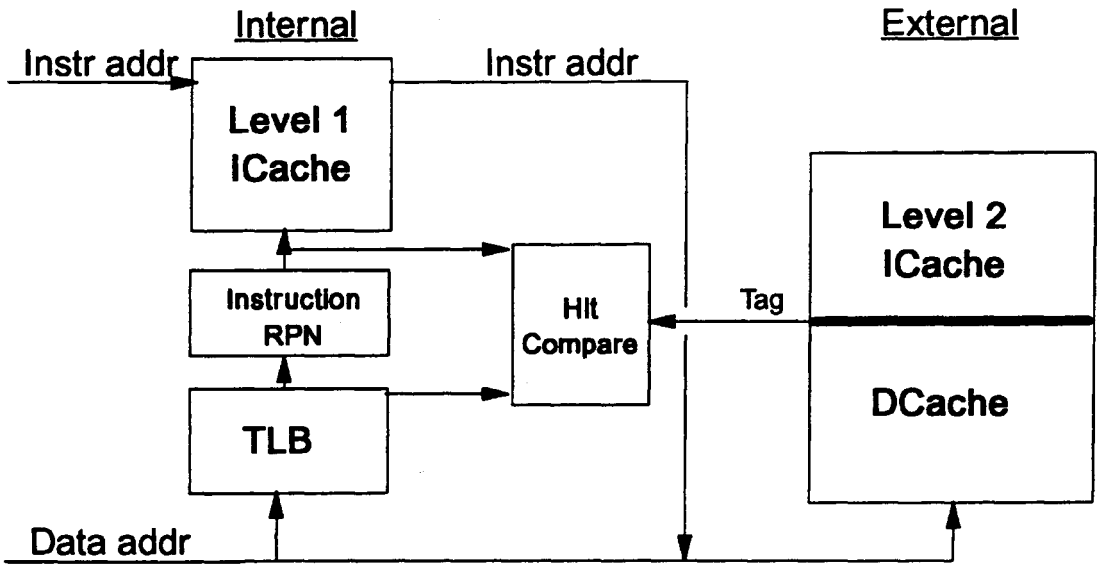
Cache Organization



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PA7100LC Die Photograph

(To Be Completed)

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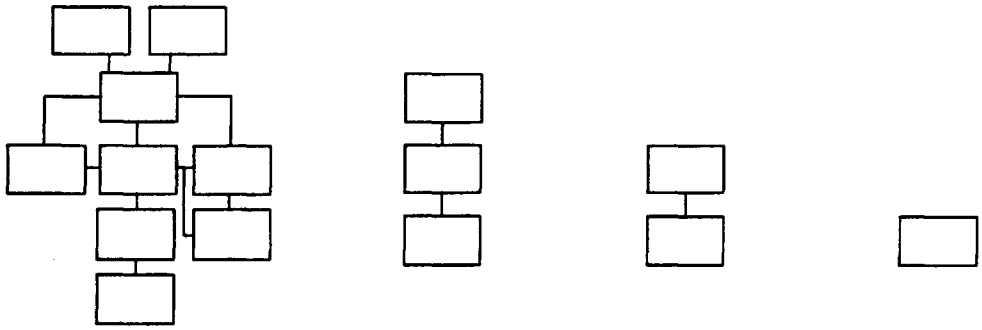
PA-RISC Integration Trend



1989 1991 1992 1993

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System Cost Reduction

- Integrated Memory and I/O Controller
- Direct Connection to DRAMs
- Single, Combined External Cache
- Uses Standard SRAMS, DRAMS, and SIMMs
- Requires Only 12 SRAM's Using x8 Technology
- With 12ns parts can run to 66MHz
- Low Power
- Mature VLSI Technology
- Reduced Cost Packaging

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System Cost Reduction (Continued)

- Reduced Multiplier Array with No Degradation to Single Precision Flops
- Reduced Complexity for Long-Latency Flops
- 64 Entry Fully-Associative TLB
- Unified TLB with Lookaside Buffer
- Multimedia Improvements without Dedicated Hardware

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Superscalar Instruction Bundling

Instruction Classes	Rules
A: Integer ALU Operation Shift/Merge Operation Branch	Any 2 from sparate classes or 2 integer ALU operation
L: Int or FP Load/Store	L-L bundles for ldw or stw pairs to same doubleword address
E: Floating Point Operation	Dynamic dependency checking

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FP Latency and Issue Rates

	Single Precision	Double Precision
Add / Sub	2 / 1	2 / 1
Multiply	2 / 1	3 /2
MPYADD / MPYSUB	2 / 1	3 / 2
Divide	8 / 8	15 / 15
Square Root	8 / 8	15 / 15

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Virtual Memory Performance

- 8 Block TLB Entries, Each Map 512K - 64MBytes
- Hardware TLB-Miss Handler
- "Fast" TLB Insert Instructions
- GR Shadow Registers

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Cache Performance

- External Cache Runs at Processor Frequency
- Pipelined Stores
- Address Hashing
- Cache Miss Optimizations
  - Instruction Streaming
  - Stall-on-Use
  - Hit-Under-Miss
  - Store-Under-Miss
  - Miss-Under-Miss
- Cache Hints
- Aggressive Instruction Prefetching

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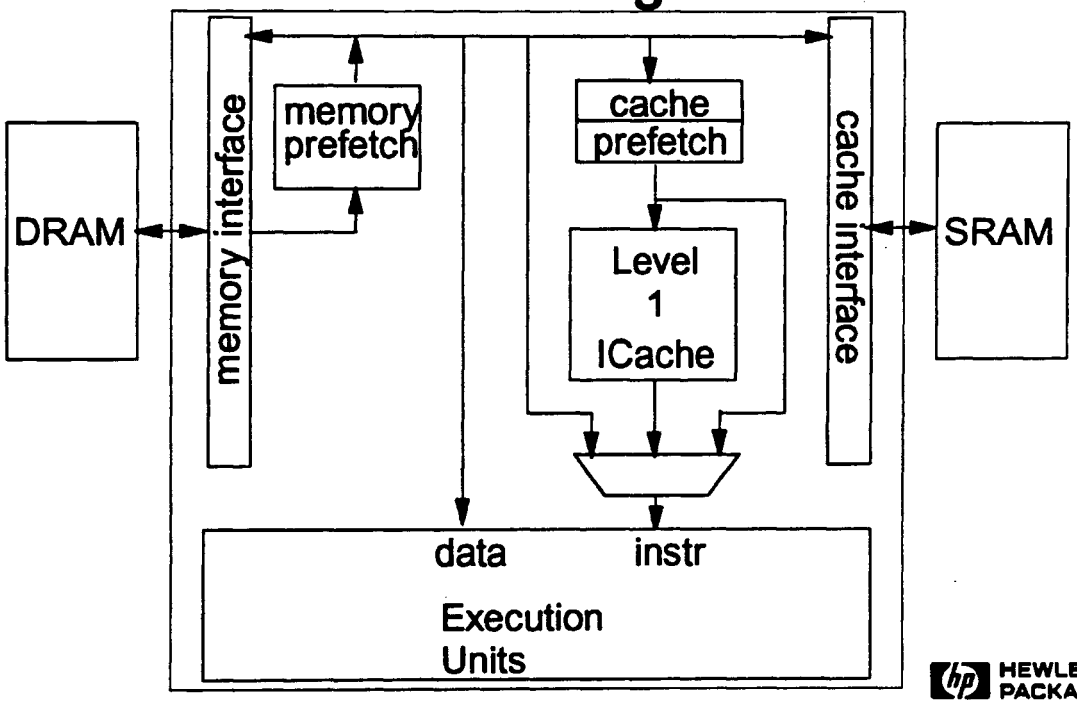
Instruction Prefetching



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Memory and I/O Performance

- Dedicated 64-bit Memory Bus + 8 ECC Bits
- Tightly Coupled to CPU
  - Early Address Issue
  - Critical Doubleword First
- Uses DRAM Fast Page Mode
- Supports Extended Data Out Mode DRAMs
- Dedicated 32-bit I/O connection
  - DMA Concurrent with Cache Misses
- 50MB/sec Sustained CPU-Controlled Memory to I/O Transfer

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Scalability

- Wide Range of Processor Frequency
- 48 Bit Virtual Addressing
- 8K to 2MBytes of External Cache
- 4M to 2GBytes of Main Memory
- Programmable DRAM latency and timing
- Programmable I/O Bus Frequency

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Low Power Design

- Limited Use of Dynamic Circuits
- Elimination of PLA's
- Automatic Power-Up States
  - TLB
  - FP Megacells
  - Register Files
- Gating of Non-Overlapping Clock Nets

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Design for Testability

- IEEE 1149.1 (JTAG) Compliant
- Parallel and Serial Block Tests
- Extensive Scannability
- Single-Step Capability
- IDDQ Static Current Testing

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Summary

- Optimized For Low Cost Systems
- Performance Was Not Sacrificed
- Highly Configurable
- New Features
- Low Power
- Low Manufacturing Costs

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