# R4200 (Codename ICE)

## A high-performance MIPS microprocessor for portables

Barb Zivkov,
MIPS Technologies Inc.

Hot Chips Symposium
August 9, 1993

mips
Open RISC Technology

# Introduction and agenda

1/ R4200 Program objectives

2/ Key features

3/ Feature comparison

mips
Open RISC Technology

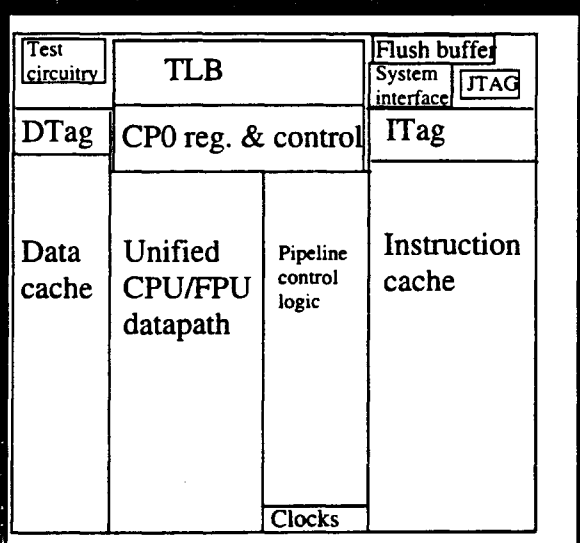
# 1/ R4200 Program Objectives

*Design for portables*

- Low power (<= 2 watts)
- Low cost (<= $100)
- Small die size (<= 100 sq. mm)
- High performance (>= 50 SPECint92)
- Modular design (Megacell capable)
- R4000/R4400 Compatibility (HW & SW)

mips
Open RISC Technology

# R4200 Floorplan




mips
Open RISC Technology

# Low Power:

- Designed for 3.3 volts
- Caches organized in banks
- Writeback cache
- Instruction cache Prefetch buffer
- Instruction micro-TLB
- Unified datapath
- Power management capability

mips
Open RISC Technology

# Low Power (continued):

*How does power management work?*

- For reduced system activity, switch to RP mode
  - RP "reduced power" mode dissipates 0.4W
  - processor slows to 1/4 of normal frequency
  - no sacrifice in functionality
  - dynamically initiated by external agent / software
- For low system activity, switch to instant-off mode
  - instant-off mode dissipates 0 power
  - save processor state, flush cache
  - save / restore completed in milliseconds

mips
Open RISC Technology

# Low Cost:

- Volume price near $70
- Small die-size (76 sq. mm)
- Plastic 208-pin QFP packaging
- High yields (column redundancy in caches, conservative design methodology)
- High-volume mass-production

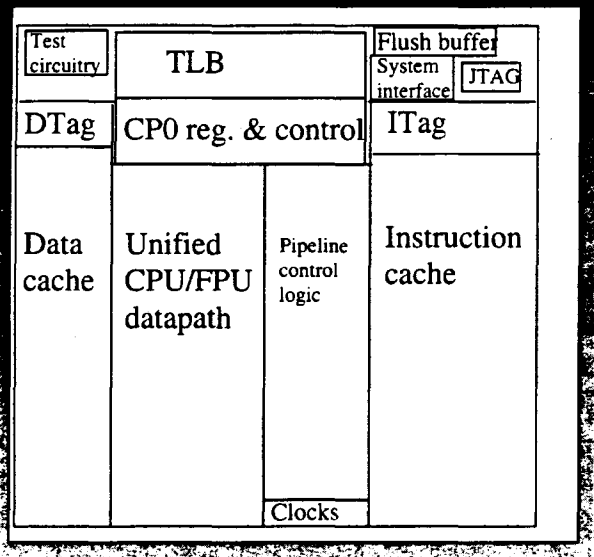
mips
Open RISC Technology

# High Performance:

- 55 SPECint92 & 30 SPECfp92 (simulated with 256 KB write-through L2 cache)
- 50 SPECint92 & 28 SPECfp92 (simulated with no L2-cache)
- 160 MB/sec (sustained) System Interface
- Low latency for primary cache miss

mips
Open RISC Technology

# R4200 - Modular design




Easy to ...

Increase/decrease caches

Increase/decrease TLB

Change system interface

Offer core as megacell

Generate derivative designs

mips
Open RISC Technology

# R4000 / R4400 Compatibility:

- Full MIPS-III instruction set
- Full User- / Supervisor- / Kernel-level compatibility
- R4000 / R4400 compatible system interface
- R4000PC / R4400PC compatible packaging option, 179-pin CPGA (R4200PC)

mips
Open RISC Technology

# 2/ R4200 key features:

*Wise allocation of resources*

- Traditional RISC pipeline
- Large on-chip caches
- Unified datapath
  - Focused subset of R4000/R4400
  - Detailed facts and figures

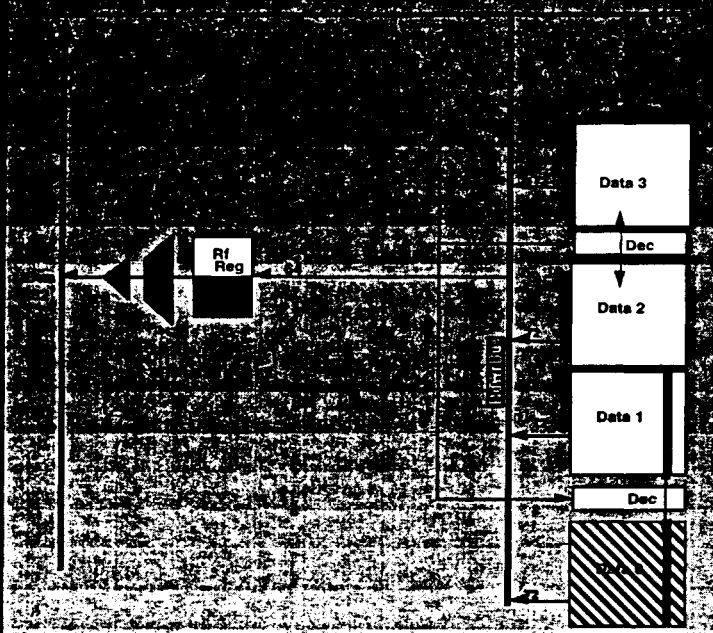
mips
Open RISC Technology

# Traditional RISC pipeline

- 5 stages (IC->RF->EX->DC->WB)
- Shorter stalls
- Simpler control
- No branch interlock / penalty
  (one architecturally defined delay slot)
  - More efficient at low clock frequencies (less power)

mips
Open RISC Technology

# Large on-chip caches

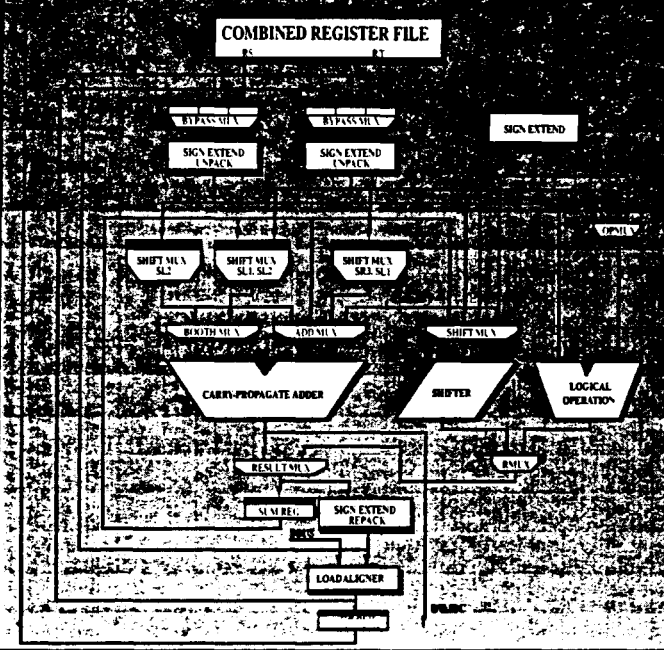



Instruction cache design
14-bit index (16Kbyte cache)
8-word line size, 4T RAM cells

- Writeback reduces system activity (low power)
- Organized in banks; only 1 bank powered on in any 1 access for power reduction (2 MSB's select bank)
- 1 cache access, 2 sequential instructions fetched (further reduces power)
- High hit rate (96.4% hit I-cache on SPECint92)
- Column redundancy for improved yields

mips
Open RISC Technology

# R4200 - Unified Datapath




- *Separate registers, shared datapath*
- *Less die area, lower cost*
- *Less capacitance, lower power*
- *Multicycle execution for Multiply, Divide, FP instructions with variable latencies*

mips
Open RISC Technology

# R4200 Unified datapath (contd.):

*What are these variable latencies?*

| Instruction | Int(32) | Int(64) | FP(SP) | FP(DP) |
|---|---|---|---|---|
| Add/sub | 1 | 1 | 2,3 | 2,3 |
| Multiply | 13 | 24 | 2,11 | 2,20 |
| Divide | 37 | 69 | 2,29 | 2,58 |
| Sqrt | - | - | 2,30 | 2,59 |
| Abs/neg | - | - | 1,1 | 1,1 |
| Compare | - | - | 1,1 | 1,1 |
| DP->SP | - | - | 2,2 | 2,2 |
| SP->DP | - | - | 1,1 | 1,1 |
| FP->Int | - | - | 2,5 | 2,5 |
| Int->FP | - | - | 2,5 | 2,5 |

mips
Open RISC Technology

# R4200 Focused configuration

- Primary cache support only
- No MP support
- 2 page sizes supported (4KB & 16MB)
- Fixed cache line sizes (Inst.– 8 words; Data – 4 words)

mips
Open RISC Technology

# R4200 Detailed facts & figures

| | |
|---|---|
| Product configurations: | R4200LP, R4200PC |
| Die size: | 8.8mm x 8.6mm |
| Process technology: | 0.6 micron, 3 layer metal, 2 poly |
| Clock rates: (external/internal) | 40/80 MHz (normal), 10/20 MHz (reduced power) |
| Transistor count: | 1.3 million |
| Packages: | 208-pin PQFP, 179-pin C-PGA |
| On-chip I-cache: | 16 kilobytes w/ 8-word line |
| On-chip D-cache: | 8 kilobytes w/ 4-word line |
| Supply voltage: | 3.3 volts +/- 10% |
| Power consumption: | 1.5W (normal), 0.4W (reduced) |
| On-chip integration: | Combined CPU/FPU, I-cache, D-cache, MMU w/ 32 double-entry TLB, 64-bit interface bus, Power management features, Graphics fush-buffer |

mips
Open RISC Technology

# 3/ Feature comparison:

*How does R4200 compare to other processors?*

- **Implementation data**
- **Performance data**

mips
Open RISC Technology

# R4200 Implementation data

| Processor | Size (sq. mm) | Micron/metal | Primary cache Inst. | Data | Approx. cost |
|---|---|---|---|---|---|
| R4000SC | 184 | 0.8 / 2 | 8K | 8K | $600 |
| R4400SC | 184 | 0.6 / 2 | 16K | 16K | $1100 |
| i486 DX/2 66 | 82 | 0.8 / 3 | 8K (Unified) | | $500 |
| Pentium | 294 | 0.8 / 3 | 8K | 8K | $1000 |
| PowerPC | 121 | 0.6 / 4 | 16K | 16K | $400 |
| MicroSPARC | 225 | 0.8 / 3 | 4K | 2K | $200 |
| Hobbit | 73 | 0.6 / 2 | 3K | 0K | $35 |
| R4200 | 76 | 0.6 / 3 | 16K | 8K | $70 |

mips
Open RISC Technology

# R4200 Performance data

| Processor | MHz | SPEC92 | | Power | SPECint92/ watt |
|---|---|---|---|---|---|
| | Ext/Int | Int | FP | Watts | |
| R4000SC | 50/100 | 62 | 63 | 12 | 5.2 |
| R4400SC | 75/150 | 94 | 105 | 15 | 6.3 |
| i486 DX/2 66 | 33/66 | 32 | 16 | 7 | 4.6 |
| Pentium | 66 | 64 | 57 | 20 | 3.2 |
| PowerPC | 66 | 45 | 70 | 9 | 5.0 |
| MicroSPARC | 25/50 | 23 | 18 | 4 | 5.8 |
| Hobbit | 25 | 8? | 8? | 0.4 | 20.0 |
| R4200 | 40/80 | 55 | 30 | 1.5 | 36.7 |

mips
Open RISC Technology