



***DECchip 21066 -
Alpha AXP
Architecture Processor
for Low-Cost
Applications***

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***Microprocessor attributes by
system band***

System Band	1st Priority	2nd Priority
Performance Driven	Performance	
Value Driven	Price/Performance	Performance
Cost Driven	Price	Integration Performance
Low-power Driven	Low-power	Integration Performance/Watt

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DECchip 21066 Goals

- **Highly Integrated Microprocessor**
 - **Benefits are:**
 - ◆ **Lower System Cost**
 - ◆ **Faster Time-to-Market**
- **High Performance**
- **Leverage of Existing Design**

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Leverage of existing design

- **Start with existing CPU, FPU, Instruction and Data cache of 21064**
- **Remove pin interface logic**
- **Add memory controller and PCI Bus controller**
- **Lower manufacturing cost through process shrinks**
 - **Original design used .75 um process**
 - **10% linear shrink for first version (.675 um)**
 - **33% linear shrink for second version (.5 um)**

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DECchip 21066 Floorplan



CPU and FPU Feature Summary

- 64-bit architecture
- 8-, 16-, 32- and 64-bit integers
- 32 bit instructions
- VAX F and G floating point formats
- IEEE S and T floating point formats
- Virtual address 43 bits
- Physical address 34 bits
- Issue rate -- 2 instructions per cycle
- Translation buffer, 32 data, 12 instruction (fully associative)



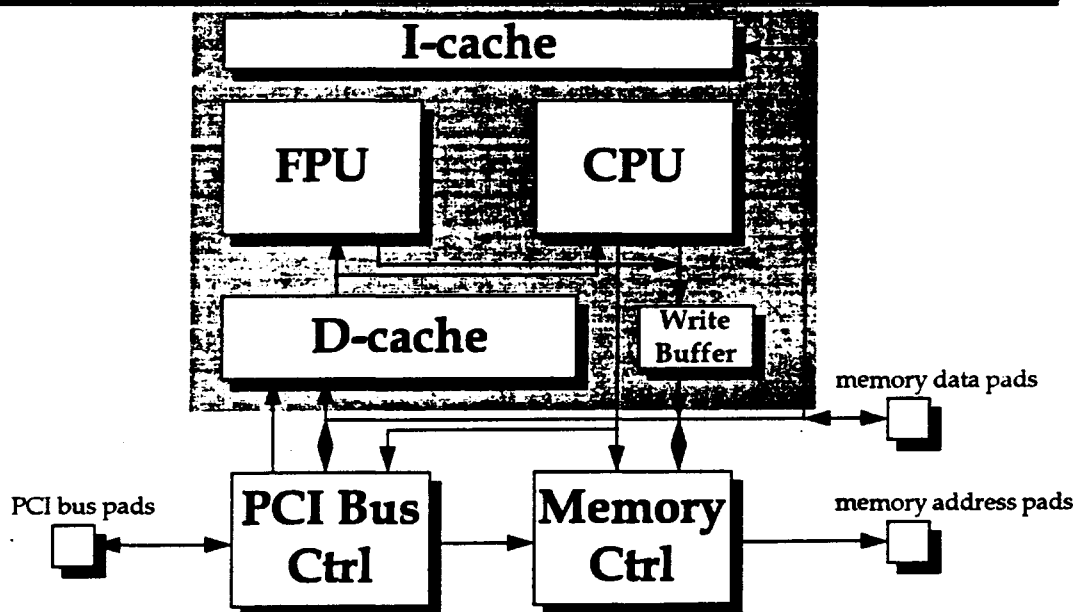
Primary Caches

- 8 KB instruction
- 8 KB data
- Direct mapped
- 32 byte block size

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Internal block diagram



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On-chip memory controller: DRAM and VRAM

- Direct control of all DRAM control signals - only electrical buffering required
- 1 to 4 banks - 2 MB minimum to 512 MB maximum
- Fully programmable timing on per-bank basis
- Optional ECC on per bank-basis
- Graphics hardware for dumb frame buffer assist

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On-chip memory controller: External cache

- 64KB to 2MB (cache size independent of memory size)
- Direct mapped, write-back, block size 8 bytes
- Fully programmable read and write timing
- Cache may be skipped based on physical memory address
- Optional ECC
- Optional tag parity

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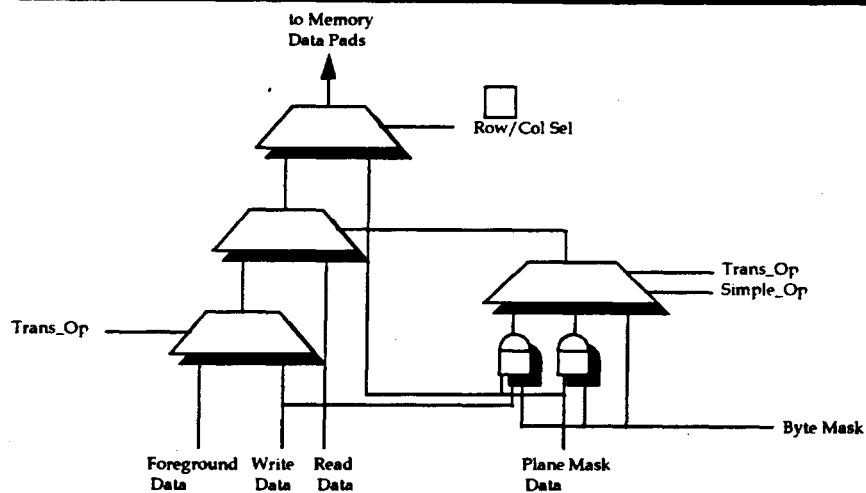
On-chip memory controller: Graphics hardware

- Plane masking
- Stipple operation
- Write-per-bit memory support
- VRAM Data Transfer cycles in response to monitor timing

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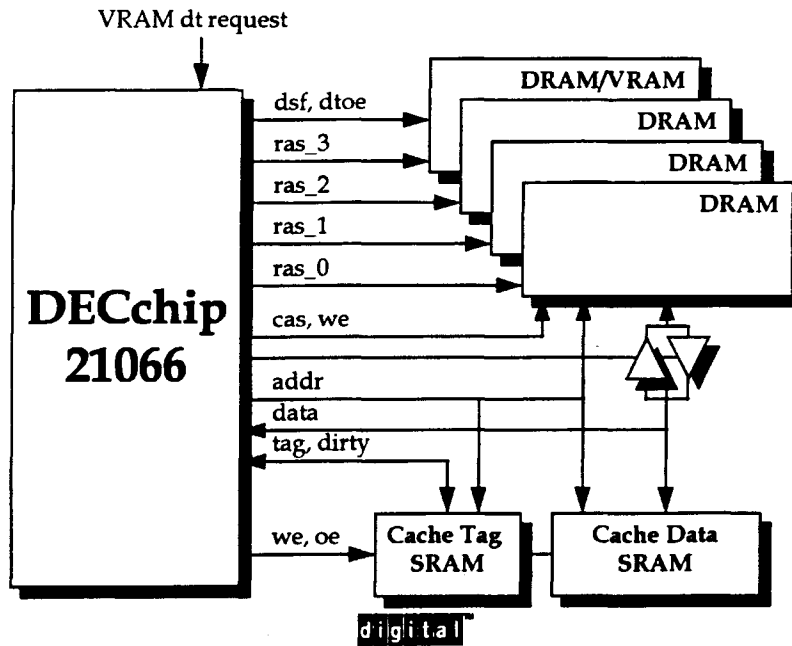
On-chip memory controller: Graphics hardware block diagram



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Memory block diagram



Memory Bandwidth

	I-read	D-read	D-write
Internal Cache	1.3 Gbyte/s	1.3 Gbyte/s	1.3 Gbyte/s
External Cache	149 Mbyte/s	183 Mbyte/s	84 MByte/s
Memory	44 Mbyte/s	47 Mbyte/s	83 MByte/s

Note: 166 MHz, 64 bits/access



PCI Bus

- 32/64-bit multiplexed address and data
- Fully synchronous operation up to 33 MHz
- Burst mode supported for programmed IO and DMA
- Separate initiator and target ready signals
- Symmetric bus mastering
- Byte and word access supported
- Separate configuration space used for initialization

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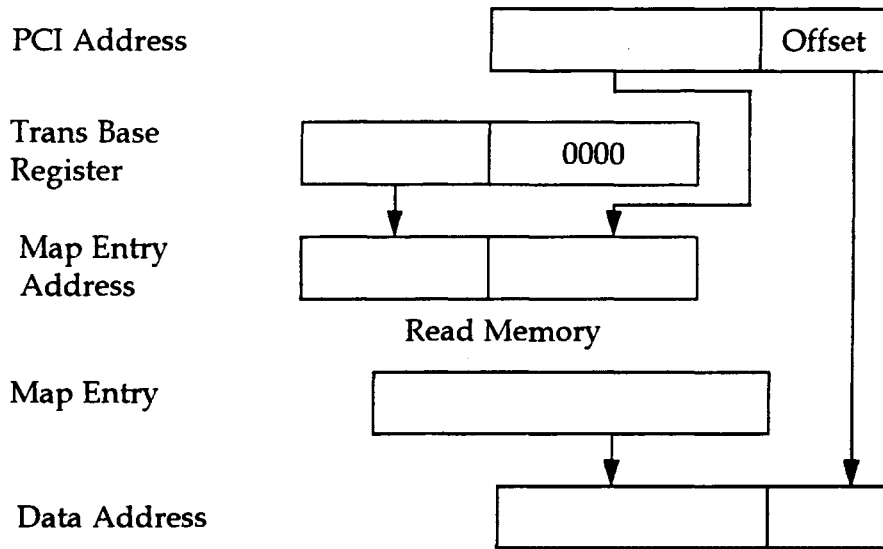
On-chip PCI Bus controller

- Asynchronous to CPU to allow for flexible design options
- Optional scatter-gather map stored in memory
 - 8-entry on-chip scatter-gather entry buffer
- Write buffering
- Read prefetching
- Memory request protocol to support ISA bus bridge

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PCI to memory address translation



On chip phase-locked loop

- Allows use of inexpensive oscillator
- Multiplier range is selected at chip reset



Summary

■ The DECchip 21066 offers...

- Alpha AXP architecture
- Integration of memory and PCI
- Ease of system design

■ Chip features...

- Process - .675 um, 3 metal layers
- 12.3 x 17.0 mm
- 1,746,892 transistors
- 166 MHz
- 3.3 V power supply

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