August 8, 1993 — Memorial Auditorium

SUNDAY

Sunday Tutorial Schedule

7:30 – 8:30	Registration & Coffee at Memorial Auditorium
8:30 – 12:00	Cache Memories Tutorial, Alan J. Smith
12:00 – 1:00	Lunch
1:00 – 4:30	DRAM Choices for the 1990s, Steven Przybylski
4:30 – 6:30	Wine & Cheese Reception in the Dohrmann Grove just north of the Hoover Tower on Serra Street

CACHE MEMORIES

Alan J. Smith, UC Berkeley

This tutorial will survey the design and design considerations for cache memories. Specific topics discussed will include: fetch, placement and replacement algorithms, line size, cache size, store through vs. copy back updating of memory, cold start vs. warm start miss ratios, multicache consistency, virtual address caches, user/supervisor caches, split instruction/data caches, multilevel caches, translation lookaside buffers, and the effect of I/O through the cache.

DRAM CHOICES FOR THE 1990s

Steven Przybylski, Consultant

This tutorial will summarize the strengths and weaknesses of each of the emerging DRAM alternatives: Synchronous DRAM, Cache DRAM, Enhanced DRAM, Rambus DRAM, and Ramlink DRAM. The discussion will show which DRAM markets will be best served by each architecture, why these changes are occurring now, and what further changes can be expected as the industry moves toward the 64M bit level and beyond.

Additional On-Site Registration will be available for an hour before the sessions begin on Monday and Tuesday.

August 9, 1993 — Memorial Auditorium

8:45 – 9:00 **Welcome and Opening Remarks**
John Hennessy, General Chair
Ruby Lee and Teresa Meng, Program Co-Chairs

9:00– 11:00 **Session 1: High Integration**
Session Chair: Ruby Lee, Hewlett-Packard Co.

- **DECchip 21066 - Alpha AXP Architecture Processor for Low-Cost Applications**
  Mark Rosenbluth, Digital Equipment Corp.
- **ICE: A high-performance MIPS microprocessor for portables**
  Barbara Zivkov, MIPS Technologies Inc.
- **Hummingbird: A Low-Cost Superscalar PA-RISC Processor**
  Stephen R. Undy, et al, Hewlett-Packard Co.
- **Optimized Pentium™ Processor 82430 PCIset for High Performance Local Bus Designs**
  Dale Jorgensen, Intel Corp.

11:00 – 11:30 **Break**

11:30 – 12:30 **Session 2: Portable Communications**
Session Chair: Teresa Meng, Stanford University

- **An Integrated Solution to CT2 Digital Cordless Telephones**
  David Norris, Alan Hendrickson, Advanced Micro Devices
- **CDMA Mobile Station Modem ASIC**
  Timothy Rueth, Qualcomm Incorporated

12:30 – 2:00 **Lunch**

2:00 – 3:30 **Session 3: Glowing Hot Chips**
Session Chair: John Mashey, Silicon Graphics, Inc.

- **A 300MHz 115W 32b Bipolar ECL Microprocessor with On-chip Caches**
  Norman P. Jouppi, et al, Digital Equipment Corp. Western Research Lab.
- **The Aurora Project**
  Mike Upton, Tom Huff, Trevor Mudge, Rich Brown, University of Michigan
- **MasPar MP-2 PE Chip: A Totally Cool Hot Chip**
  Won Kim and Russ Tuck, MasPar Computer Corp.

3:30 – 4:00 **Break**

4:00 – 5:30 **Session 4: Graphics Processors**
Session Chair: Robert Garner, Sun Microsystems, Inc.

- **A Single-Chip Workstation Graphics System**
  Larry J. Thayer, Hewlett-Packard Co.
- **Compact 3D Graphics Chip Set**
  Michael Deering, Sun Microsystems
- **A 200 Mpixels/sec Graphics Accelerator with Multimedia Expansion**
  Jacques Martinella, Weitek Corporation

5:30 – 7:00 **Reception Dinner**

7:15 – 9:30 **Evening Panel Session**
Compelling Applications for Computing in the Year 2000
Moderator: David Liddle, Interval Research
Panelists: Paul Allen, Asymetrix; Forest Baskett, Silicon Graphics; Gordon Bell, Consultant; Richard Rashid, Microsoft; Wayne Rosing, First Person

Program Committee

Co-Chairs: Ruby Lee, Hewlett-Packard and Teresa Meng, Stanford University

Donald Alpert, Intel Corp.
Robert Garner, Sun Microsystems, Inc.
John Mashey, Silicon Graphics, Inc.
Peter Ruetz, SiArc
Alan J. Smith, UC Berkeley

HOT CHIPS V

August 10, 1993 — Memorial Auditorium

9:00 – 10:30 **Session 5: Video Processors**
Session Chair: Peter Ruetz, SiArc

- **A Single Chip Multistandard Video Codec**
  Subroto Bose, Steve Purcell and Tony Chiang, C-Cube Microsystems
- **The Multiprocessor Video Processor, MVP**
  Karl Guttag, Texas Instruments
- **A Family of MPEG Video Encoder and Decoder Chips Optimized for Consumer Applications**
  Martin Bolton, SGS-Thomson Microelectronics, France

10:30 – 11:00 **Break**

11:00 – 12:00 **Session 6: Design Validation**
Session Chair: Donald Alpert, Intel Corp.

- **Pre-Silicon Validation of Pentium™ CPU**
  Azam Barkatullah, Wern-Yan Koe, Harish Nayak, Nazar Zaidi, Intel Corp.
- **System Design Verification of the HP735 VLSI**
  Gregory Burroughs and Alan Wiemann, Hewlett-Packard Co.

12:00 – 1:30 **Lunch**

1:30 – 3:30 **Session 7: New Technology**
Session Chair: Teresa Meng, Stanford University

- **AMULET1 - An Asynchronous ARM Processor**
  S. B. Furber, University of Manchester, UK
- **Pushing The Limits of CMOS Technology: A Wave-Pipelined Multiplier**
  Fabian Klass, Michael Flynn, and Ad J. Van de Goor
  Stanford University and Delft University
- **A 40,000 Pattern/s Classification Coprocessor with Learning Capability**
  Chin Park, et al, Intel Corp.
- **Stanford Ultra Low Power CMOS**
  Jim Burr, Stanford University

3:30 – 4:00 **Break**

4:00 – 5:30 **Session 8: High Performance Processors**
Session Chair: Alan J. Smith, University of California, Berkeley

- **A 120 MHz BiCMOS Superscalar PA-RISC Processor**
  Kenji Matsubara, Hitachi, Ltd., Japan
- **601 PowerPC Microprocessor**
  Keith Diefendorff, Motorola, Inc.
- **Silicon Graphics TFP Micro-Supercomputer Chipset**
  Peter Yan-Tek Hsu, Silicon Graphics Computer Systems

5:30 **Closing Remarks**

Organizing Committee

General Chairman: John Hennessy, Stanford University

Program Co-Chairs:
Ruby Lee, Hewlett-Packard
Teresa Meng, Stanford University

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