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# The P5 Floating-Point Unit

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## Agenda

- Design Goals
- Micro-Architecture Overview
- Register-Stack Manipulation
- Transcendental Functions
- Compiler Optimization
- Summary

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# Design Goals

- Architectural Compatibility
  - Full Compatibility with Intel486™ CPU
  - IEEE Standard 754
- High Performance
  - 4-10 Times Intel486™ DX 33MHz CPU

4-5 on SCALAR
6-10 on VECTORIZABLE CODE



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# Micro-Architecture Overview

## Floating Point Pipeline

- Three Dedicated Arithmetic Units
- Eight Stage Pipeline

FP EXECUTION

Integer Pipe: PF D1 D2 E WB

FP Pipe: PF D1 D2 E X1 X2 WF ER

- Three Execution Stages

OPERAND FETCH (ALF MEM)

ERROR REPORT

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# Micro-Architecture Overview

## Floating Point Pipeline Characteristics

- One Cycle Throughput
- Execution in U-Pipe
- U-Pipe and V-Pipe Used to Access Data Cache
- Concurrent Data Cache Access and FP Computation
- Tuned for Double Precision Memory-Register Operations



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# Micro-Architecture Overview

## Safe Instruction Recognition

- Early Detection of Potential Exceptions

Example:

**FMULP Recognized as Safe**

| | | |
|---|---|---|
| Cycle 1 | → | FMULP ST (2), ST |
| Cycle 2 | → | FADD QWORD PTR [EAX] |

**FMULP Recognized as Unsafe**

| | | |
|---|---|---|
| Cycle 1 | → | FMULP ST (2), ST |
| Cycle 2 | → | 0 |
| Cycle 3 | → | 0 |
| Cycle 4 | → | 0 |
| Cycle 5 | → | FADD QWORD PTR [EAX] |

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# Micro-Architecture Overview

## Arithmetic Units

- Multiplier
  - Full Extended Precision Multiply Array
  - Three Cycles Latency for All Precisions
  - Support for Integer Multiplication
- Adder
  - Execution of Majority of Basic Instructions
  - Three 71-Bit Adders
  - Two 69-Bit Shifters
  - Three Cycles Latency for All Precisions
- Divider
  - Divide, Remainder and Square-Root Operations
  - SRT Algorithm



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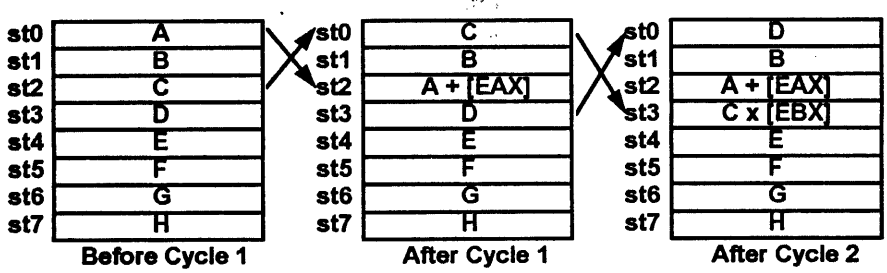
# Register Stack Manipulation

- Instruction Set Uses Top of Register Stack as Accumulator
- Parallel Execution of FXCH

Example:
Cycle 1 → FADD QWORD PTR [EAX] | FXCH ST (2)
Cycle 2 → FMUL QWORD PTR [EBX] | FXCH ST (3)



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# Transcendental Functions

- Direct Microcode Support for All Architecturally Defined Transcendental Instructions:
  - Sine
  - Cosine
  - Sine-and-Cosine
  - Tangent
  - Arctangent
  - $2^x - 1$
  - $Y \times \log_2 X$
  - $Y \times \log_2(X + 1)$
- Table Driven Algorithms Using Polynomial Approximation
- Performance and Error Bound Improvement over Intel486™ DX 33MHz CPU
- Comprehensive Validation Program

4-6X 33MHz 486

410M TEST CASES BEFORE SILICON



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# Compiler Optimization

- Instruction Scheduling
- Register Allocation
- Loop Unrolling
- Parallel FXCH

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# Summary

- Streamlined Pipeline Provides High Performance
  - Integration with Integer Pipeline
  - One Cycle Throughput
  - Tuning for Memory-Register Double Precision Operations
- Fast Arithmetic Units Using State of the Art Algorithms
  - Multiplier
  - Adder
  - Divider
- Improved Performance and Accuracy of Transcendentals
- New Compiler Optimizations Co-Developed with Micro-Architecture