

# **SuperScalar Architecture of the P5 Intel's Next Generation Microprocessor**

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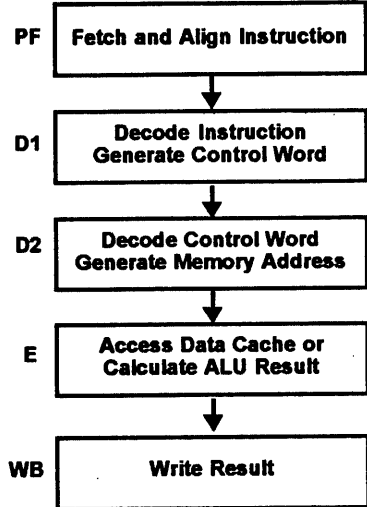
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## **Outline**

- **Integer Pipeline**
- **Superscalar Execution**
- **Branch Prediction**
- **Dual-Access Data Cache**
- **Compiler Optimizations**

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# Integer Pipeline

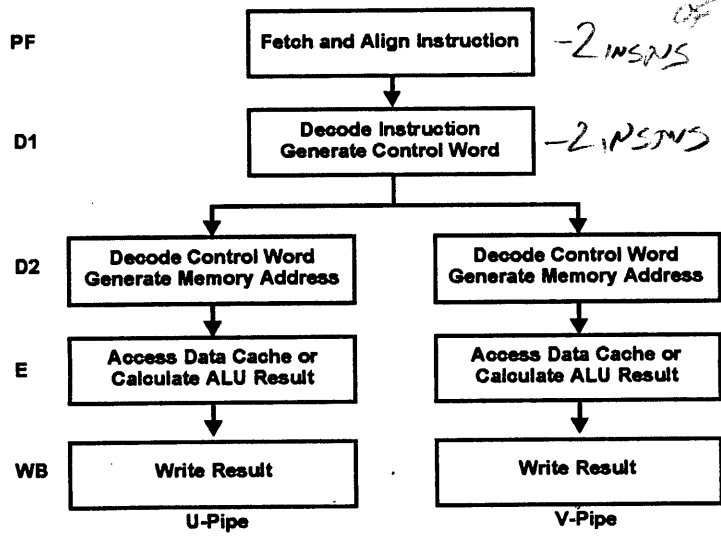


*- SPLIT INSTR, DATA*  
*-> 3M XTORS*  
*ARBITRARY*  
*MEMORY*  
*ARITHMETIC*

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# Superscalar Execution



*REPLICATED INST. OF INT PIPELINE*  
*- 2 INSTRS*  
*- 2 INSTRS*  
*RESOURCES AVAILABLE TO MAKE THE WORK FASTER*  
*10 STAGES*

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## Instruction Issue Algorithm

Decode Two Consecutive Instructions: I1 and I2  
If the Following Are All True

I1 Is a "Simple" Instruction

I2 Is a "Simple" Instruction

I1 Is Not a JUMP Instruction

Destination of I1 = Source of I2

Destination of I1 = Destination of I2

Then Issue I1 to U-Pipe and I2 to V-Pipe  
Else Issue I1 to U-Pipe

"Simple" Instructions Are Generally ALU or MOV Operations, Including Reg-Reg, Imm-Reg, Mem-Reg, and Reg-Mem Formats, and JUMPS

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90% of Dynamic Frequency

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DYNAMIC BENCHMARK

>100 MIPS  
@ 600 MHz

## Example

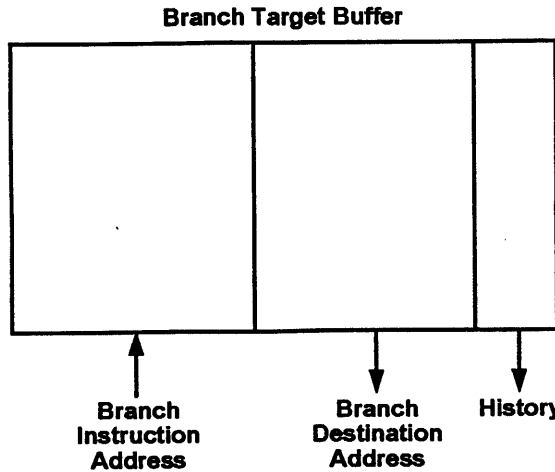
	U-Pipe	V-Pipe
Proc2:		
pushl	%ebx	movl %eax, %ecx
movl	(%ecx), %edx	
addl	\$10, %edx	movb Char1Glob, %ah
cmpb	\$65, %ah	jne .B4_4
decl	%edx	movl IntGlob, %eax
movl	%edx, %ebx	subl %eax, %edx
movl	%edx, (%ecx)	movl %ebx, %edx
.B4_4:		
popl	%ebx	
ret		

would know  
PAIR MEM  
MIPS

↑  
THIS BEING WHAT'S TYPICAL  
30%-50% PER SUPER SCALING  
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## Branch Prediction



COMPARE TARGET ADDRESS TO CACHE BRANCH TARGETS ADDRESS MISS

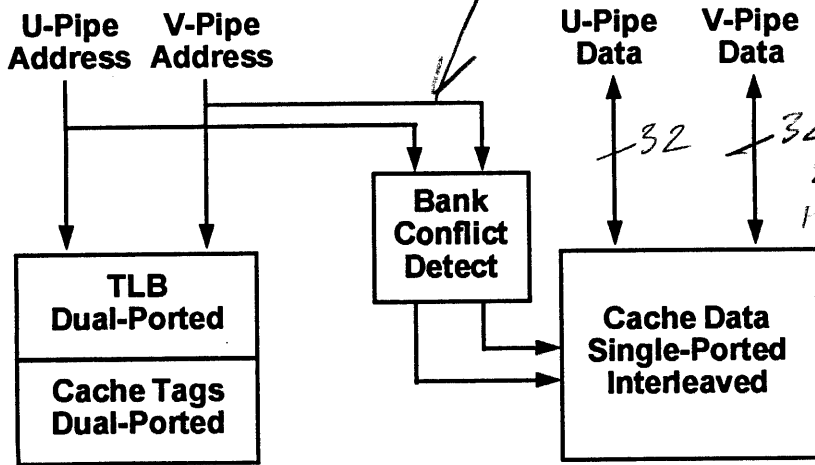
Correctly Predicted Branches Execute with No Delays

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NATURALLY HANDLES RAW, WAR CONFLICTS

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## Dual-Access Data Cache



0.6 DATA REFS/INSTN

COMBINED 64-BIT FP DATA

ICACHE 1MB DATA MISS

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CONTAINING IN HARDWARE

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## Compiler Optimization

- **Instruction Selection**
  - Use Simple Formats for Efficient Decoding
- **Instruction Scheduling**
  - Minimize Address Generation Interlocks
  - Maximize Parallel Execution
- **Register Allocation**
  - Schedule and Allocate Together to Make Best Use of Small Register Set

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*0.8µm Technology*

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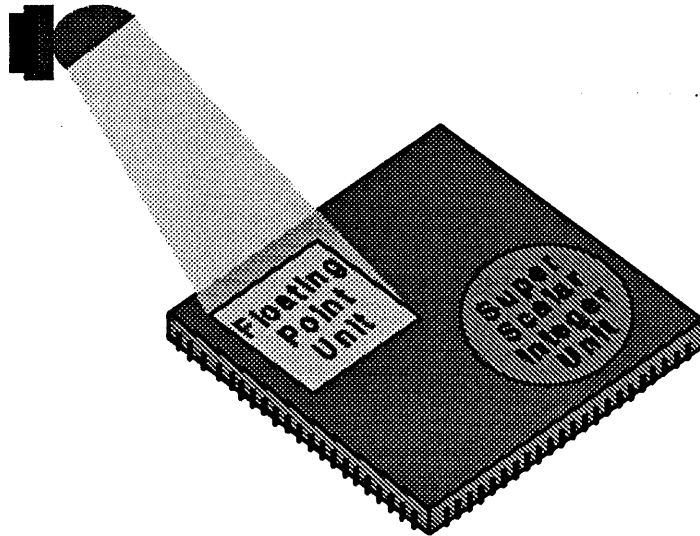
## Summary

- **Superscalar Microarchitecture**
  - Dual Integer Pipelines
  - Branch Target Buffer
  - Dual-Access Data Cache
- **Fully Compatible with Intel486™ CPU**

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