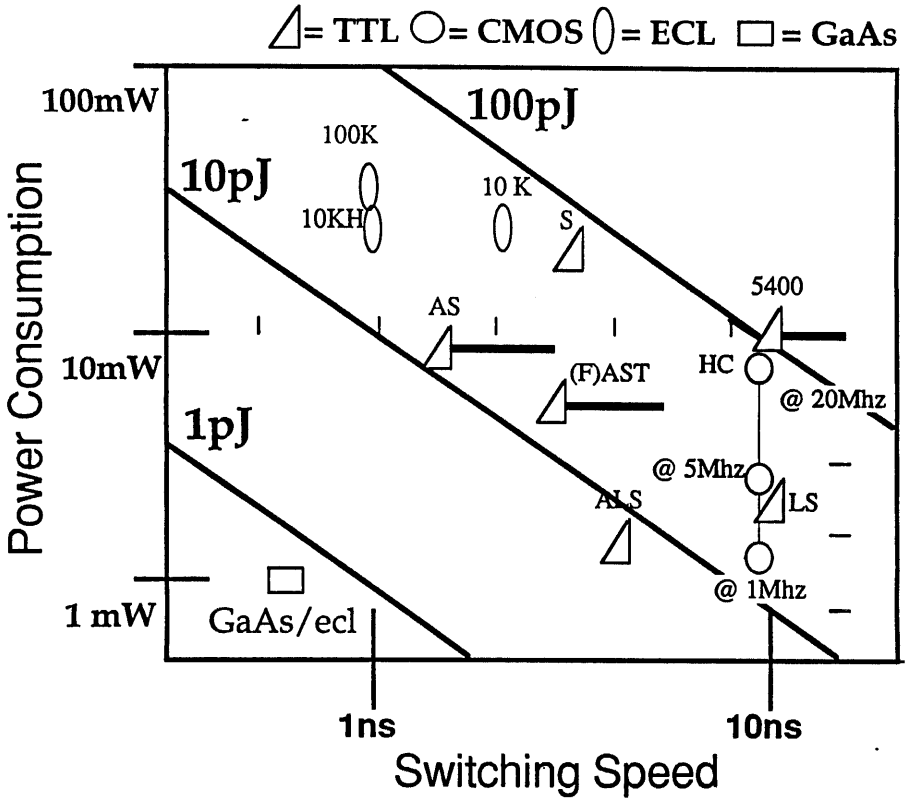
GaAs VLSI Enhancement through the Utilization of Global Optical Free Space "Smart" Interconnets

IEEE Hot Chips Symposium IV
Stanford University

Peter S. Guilfoyle and Frederick F. Zeise
OptiComp Corporation
Zephyr Cove, NV

OptiCompcorporation

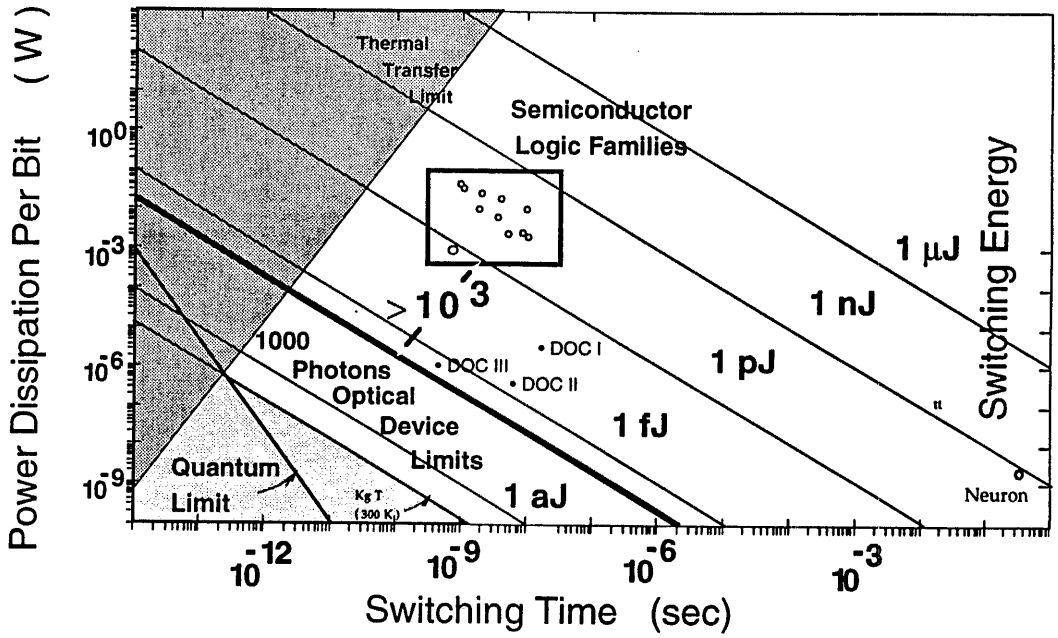
Logic Family Comparison



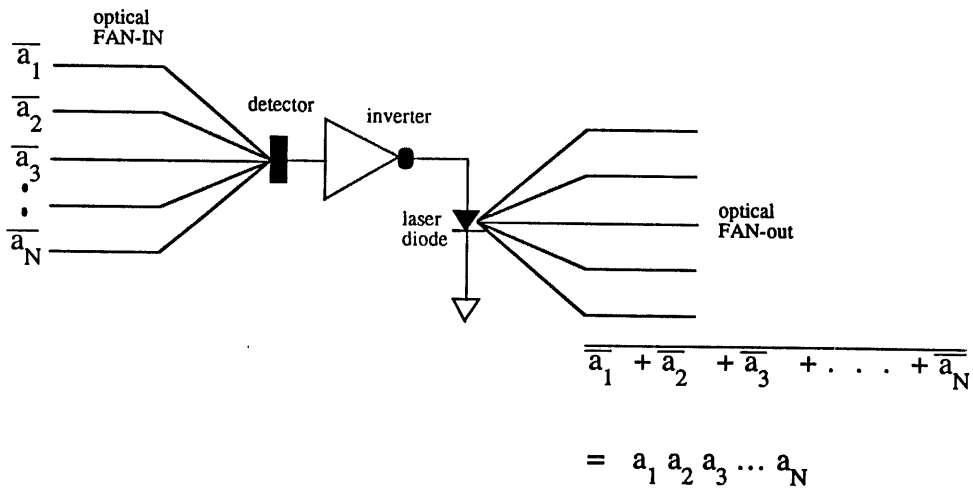
OptiCompcorporation

Digital photonic and electrical switching energies

(Power Dissipation vs. Switching Time)



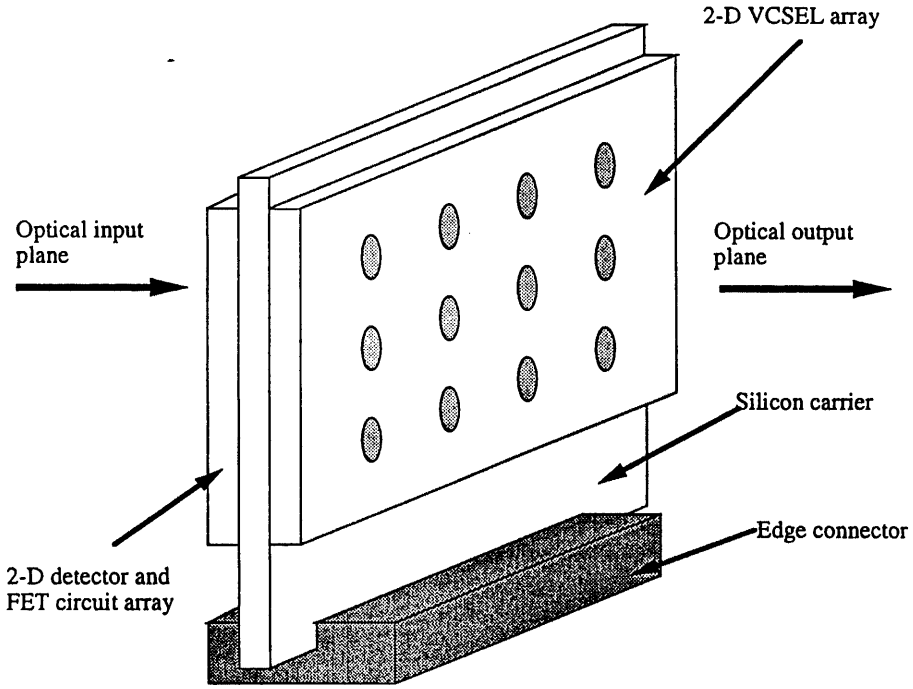
"Smart" Interconnect



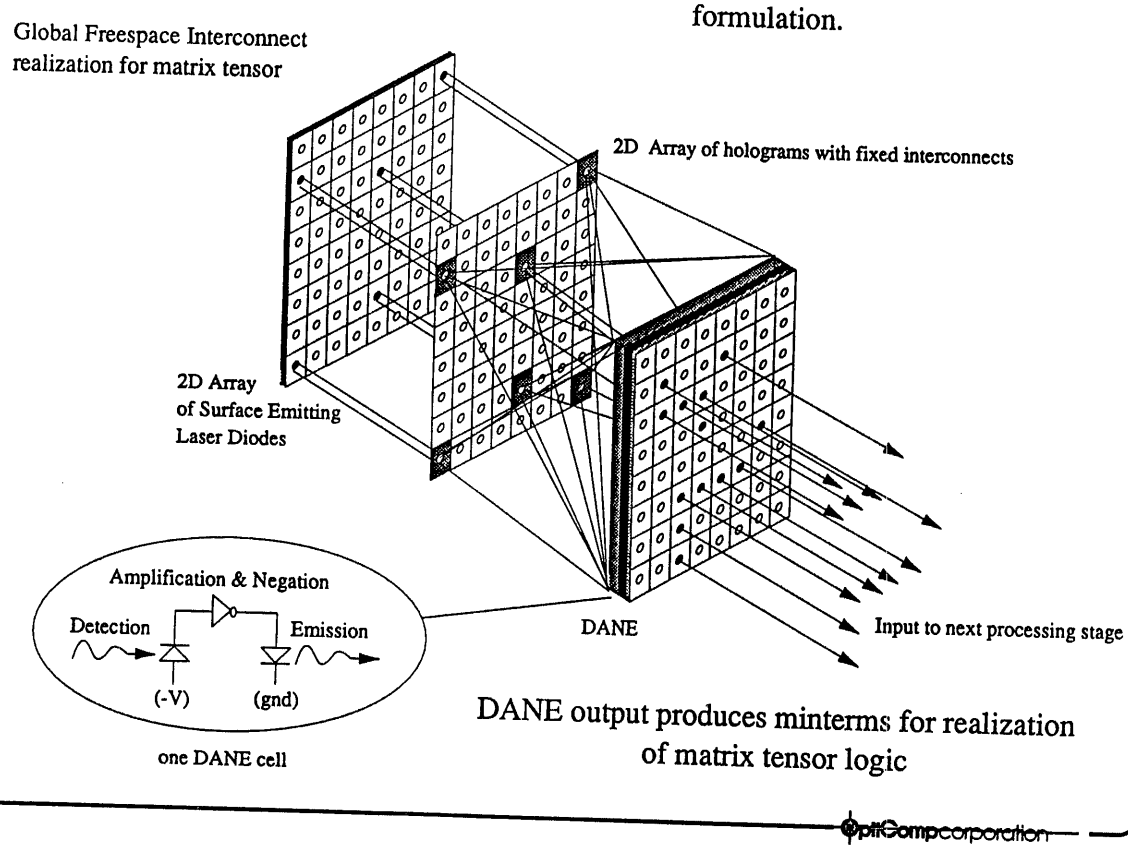
Detection Negation Amplification Emission (DANE) Specifications

Characteristic	Specification
Number of DANE cells	32 x 32
Optical gain	1,000
Electrical gain	10,000
Max fan-out	128
Threshold (detection)	-37dbm @10^{-18} BER or 0.2μW
Switching energy	< 1.2fJ
Gain characteristic	Limiting 1-bit
Min SNR (after fan-in)	13db
Min. optical output power/cell	0.2mW
Max power dissipation/cell	1W/cm^2
Max one cell size	0.1mm^2
Laser modulation	RTZ
Data rate	>400 MHz

2D DANE Subsystem

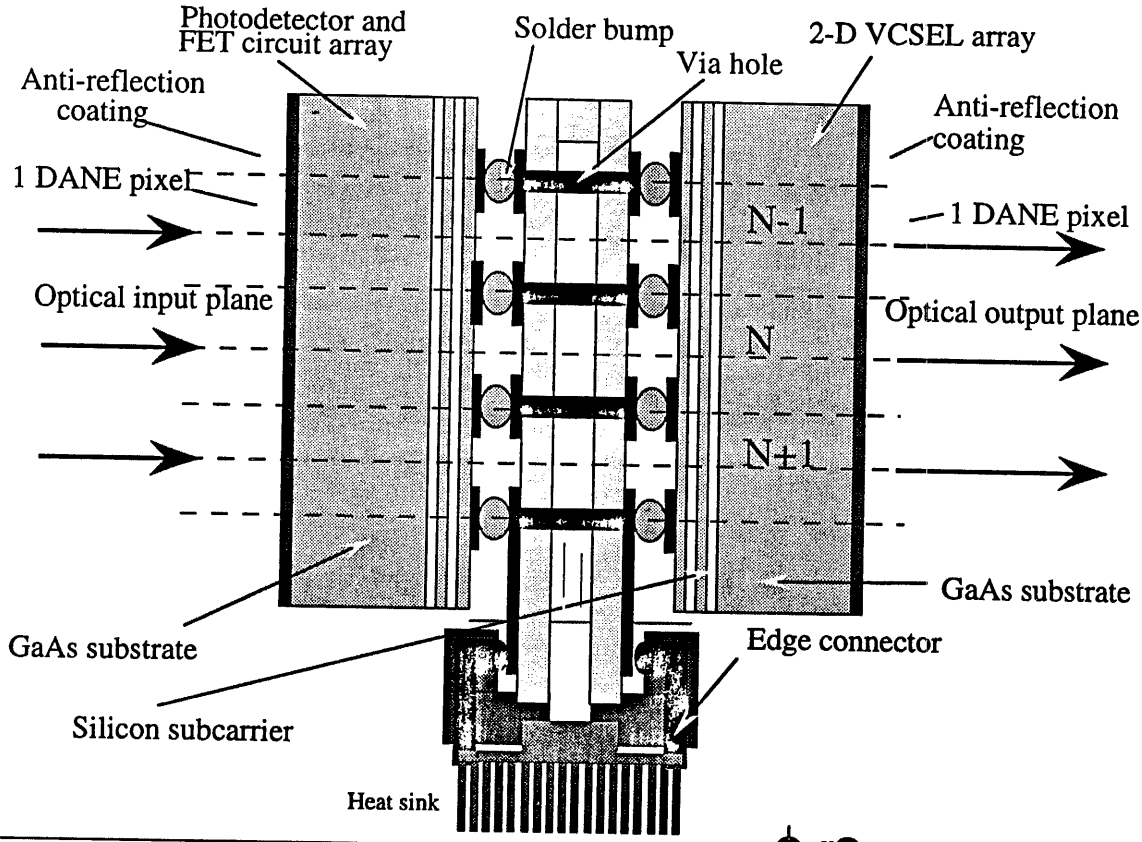


2 D single stage global free space interconnect minterm formulation.

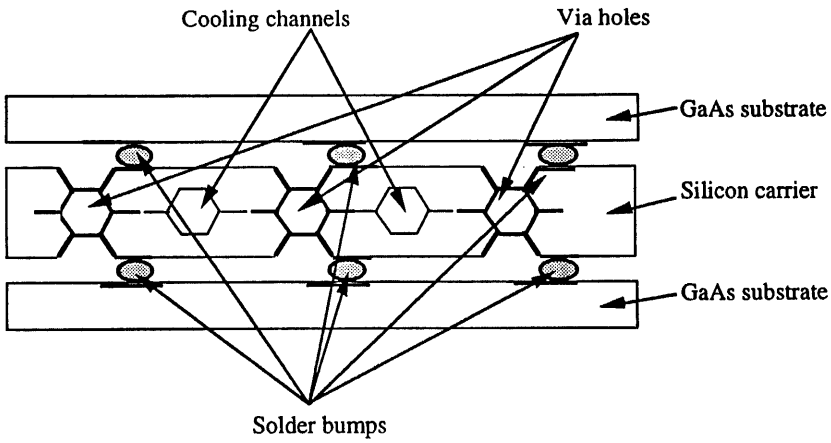


DANE output produces minterms for realization of matrix tensor logic

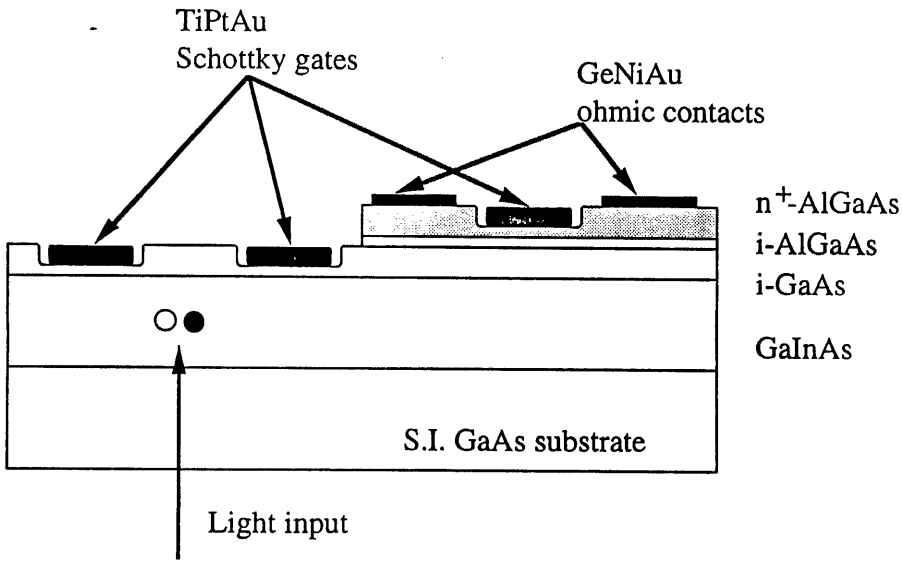
Cross-section of the 2-D DANE subsystem



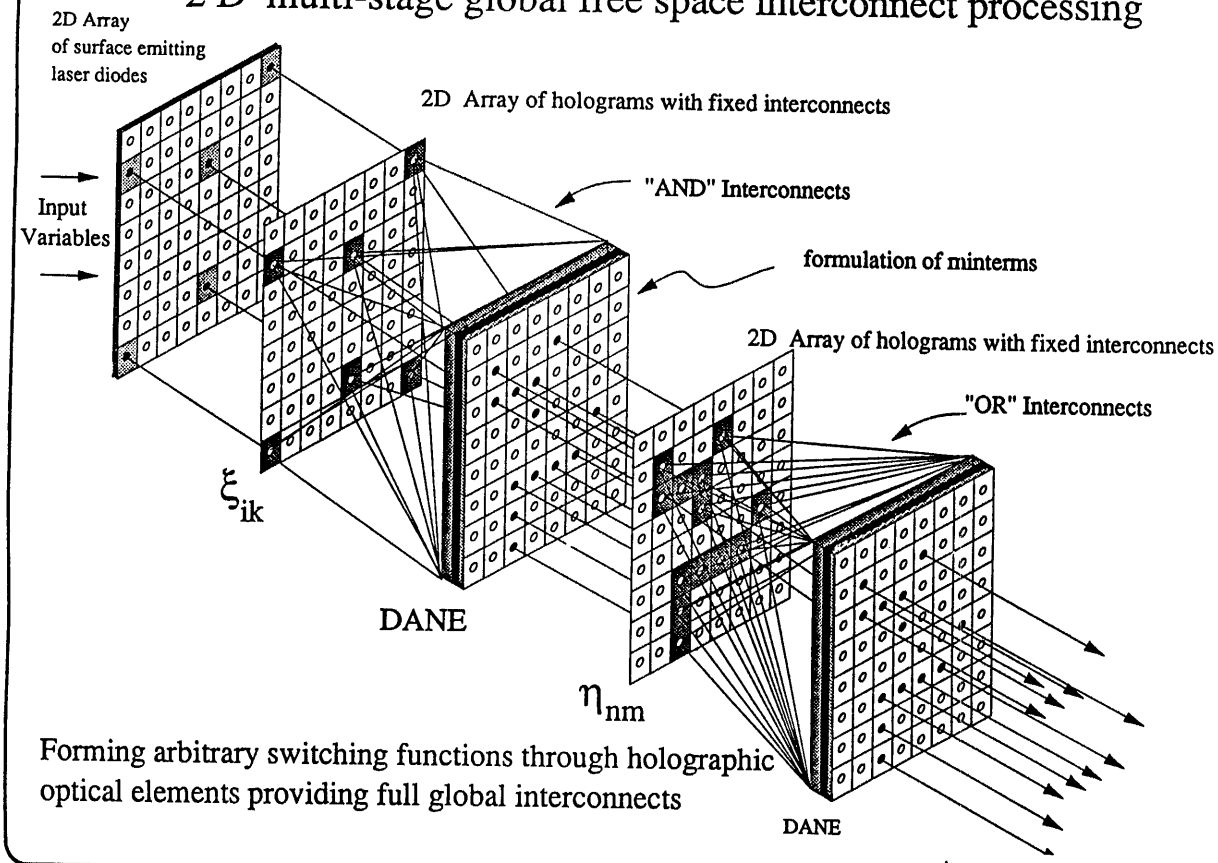
Cross-section of a silicon carrier showing cooling channels and via holes



Integration of GaAs Detectors with HEMTs



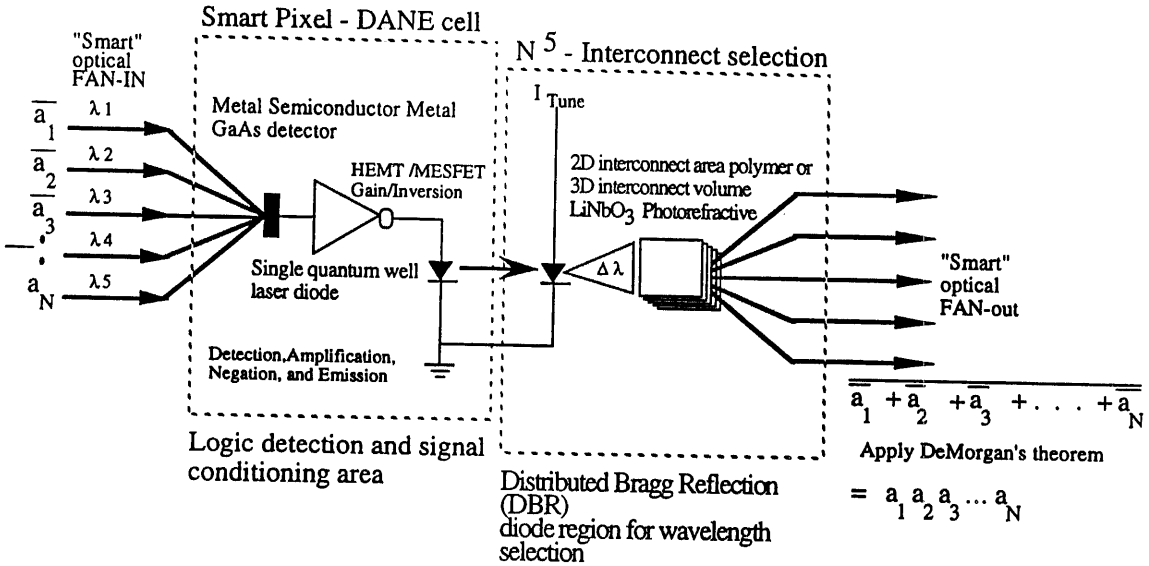
2 D multi-stage global free space interconnect processing

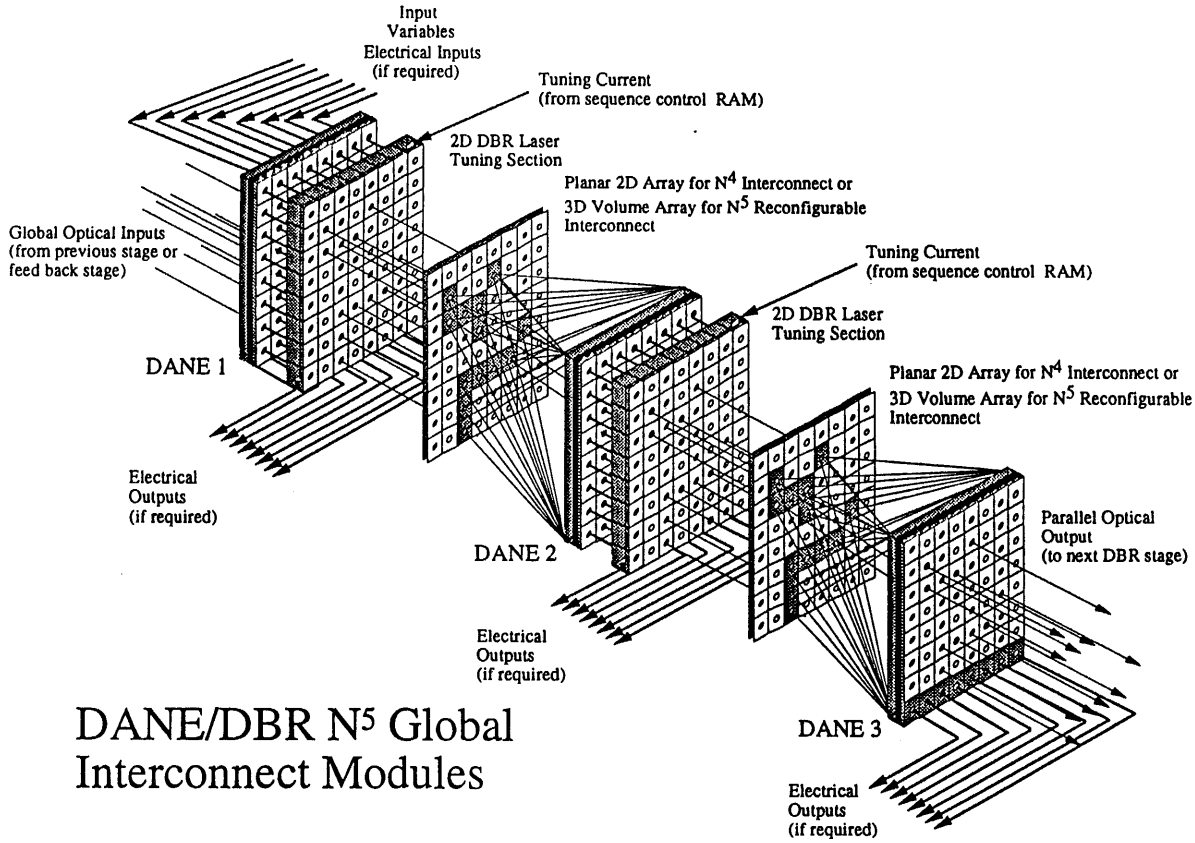


Forming arbitrary switching functions through holographic optical elements providing full global interconnects

OptiCompcorporation

Smart Pixel + N^5

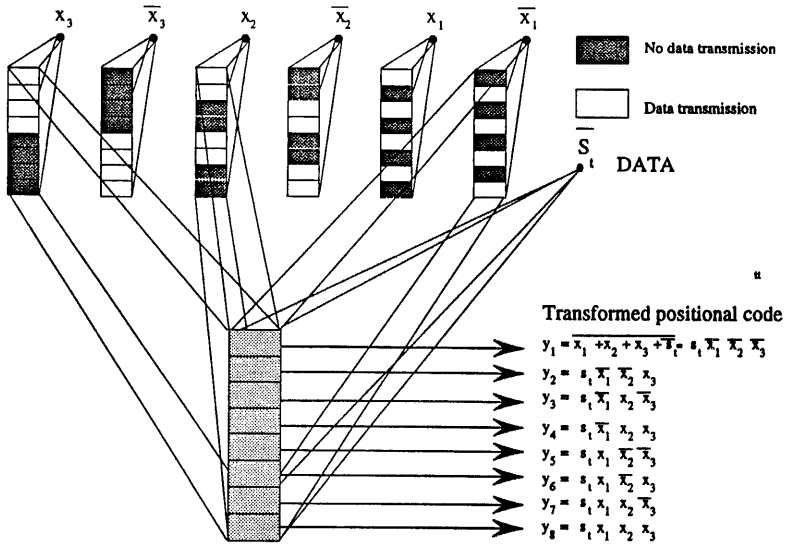




DANE/DBR N^5 Global Interconnect Modules

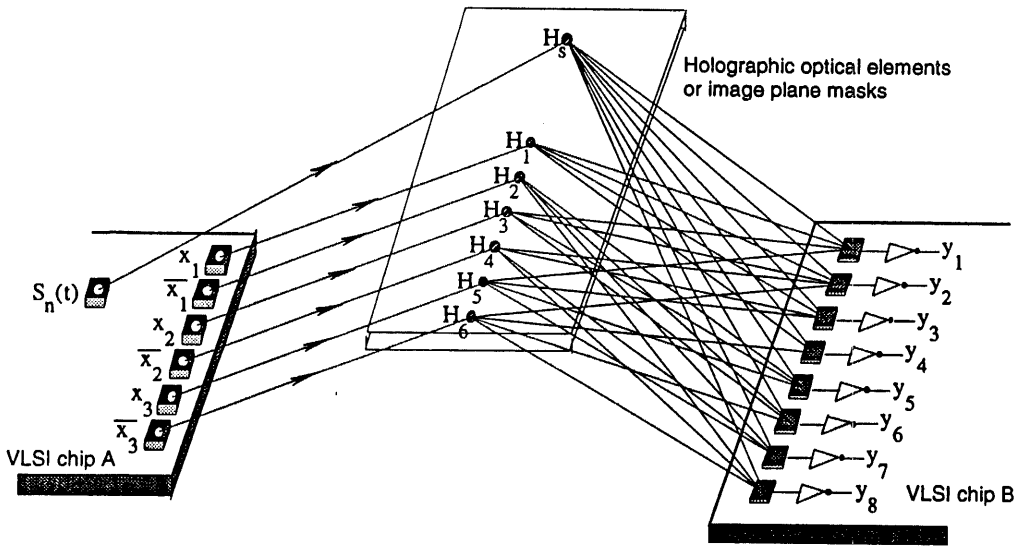
DANE Applications

"Smart" Holographic Intecrconnect for a 3:8 Decoder



Optical Multichip Modules

"Smart" chip-to-chip level interconnects with optical bus and address decode



Addition - [$\tau = 1\Delta$ T (one clock / cycle)]

Addition - (one clock) Optical Free Space Global Interconnect Primitive Implementation.

$A = A_{n-1}, A_{n-2}, \ldots A_i \ldots A_0$ A_{n-1}, B_{n-1} — Most Significant Bit (MSB)

$B = B_{n-1}, B_{n-2}, \ldots B_i \ldots B_0$ A_0, B_0 —— Least Significant Bit (LSB)

Step 1 - Calculate partial sum and partial carry (asynchronous,electronic)

$$P_k = A_k \oplus B_k \qquad G_k = A_k \bullet B_k$$

Step 2 - Calculate true look ahead carry (synchronous,optical)

$$C_m = G_m + \sum_{i=1}^{m} G_{m-i} \prod_{j=1}^{i} P_{m+i-j}$$

Step 3 - Calculate true summation (synchronous,electronic)

$$S_m = P_m \oplus C_{m-1}$$

OpticComp corporation

Global Addition

OpticComp corporation

Addition - Partial carry for 5 bit addition:

$C_{11}=G_0$	$C_{12}=0$	$C_{13}=0$	$C_{14}=0$	$C_{15}=0$
$C_{21}=G_1$	$C_{22}=G_0 P_1$	$C_{23}=0$	$C_{24}=0$	$C_{25}=0$
$C_{31}=G_2$	$C_{32}=G_1 P_2$	$C_{33}=G_0 P_1 P_2$	$C_{34}=0$	$C_{35}=0$
$C_{41}=G_3$	$C_{42}=G_2 P_3$	$C_{43}=G_1 P_2 P_3$	$C_{44}=G_0 P_1 P_2 P_3$	$C_{45}=0$
$C_{51}=G_4$	$C_{52}=G_3 P_4$	$C_{53}=G_2 P_3 P_4$	$C_{54}=G_1 P_2 P_3 P_4$	$C_{55}=G_0 P_1 P_2 P_3 P_4$

True carry $C_i = \sum_k C_{ik}$

Total number of interconnects for lookahead carry $9 \times 5^2 = 225$

Total number of active interconnects for lookahead carry $9 \times 15 = 135$

Addition - Optical Free Space Global Interconnect Primitive Implementation.

$$C_m = G_m + \sum_{i=1}^{m} G_{m-i} \prod_{j=i}^{i} P_{m+i-j}$$

General Expression:

$C_0 = G_0$

$C_1 = G_1 + G_0 P_1$

$C_2 = G_2 + G_1 P_2 + G_0 P_1 P_2$

$C_3 = G_3 + G_2 P_3 + G_1 P_2 P_3 + G_0 P_1 P_2 P_3$

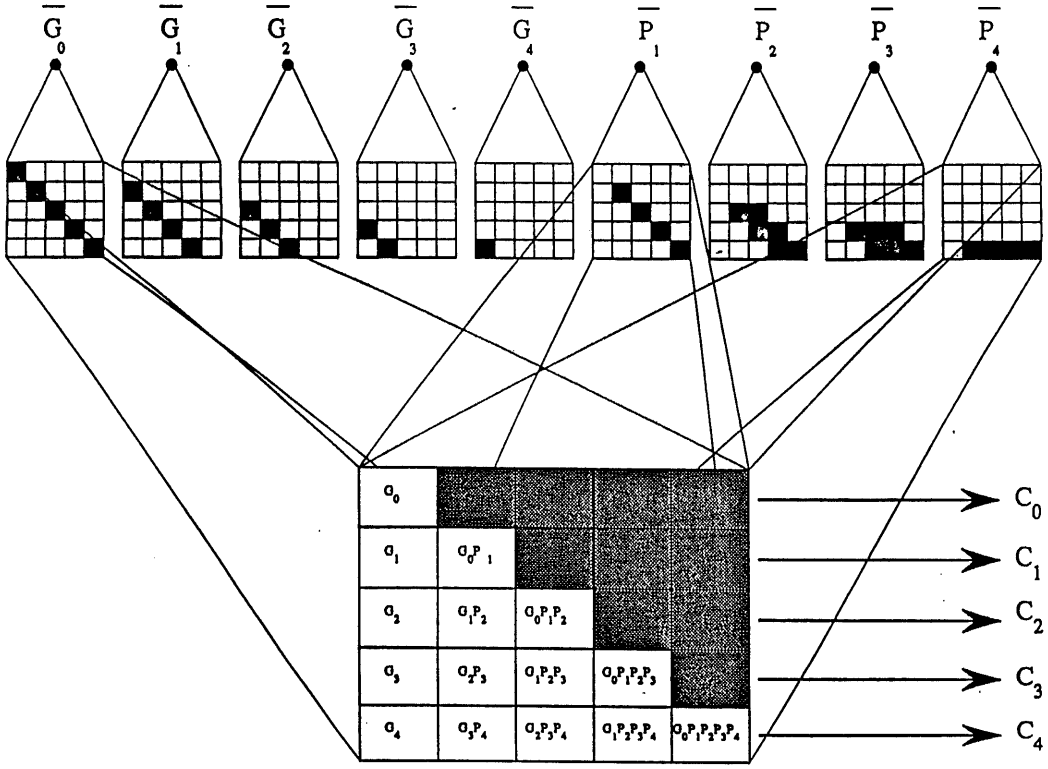
•
•
•

$C_{i-1} = G_{i-1} + G_{i-2} P_{i-1} + G_{i-3} P_{i-2} P_{i-1} + \ldots + G_0 P_1 P_2 \ldots P_{i-1}$

$C_i = G_i + G_{i-1} P_i + G_{i-2} P_{i-1} P_i + \ldots + G_1 P_2 P_3 \ldots P_i + G_0 P_1 P_2 P_3 \cdots P_i$

$C_{i+1} = G_{i+1} + G_i P_{i+1} + G_{i-1} P_i P_{i+1} + \ldots + G_2 P_3 P_4 \ldots P_{i+1} + G_1 P_2 P_3 \cdots P_{i+1} + G_0 P_1 P_2 \ldots P_{i+1}$

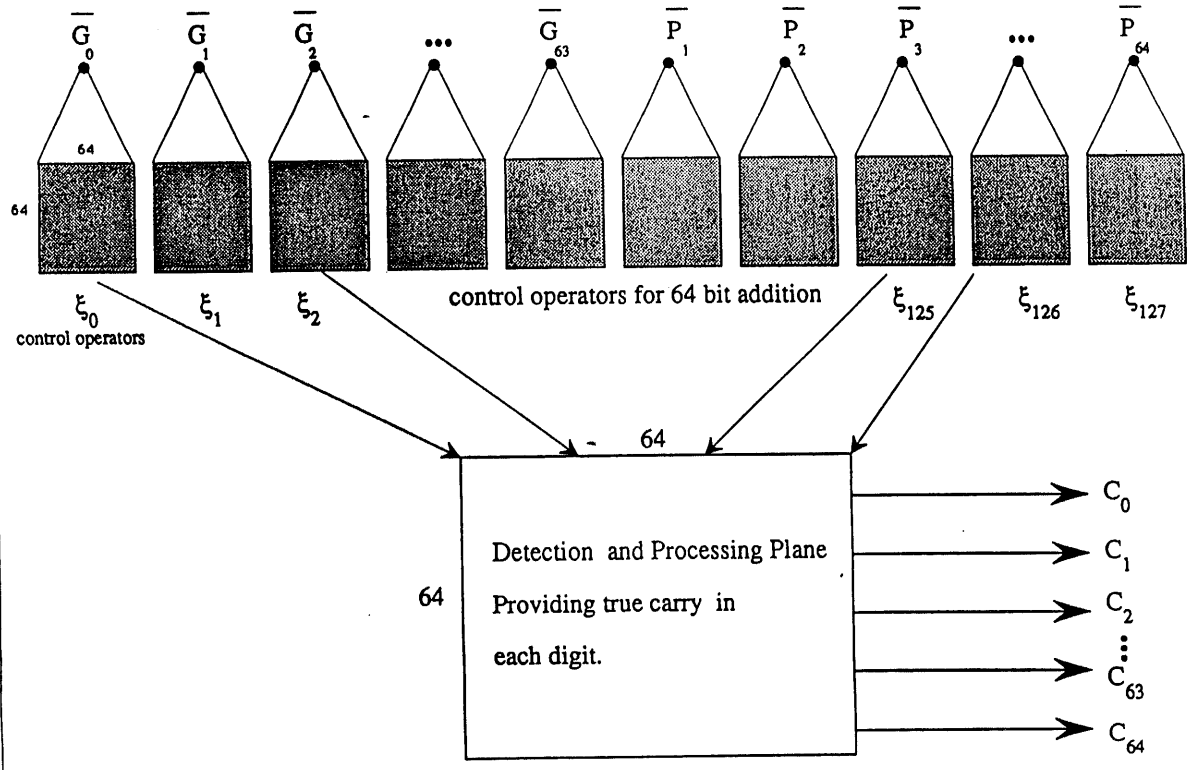
Addition
Example for 5bit addition



Processing (Inversion, OR- ing) Photodiode matrix

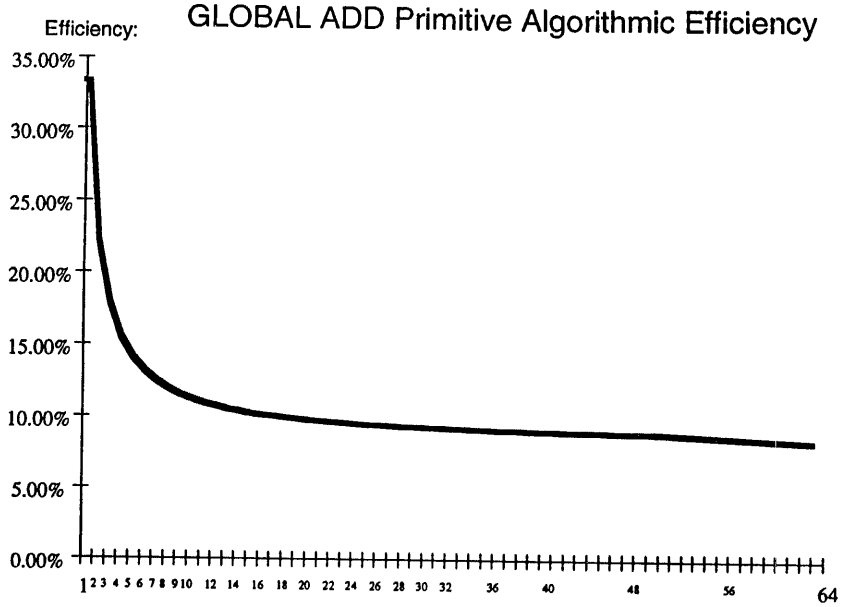
OptiCompcorporation

Addition
Example for 64 bit addition



Photodiode matrix

OptiCompcorporation



OptiCompcorporation

Summary

Primary Benefits

- Low Power
- Low BER ($<10^{-18}$)
- Smart pixels (high fan-in and fan-out)
- High algorithmic efficiency through increased fan-in

Secondary Benefits

- No capacitve loading: fan-in limited only by contrast ratio
- No signal dispersion
- No signal skew
- No cross talk between channels

OptiCompcorporation