# Fujitsu MB92831

The first member of Fujitsu's μVP Series of vector coprocessors.


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Local Knowledge FUJITSU

- Local Knowledge is providing Fujitsu with English language technical support. Local Knowledge is also writing a series of manuals that describe the μVP Series.
- The MB92831 was designed at Fujitsu's R&D facility in Kawasaki, Japan (near Tokyo). The principle designers were: Hideyuki Iino, Hiromasa Takahashi, Takao Sukemura, Masaharu Kimura, Koichi Fujita, and Shosuke Mori. Mr. Takahashi works for Fujitsu Labs. Everyone else works for the Semiconductor Group within Fujitsu Limited.
- The μVP technology was introduced at ISSCC last February. The MB92831 was announced in late June. Several design wins exist in both the U. S. and Japan.



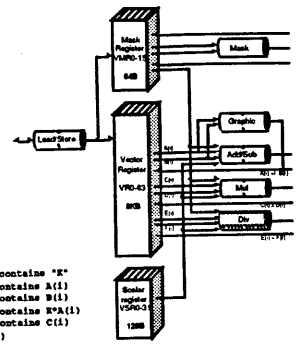


## Programming Model

```
FORTRAN Source
      DO 10 i=1,n
      10 C(i) = K * A(i) + B(i)

μVP Source
      ; VLEN   = vector length "n" (256 max)
      ; VBR31  = address of "K"
      ; VBR30  = base address of A(i)
      ; VBR29  = base address of B(i)
      ; VBR28  = base address of C(i)
      ; VBR27  = vector stride for A(i)
      ; VBR26  = vector stride for B(i)
      ; VBR25  = vector stride for C(i)
      VSLD64   VBR31, VBR0        ; VBR0 now contains "K"
      VLD64    VBR27, VBR30, VR0  ; VR0 now contains A(i)
      VLD64    VBR26, VBR29, VR8  ; VR0 now contains B(i)
      VMULSD   VR0, VBR0, VR0     ; VR0 now contains K*A(i)
      VADDD    VR0, VR8, VR0      ; VR0 now contains C(i)
      VST64    VR0, VBR25, VBR28  ; Store C(i)
```

The three underlined instructions are automatically executed in parallel

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- Fujitsu claims that a computer system containing a single 70 MHz MB92831 can execute the double precision LINPACK benchmark at 42.7 Mflops.
- A μVP is not a microprocessor. An external device must initialize its command buffer and tell it to start. An external device must handle all μVP exception conditions (unless they are masked off). A μVP cannot accept interrupts. It can only address 32 bit and 64 bit data aligned on 32 bit or 64 bit boundaries.
- Most embedded μVP design wins combine it with Fujitsu's SPARClite embedded microprocessor (because software support for the combination is available from the Portland Group). However, any microprocessor will work. If a μVP system contains a FORTRAN compiler, a "big-endian" microprocessor works best.
- The MB92831 has 141 vector instructions, 57 scalar instructions, and 8 general control instructions. The instruction set includes a scatter/gather (indirect addressing) vector load instruction.
- As demonstrated above, "chaining" is automatic.

## Process

| Part Number | MB92831-33ZF | MB92831-50ZF | Not Yet Available |
|---|---|---|---|
| Clock | 33 MHz | 50 MHz | 70 MHz |
| Single | 136 Mflops | 206 Mflops | 289 Mflops |
| Double | 70 Mflops | 106 Mflops | 149 Mflops |
| Memory | 264 Mb/sec | 400 Mb/sec | 560 Mb/sec |
| Power | 3 W | 4.5 W | Unknown |

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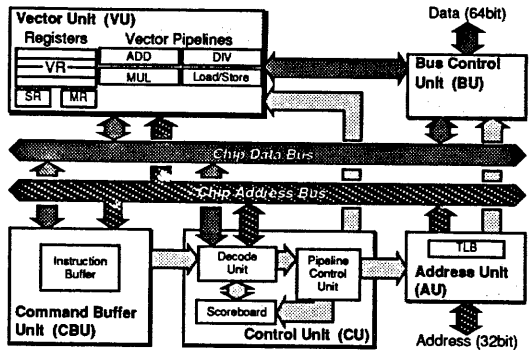
- The MB92831 is Fujitsu's first commercial application of its new 0.5 micron CMOS process. It uses three metal layers. The first two layers have a 2.1 micron pitch. The third layer has a 4.2 micron pitch.
- The MB92831 contains approxmately 1.5 million transistors on a die 15.99 mm by 15.99 mm.
- The µVP supply voltage is 3.3 volts.
- The MB92831 is available in a 256 pin, ceramic, SQFP with a lead pitch of 0.5 mm.
- All members of the µVP Series have an IEEE 1149.1-1990 standard test access port(the JTAG standard).

## Block Diagram

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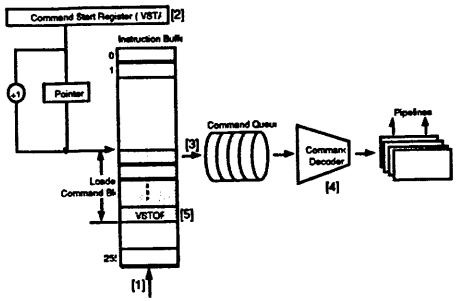
- Getting data into and out of the chip is a problem that all of the fast floating point chips share. The µVP architecture supports multiple load/store pipelines, a unique advantage. However, the first µVP chip, the MB92831, has only one load/store pipeline.
- With the exception of the vector and mask register sets, all other MB92831 registers can be accessed from the host microprocessor.
- System software cannot "context switch" a member of the µVP Series. Therefore, in time sharing systems, designers typically use between two and four µVP chips to each host microprocessor.

## Command Buffer Unit

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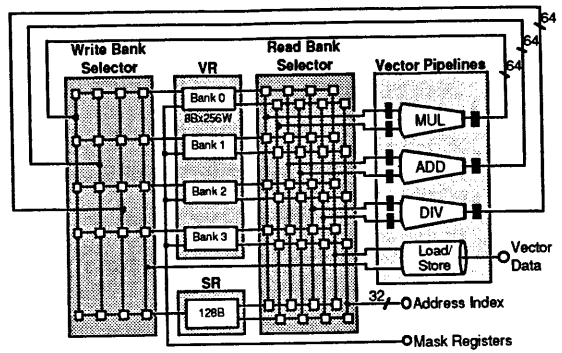
- The command buffer contains 256 thirty-two bit registers. They can contain instructions or immediate data.
- Using a special instruction, the command buffer can reload itself. However, an external host processor must load the first command block.
- The instruction set supports two conditional branch instructions. However, the instruction set does not support subroutines.

## Vector Registers

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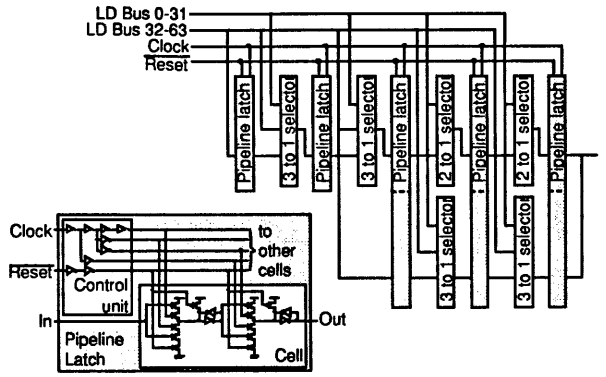
- The vector register set contains 8 Kbytes. The scalar register set is 128 bytes (32 registers long, 32 bits wide). The mask register set contains 64 bytes.
- A programmable vector length register holds the logical length of every register in the vector register set (they are all the same length). Depending upon the value stored in the vector length register, the number of vector registers varies, either 8, 16, 32, or 64 registers.
- The vector length register also controls the number of mask registers, either 2, 4, 8, or 16.
- The vector registers are internally divided into four banks. Each bank is a 2K static RAM with three ports. The banks are 64 bits wide and 256 words deep. The access time, including the bank selector delay, is less than 14 ns. when the chip is clocked at 70 MHz.
- The bank selectors use tristate drivers. Therefore, the bank selectors require only 25% of the die area that ordinary AND-NOR gates require.

## Load/Store Pipeline

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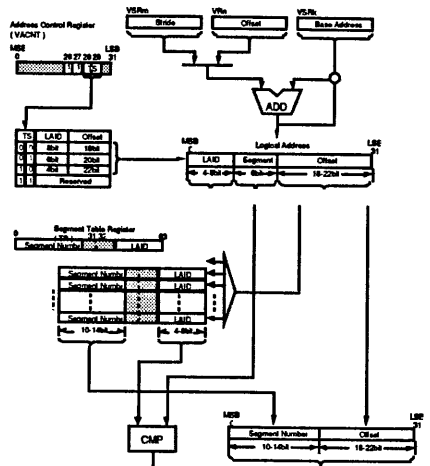
- The load/store pipeline can output addresses before it needs to use them. It can output up to four addresses.
- Two hardware memory interface modes exist: pipeline and basic. Only vector load and store operations use pipeline mode. Vector scatter/gather operations use basic mode. A basic mode access takes two clock cycles. A pipeline mode access takes a single cycle.

## Address Unit

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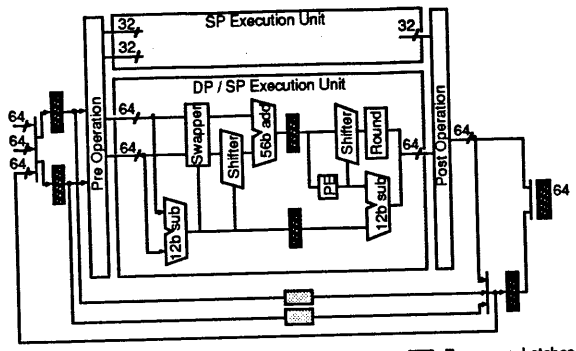
- The address unit has three modes: Real, Segment, and Page.
- The segment mode has three possible segment sizes: 256 kB, 1 MB, and 4 MB.
- In page mode, the page size is 4 kB. Page mode was designed to work with a future version of GMicro, a microprocesor used in Japan's TRON project. Designers using other microprocessors may not find page mode useful. The µVP does not generate page faults.

## ADD Pipeline

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- The ADD pipeline shares a single vector register interface with the Graphics pipeline. Therefore, both pipelines cannot operate at the same time.
- The ADD pipeline executes the macro instructions (Vector Search Maximum/Minimum Index, Vector Sum). Thus, it needs the feedback loop and temporary registers pictured above.
- The multiply and divide pipelines are not shown.
  - The multiply pipeline first stage contains a 54 byte by 54 byte multiplier tree and a Booth's decoder that produces a double precision result each clock. The second stage contains a 108 byte final partial product adder, a normalizer, and a rounding circuit.
  - The divide pipeline contains two divider units operating simultaneously. Each divider is implemented using iterative and high radix nonrestoring division.

## Software

- VAST from Pacific-Sierra
- Compilers
  - Portland Group (SPARC with µVP)
  - Green Hills Software (GMicro with µVP)
- SEG & BLAS Libraries from SofTek in Japan

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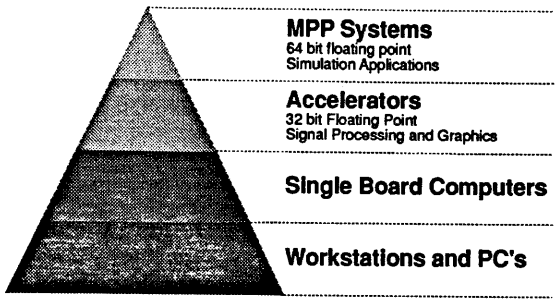
- Fujitsu has an assembler and a simulator available.
- It is not yet final. However, I believe Local Knowledge will provide SofTek's µVP support outside Japan.

## Customers

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- The µVP Series is a "horse" more than one massively parallel vendor is riding in the "Teraflop Race".
- Intel's i860 currently dominates the other markets that the µVP Series is targeted at. However, many existing i860 customers are convinced that Intel will not design new members of the i860 family. Therefore, the µVP Series is getting significant attention from Intel's existing customers.

## Schedule

- 50 MHz samples were shipped in mid-June to design wins in both the U. S. and Japan.
- Fujitsu expects production 33 MHz parts in September and 50 MHz parts in December.
- Fujitsu has not yet announced a schedule for 70 MHz parts.

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