PCI
Peripheral Component Interconnect

Hot Chips Symposium
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David Carson

Intel Corporation

Peripheral Component Interconnect

- Motivation - Design Objectives
- Local Bus Alternatives
- PCI Characterization
- Performance Considerations
- PCI Applications
- Summary

MARKETING PRESENTATION

What should a local bus accomplish?

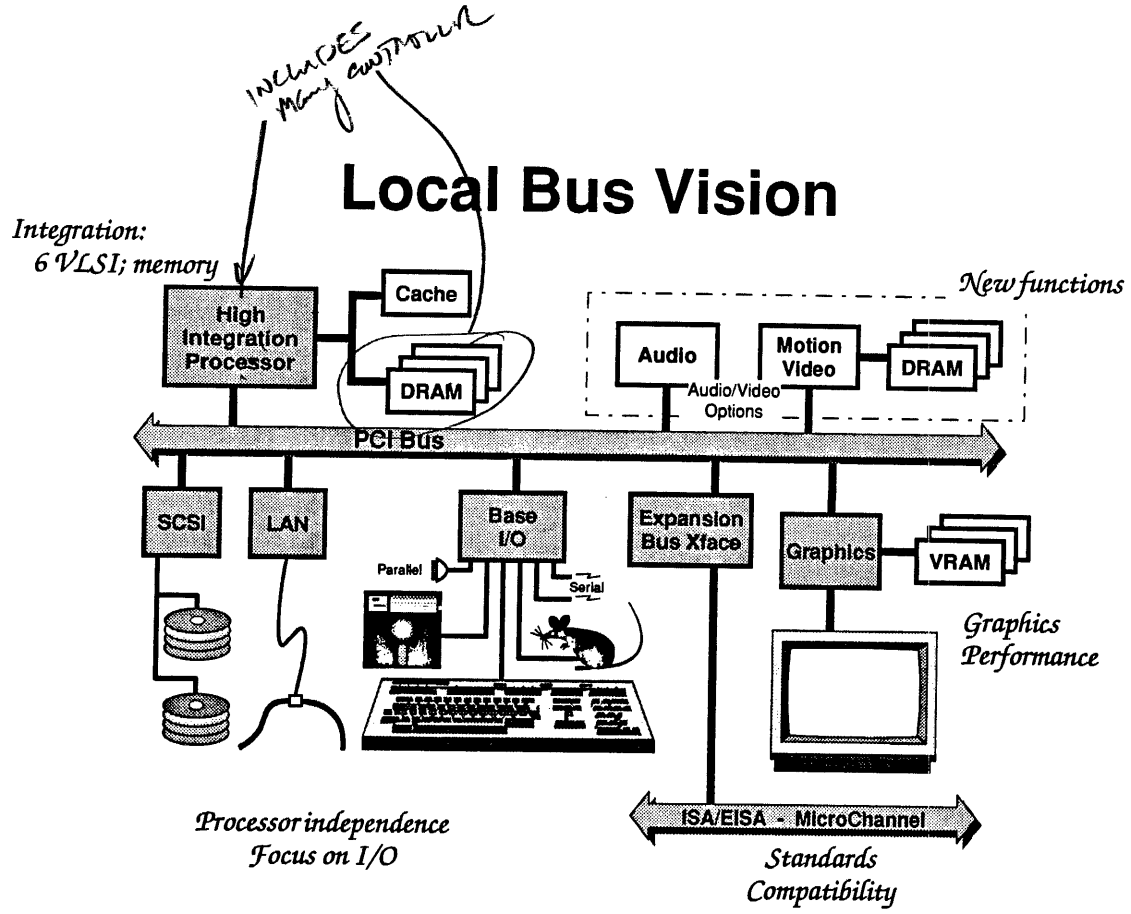
Enable PC innovation in:

- ✦ **Performance:** ✓ allow second to none graphics for PCs
  ✓ overcome standard bus limitations
- ✦ **Function:** ✓ e.g., multi-media, motion video at volume price points
- ✦ **Cost:** ✓ highly integrated systems
  ✓ lowest cost peripherals
  ✓ investment spanning multiple CPU generations

by driving a

component-to-component connection standard

for PCs, to complement existing board-to-board connection standards.



PCI Design Objectives

- Performance
  - ✓ Data bursting as normal operating mode - both read & write
  - ✓ Linear burst ordering (NOT CACHE WRAPAROUND)
  - ✓ Concurrency support (deadlock, buffering solutions)
  - ✓ Multi-master, peer-to-peer protocol
  - ✓ Low latency guarantees for real time devices
  - ✓ Access oriented arbitration (not time slice)
- Cost
  - ✓ No connection glue; no external data buffers
  - ✓ Low pin count interface
  - ✓ Implementable in existing ASIC technologies

PCI Design Objectives

- Reliability
  - ✓ Thorough electrical design for multiple loads in 33 MHz local bus environment
  - ✓ Error detection, reporting
- Flexibility:
  - ✓ Processor independent; peripherals off processor "treadmill"
  - ✓ Multi-master; peer-to-peer protocol
  - ✓ Multi-media support
  - ✓ Compatible with existing expansion standards
  - ✓ Scaleability designed in from the beginning
  - ✓ Applicable from laptop to server

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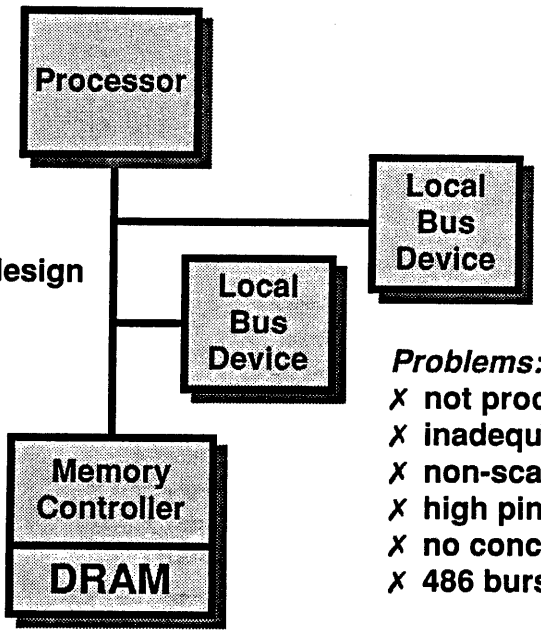
Processor Bus

Alternative 1



✔ Quick turn design

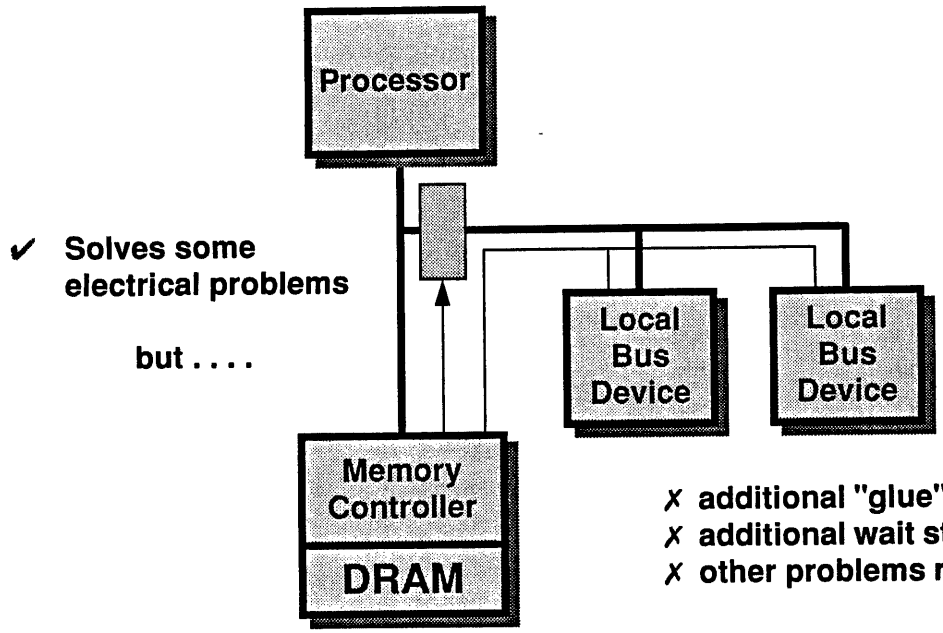
but . . . .

Problems:

✗ not processor independent
✗ inadequate electrical design
✗ non-scaleable thruput
✗ high pin count
✗ no concurrency
✗ 486 burst ordering

Buffered Processor Bus

Alternative 2



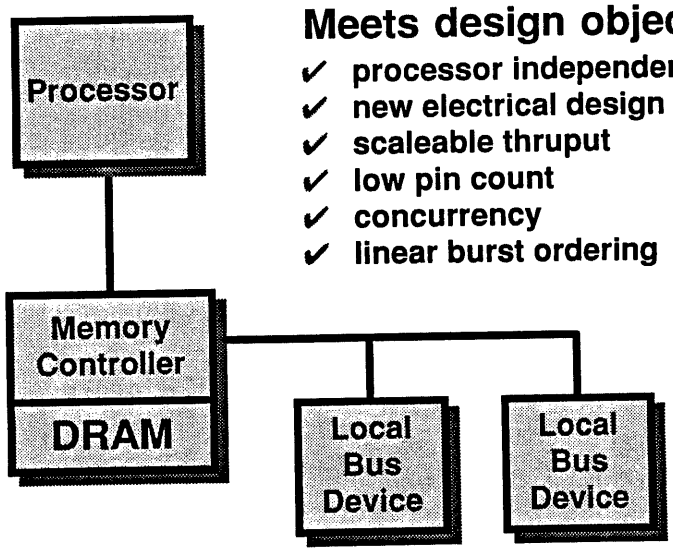
✔ Solves some electrical problems

but . . . .

✗ additional "glue"
✗ additional wait states
✗ other problems remain

Intermediate Local Bus

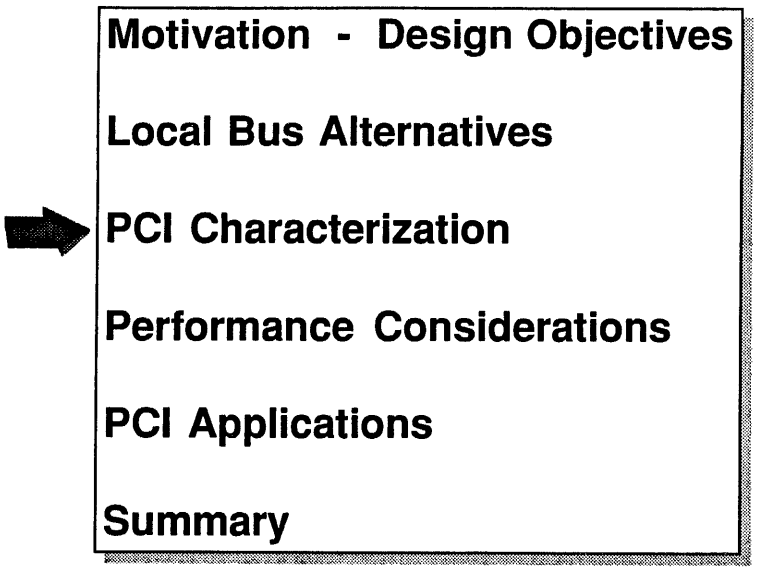
Alternative 3



Meets design objectives

✔ processor independent
✔ new electrical design
✔ scaleable thruput
✔ low pin count
✔ concurrency
✔ linear burst ordering

Peripheral Component Interconnect



PCI Characterization

- Protocol
  - ✓ Multi-master, peer-to-peer
  - ✓ 32-bit multiplexed, processor independent
  - ✓ Low pin count; 45 slave; 47 master
  - ✓ Synchronous, 8 - 33 MHz (132 Mbyte/sec)
  - ✓ Variable length, linear bursting - read & write
  - ✓ Parity on address, data, command
  - ✓ Concurrency/pipelining support
  - ✓ Initialization hooks for auto-configuration
  - ✓ Arbitration: central, access oriented, "hidden"
  - ✓ Comprehends write-back cache operation
  - ✓ 64-bit extension transparently interoperable with 32-bit

PCI Characterization

- Electrical
  - ✓ CMOS drivers; TTL voltage levels
  - ✓ 5 V, 3.3 V interoperable; 5-volt "safe"
  - ✓ Reflected wave, rail-to-rail signalling
  - ✓ Dynamic current / voltage specified for drivers
  - ✓ Optimized drivers minimize pwr/gnd requirements
  - ✓ Direct drive - no external buffers; comprehends connectors

PCI . . . more than a paper spec

- ✦ 5000+ hours SPICE simulation completed
- ✦ Full scale prototype correlated to SPICE model
- ✦ PCI-optimized buffers available thru several ASIC houses
- ✦ PCI SPICE models available thru Meta-Software
- ✦ PCI logic/validation models available thru Logic Modeling (LAI)

Design completeness → *RELIABILITY*

Peripheral Component Interconnect

Local Bus Bandwidth Requirements

- LAN (FDDI ~12 MB/sec) — 1 MBytes/sec
- SCSI (multiple spindles ~10-15 MB/sec) — 5+ MBytes/sec
- Full Motion "Business Video"
  - YUV-8 color space
  - compressed NTSC = 0.2 MB/sec
  - 320 × 240 = 2.3 MB/sec
  - 640 × 480 = 9.2 MB/sec (× 2) = ~20 MBytes/sec
- Graphics:
  full page 1280 × 1024
  full color - RGB × 24 bits
  "flip through a book" × 10 frames/sec = 40 MBytes/sec

PCI Bandwidth:	32-bit Base	64-bit Expansion
Peak	132 MByte/s	264 MByte/s

Observations
- Bandwidth needs to be efficiently shared
- Transparent extensions (wider/multiple buses) are important

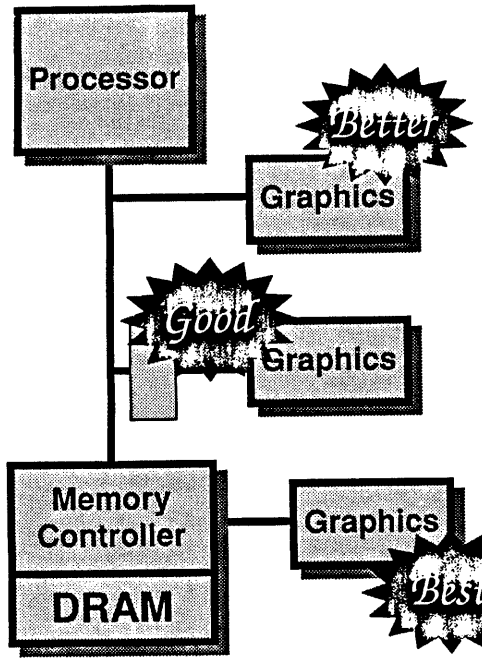
Focus on Graphics

- Frame buffer access characteristics:
  - ✓ Dumb Frame Buffer ~ 80% writes
  - ✓ Windows/"Smart" Frame Buffer > 90% writes
  - ✓ BAPCO Benchmark 95% writes (measured)
- Writes (not reads) determine graphics performance, consequently

Local bus design target should be ZERO processor wait-state writes especially on higher frequency processors

Graphics Performance

Frame Buffer Writes



- GUI attached to processor bus adds wait states with increasing bus frequency
  - ✓ Address decoding
  - ✓ Buffering delay
  - ✓ Synchronization delay
- PCI exploits pipelining potential to provide zero wait-state writes
  - ✔ PCI bridge posting & sequential access combining
  - ✔ Bursting is normal target mode for "Smart" Frame Buffer on PCI

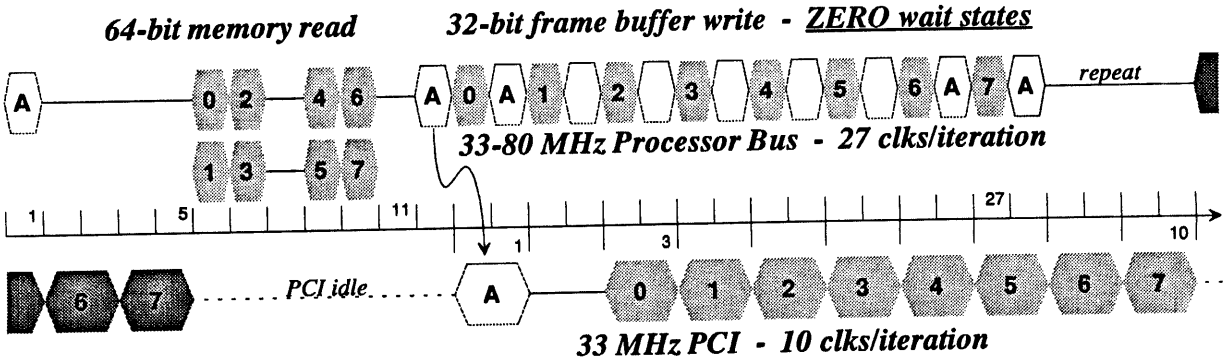
PCI provides best "Smart" frame buffer performance

An Example

Zero Wait-State Writes

Most demanding write sequence is source-copy (memory-to-screen) typically done with *Repeat-MOV-String*:

1. **Pixel map read from memory in cache line bursts**
2. **Pixels written to frame buffer in D-word (32-bit) accesses**



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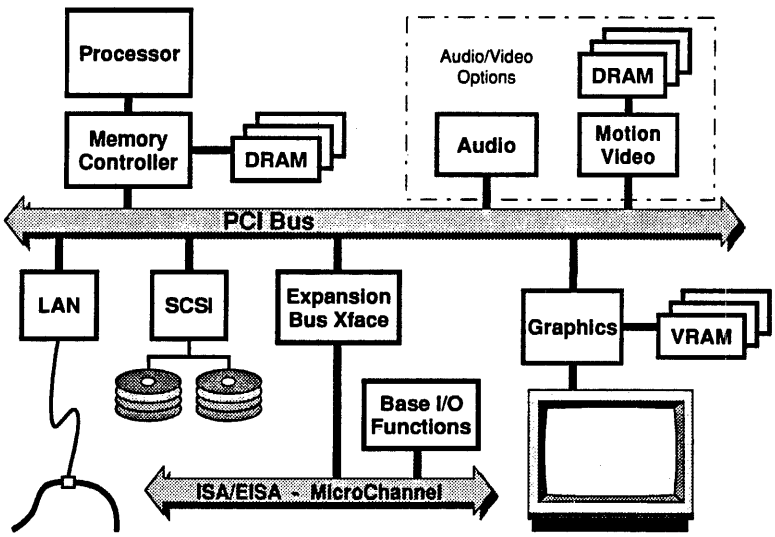
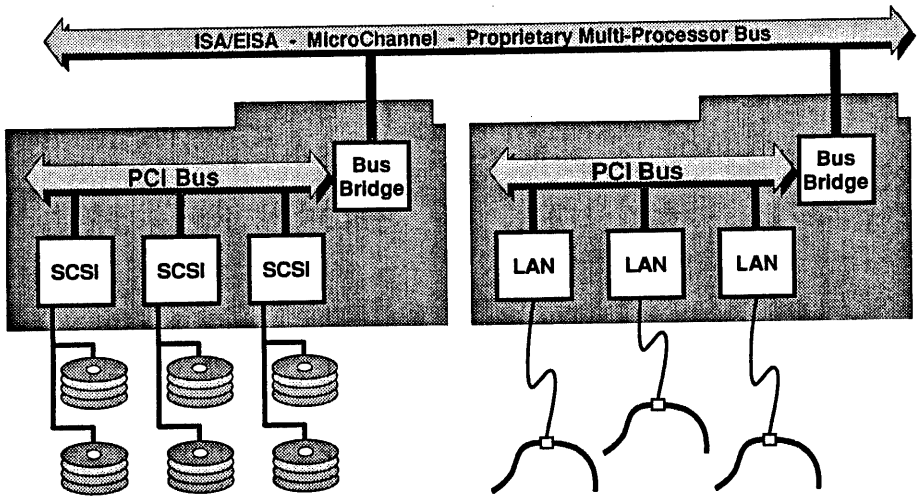
Desktop Application



I/O Subsystem Application



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Summary

Compared with processor bus or buffered processor bus approaches, PCI provides:

Performance:	**Higher graphics performance.** **Multi-master concurency.**
Cost:	**Lower pin count.** **Highest level of system integration.**
Reliability:	**Thorough electrical design and extensive modeling.**
Flexibility:	**Processor independence.** **Pre-defined, transparent scaleability.**
Acceptance:	**Broad industry support.**

Broad Industry Support

"Intend to build or support PCI-compliant devices or systems."

OEMs

- ✓ Acer
- ✓ ALR
- ✓ AST
- ✓ Compaq
- ✓ DEC
- ✓ Dell
- ✓ Epson
- ✓ FUJITSU
- ✓ Gateway 2000
- ✓ HP
- ✓ IBM
- ✓ Mitsubishi
- ✓ NCR
- ✓ NEC Tech.
- ✓ Oki
- ✓ Olivetti
- ✓ Siemens
- ✓ Tandy
- ✓ Unisys
- ✓ ZDS

Vendors

Graphics;
- ✓ ATI
- ✓ Cirrus
- ✓ Headland
- ✓ Intel
- ✓ Matrox
- ✓ NCR
- ✓ Tseng Labs
- ✓ S3
- ✓ WD

SCSI;
- ✓ Adaptec
- ✓ NCR

LAN;
- ✓ Intel
- ✓ TI

Video;
- ✓ Intel

Chipsets;
- ✓ Headland
- ✓ Intel
- ✓ VLSI
- ✓ WD

Board;
- ✓ AMI
- ✓ Micronics

Other;
- ✓ National
- ✓ NCR

Software/Tools

OSVs;
- ✓ IBM OS/2
- ✓ Microsoft

BIOS;
- ✓ AMI
- ✓ Phoenix

Tools;
- ✓ Logic Modeling (LAI)
- ✓ Meta-Software

More Information?

- PCI hotline: (503) 696-2000
  - ✓ Request a specification
  - ✓ Join PCI Special Interest Group
  - ✓ Questions / Support