The SBus GoldChip™

A High Performance SBus Interface/DMA Controller

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Sun Microsystems

Hot Chips IV

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Design Goals

- Complete implementation of SBus Spec B.0 and the IEEE P1496 draft standard
- "Glueless" Programmable Peripheral Bus
- Full-featured 8-channel DMA Engine
- High Performance (> 160 MByte/S) BW
- High Level of Integration
- Support and Conformance to IEEE 1149.1 JTAG

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The LBus

(The SBus GoldChips' Peripheral Bus)

Has the unique capability of looking like three separate peripheral buses

- Non-multiplexed 32-bit address and data bus
- Multiplexed 64-bit data with 32-bit address bus
- Handshake protocol for "oldstyle" DMA devices

Switchable 'on the fly' from protocol to protocol on a cycle-by-cycle basis, without timing delays or performance penalties.

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The LBus (Cont.)

- May be dynamically configured as big or little endian
- Will accept external acknowledgment, internal count, or combinations
- Supports atomic operations
- Provides burst support even with portsizes < 32-bits
- Provides dynamic sizing in both mux and non-mux modes
- Programmable timing on control signals allow for tuning to individual device requirements
- Bandwidth exceeds 160 MB/S

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Process Summary

INTEL VENDOR MOD

-Triple metal (2.0/2.0/2.0)

-0.7u Leff

-approx. 380,000 transistors

-304 Lead thermally enhanced PQFP

-128-bit wide internal datapaths

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Complete Implementation of SBus Spec B.0 and IEEE P1496 means

- All Burst Modes
- Supports SBus Parity
- Support Atomic Transfers
- Meets all AC and DC specifications
- Works correctly with all compliant SBus controllers produced to date, and anticipated in future.
- NO EXCEPTIONS

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Full-featured DMA Engine

- 8 channels
- Control block chaining (up to 128 blocks)
- Dynamic Chaining

  Blocks may be added/deleted/modified while channel is active.

  Protocol prevents race conditions.
- External control blocks

  May be placed on either SBus or LBus

  Are fetched and loaded automatically as required
- All channels may be active simultaneously and interleave execution (channel interleave)

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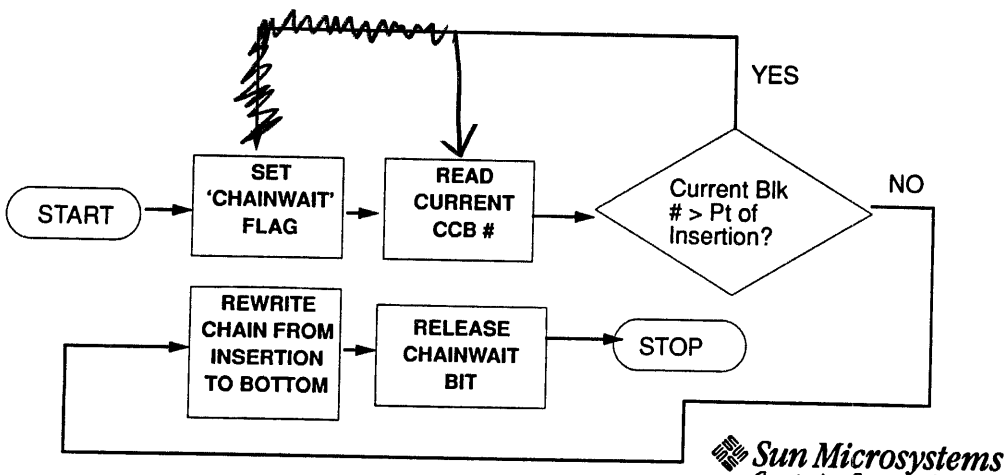
Sample Dynamic Chaining Procedure

- To insert a new control block into an existing chain without stopping DMA execution:



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DMA Engine (Cont.)

- DMA arbitration may be internal or external.

  If internal, the GC offers a unique arbitration algorithm based on the FIFO, and internal/external bus availability to the chip

- SBus and LBus may transfer data simultaneously (bus interleaving)
- The GC may serve as either master or slave on the LBus portion of a DMA transfer
- Scatter/Gather operations are supported
- Multiple instantiation of same control block is supported
- Chain and individual control block execution loops are supported w/multiple loop nesting

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GC Support of DMA Transfers

	Master Mode	Slave Mode
L -> S	Gc signals start of transfer, and after each slice is transferred.	GC signals need to load first slice, and completion of 'S' portion of each slice, and implicitly need to load following slice.
S -> L	GC signals start of transfer and after each slice is transferred.	GC signals start of 'S' portion of transfer and need to read each slice as they become ready on the LBus.
L -> L	GC signals start of transfer and after each slice is transferred.	Not Supported
S -> S	GC signals start of transfer and after each slice is transferred.	Not Supported

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DMA Control Blocks

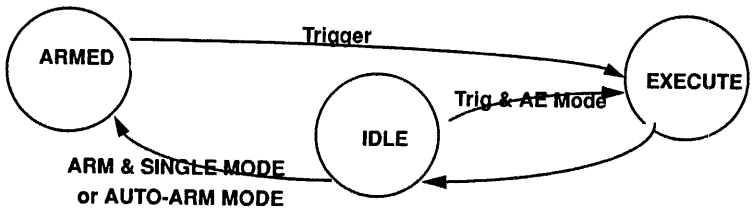
GC control blocks use the concept of being armed and triggered

- Three modes of execution are supported:

  Single execution mode: A block must be both armed and triggered to execute

  Auto-arm mode: A block arms itself and needs only be triggered

  Auto-execute mode: Block arms and triggers itself (example: once the first block in a chain is executed, the remainder in auto-execute mode 'load and go' automatically'



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Resource Based Arbitration

- Resource based arbitration supports the 160 MB/S bandwidth requirement for the chip
- Algorithm replaces fixed algorithm or priority schemes
- GC evaluates buffer capacity, internal bus availability, external bus activity and other resources to determine best way to proceed
- Algorithm is hardwired and does not add latency or a performance penalty
- May be defeated on a channel basis by "wait on resource" flag under special case conditions

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Transfer Slicing

- Transfers are broken up into "slices" or packets
- GC intelligently compares slice sizes to available buffer capacity (a resource)
- Works in conjunction with resource based arbitration algorithm
- Algorithm strives to keep buses active continually
- Channel ordering is affected by selection of slice size in driver program

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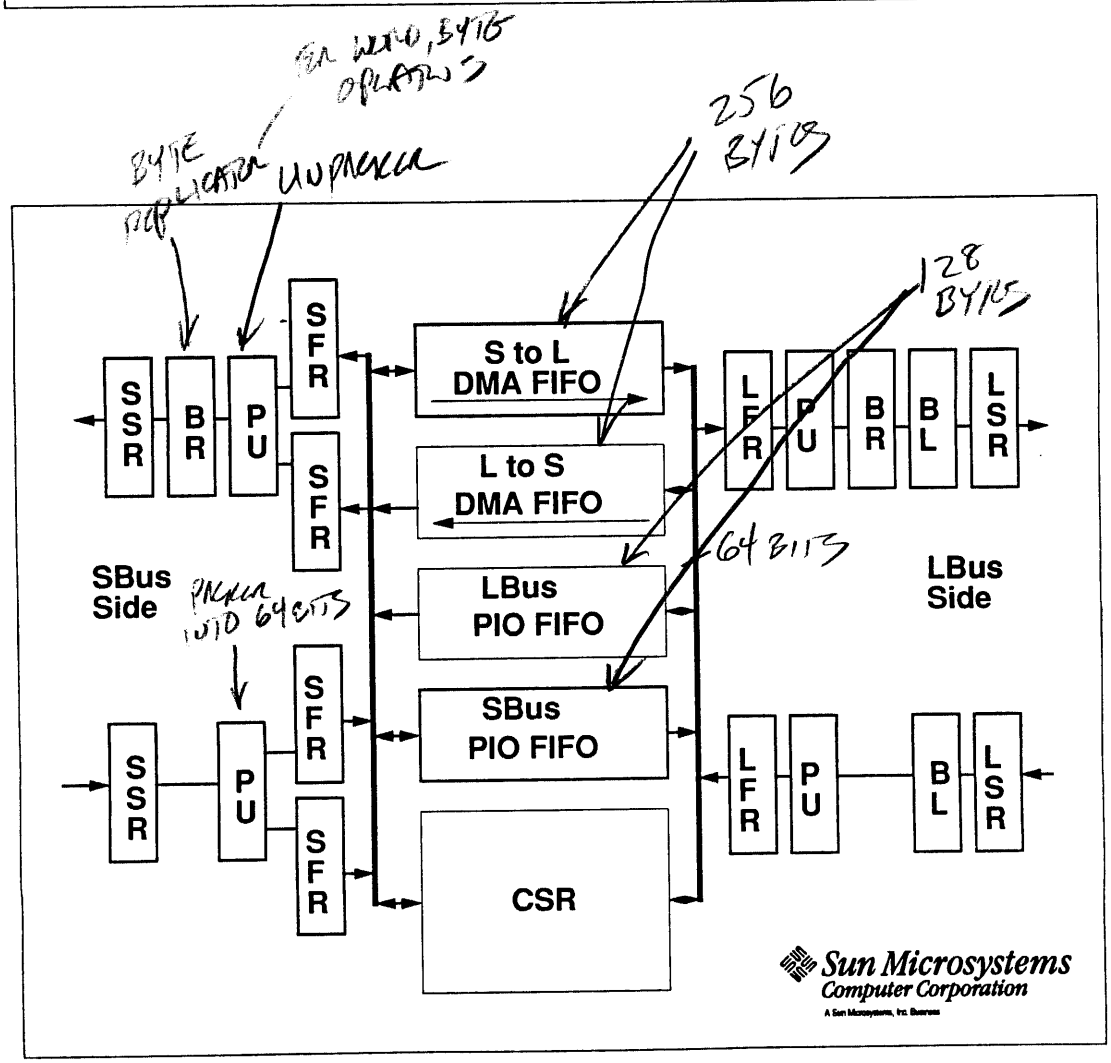

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GC Datapaths

- 5 stage data pipelining
- Pack/unpacker module assembles incoming data to 64-bit widths, and disassembles outgoing data as required for smaller portsizes
- Byte-replicator module duplicates bytes (and halfwords and words) for writes to larger portsizes
- Big-little endian swapper supports little endian conversion for such devices on the LBus
- Staging registers next to each bus and surrounding the FIFO to meet strict timing requirements
- Dataflow structure is symmetric around the middle to either right or left. Transfers conceptually are made either SBus to LBus to/from FIFOs.

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Buffer Configurations and Capacity

- One 256-byte 3 port L -> S FIFO. Data is written from the LBus and can be read by either bus.
- One 256-byte 3 port S -> L FIFO. Data is written from the SBus and can be read by either bus.
- Two 128-byte 3-port PIO FIFOs.One FIFO each is dedicated to the LBus and SBus.
- Three 64-byte 4-port rams, for internal DMA control block storage.

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Summary

- High Performance Flexible DMA Engine
- Full and Comprehensive 64-bit SBus Interface
- High level of Integration
- Innovative approaches to Arbitration and Bus Utilization Produce Sustainable High Transfer Rates