SPARC90
Chipset on a Chip

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PERSONAL COMPUTER/WORKSTATION CPU EVOLUTION

Processor and Discrete Logic --> 1988

1 to 2 large commercial processor chips
MSI components
SSI components

Processor and Proprietary ASICs 1986 --> 1992

1 to 2 large commercial processor chips
1 to 5 large proprietary ASICs (gate arrays typically)
Lesser amounts of MSI, SSI glue logic

Chip Set Solution 1989 --> 1995

Large commercial:
- Integer processor chip
- Floating point chip
- Memory management/cache control chip
- Peripheral chips

Fewer (or no) Proprietary ASICs

Single Chip Integrated Solution 1992 -->

One large commercial CPU chip:
- Internal integer processor
- Internal floating point
- Internal caches
- Internal MMU
- Internal memory controller
- DRAM, bus, DMA interfaces
- Internal system functions– timers, interrupt logic, etc.
- Minimal extra board logic

SPARC90

320K XTORS

CPU Features

Integer Processor
- SPARC Version 8 architecture
- 13 MIPs
- Integer multiply and divide
- Register file with 8 windows

Floating Point
- Floating point register file– 32 x 32bit registers
- Software emulation of arithmetic operations
- Floating point to/from integer register moves– single cycle

Instruction Cache
- Virtual
- 512 Bytes
- 4 instructions (16 bytes) per line
- 1 word sublocks

Data Cache
- Virtual
- 256 Bytes
- 2 words (8 bytes) per line
- 1 word sublocks

MMU
- SPARC Reference MMU
- Hardware tablewalk
- TLB– 32 entries, 4 way set associative

Memory System Features

Memory Interface
- Arbiter for all memory system accesses
- Controls DRAM, slave interface, on chip accesses and SPARC90 bus release
- Fault status and address registers

Direct DRAM Interface
- Clocks for DRAM signals
- Drives RAS, CAS, WRITE, OE, Address, Data pins
- Fast page mode 50-60ns DRAMs assumed
- 32 bit data bus
- 53 MBytes/sec. peak bandwidth
- 1Mb, 4Mb, 16Mb DRAMs provided for
- x1, x4 DRAM organizations
- 1 or 2 memory banks directly supported
- 4 or 8 memory banks with external logic
- Refresh controller– CAS before RAS, scrub
- Byte parity

System Bus Interface
- Controls system bus
- Drives AS, DS, RD, WR, SIZE
- Detects RDY, ERR
- Byte, halfword, word devices
- Big or little endian devices

DMA Interface
- Virtual or physical
- Handles DMA devices that do not generate addresses– type 1
- Allows DMA devices that generate addresses– type 2

External Bus Masters
- DMA type 2 special case

System Features

Timers
- 2 general purpose timers
  - interrupts generated on timeout
  - 28 bits
  - 100ns resolution (4 cycles @ 40MHz)
  - 25.6sec maximum timeout period @ 40MHz
- Slave timeout counter
  - 16 bits
  - 25ns resolution (1 cycle @ 40MHz)
  - 1.6ms maximum timeout period @ 40MHz

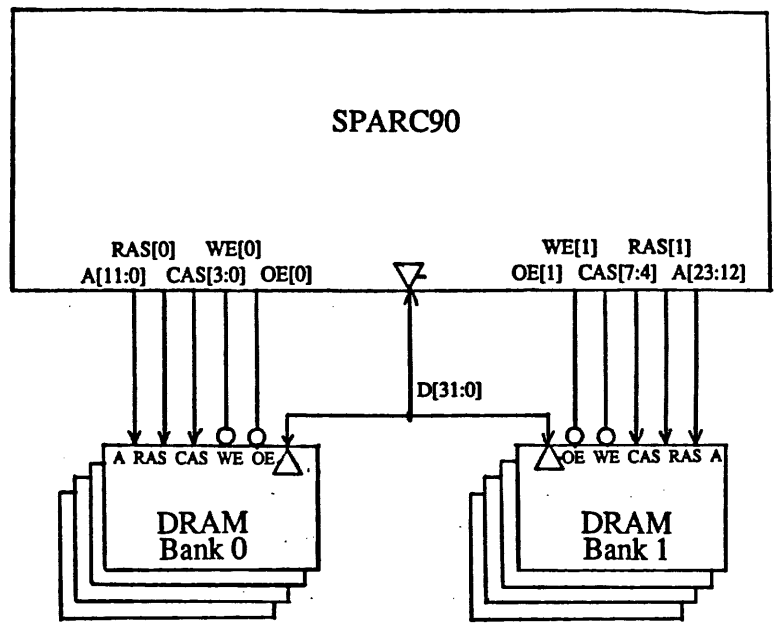
Interrupts
- 8 external interrupts
- Gathers and prioritizes interrupts from DMA devices, timers, and external sources
- Generates Interrupt Request Level (IRL) for IUcore

Debug
- Breakpoint on data accesses
- Memory mapped read/write of internal registers and caches

Powerdown
- Low power mode
- Software or pin activated
- 400mW

Reset
- RESET in pin
- Watchdog resets internally generated
- Software internal reset
- Software external reset
- RESETOUT pin for system use

DRAM Interface



OE (Output Enable) selects bank to read
CAS selects bytes to write
RAS default is asserted —> fast page mode

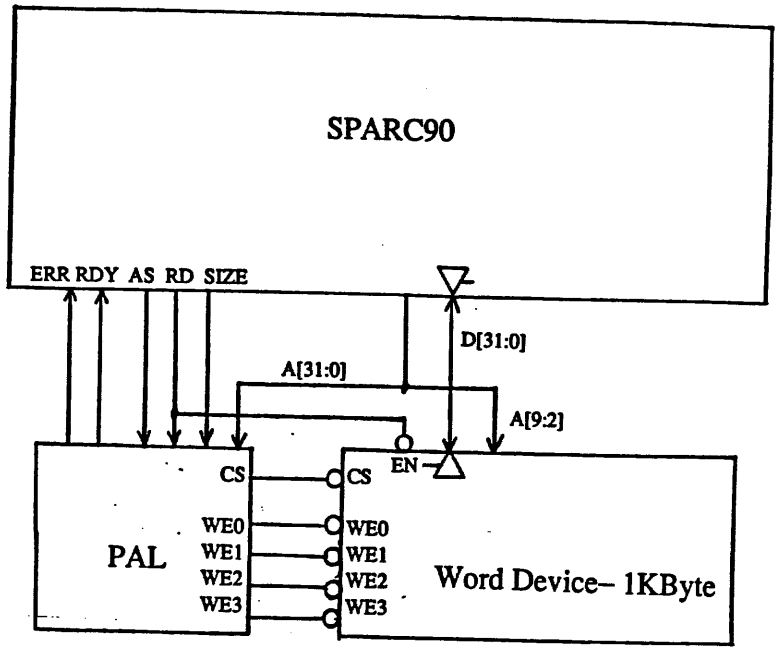
SPARC90 Memory Configurations

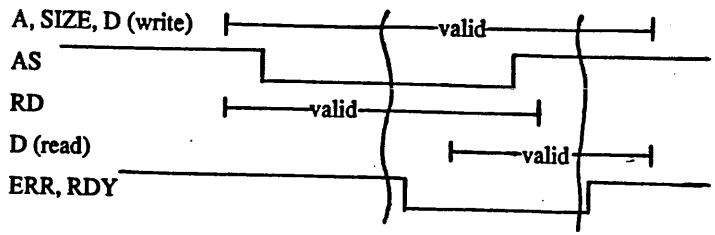
DRAM	1 Bank		2 Banks		4 Banks		8 Banks	
	DRAMs	MBytes	DRAMs	MBytes	DRAMs	MBytes	DRAMs	MBytes
256Kb, 256Kx1	36	1	72	2	144	4	288	8
1Mb, 256Kx4	9	1	18	2	36	4	72	8
1Mb, 1Mx1	36	4	72	8	144	16	288	32
4Mb, 1Mx4	9	4	18	8	36	16	72	32
4Mb, 4Mx1	36	16	72	32	144	64	288	128
16Mb, 4Mx4	9	16	18	32	36	64	72	128
16Mb, 16Mx1	36	64	72	128	144	256	288	512
64Mb, 16Mx4	9	64	18	128	36	256	72	512

One and two bank systems interface directly to SPARC90.

Four and eight bank systems require external logic. The bank select bits of the address A[31:24] indicate the bank being accessed.

System Bus, Slave Device

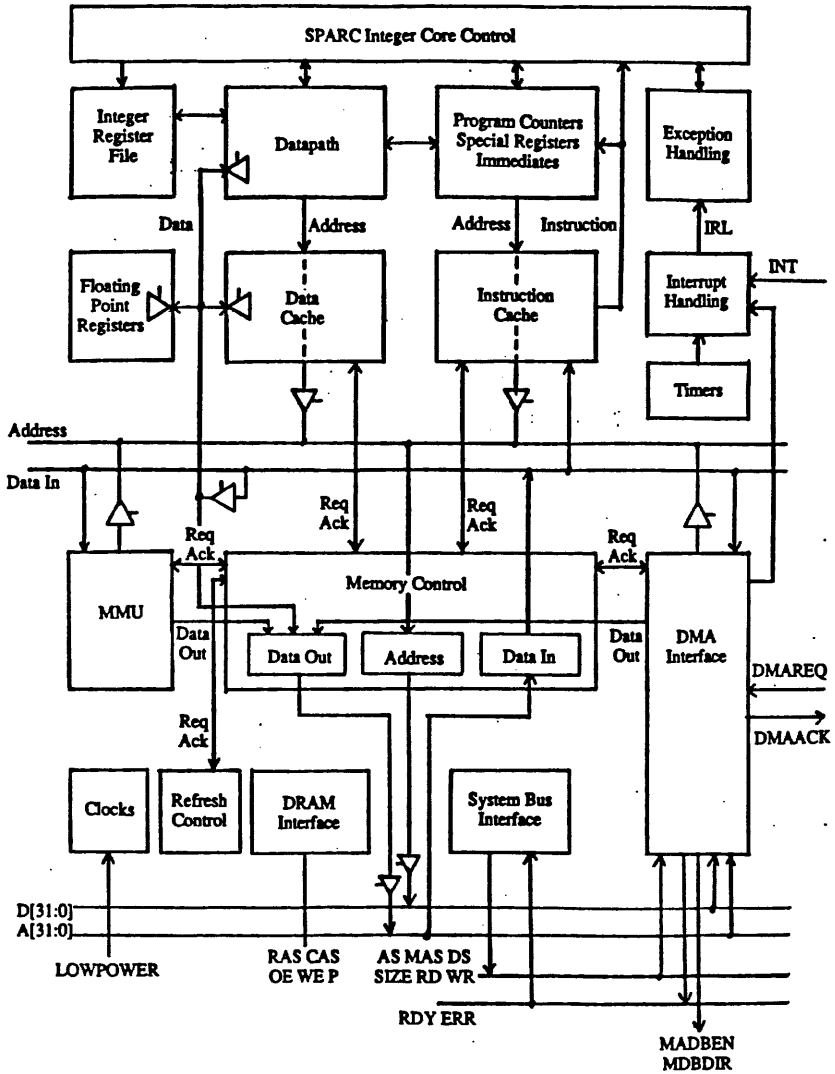




SPARC90 Pipeline– 5 Stage

Time	Stage	Description
Cycle	IFETCH –Instruction Fetch	Instruction is fetched
	READ –Register Read	Decode for READ stage control lines Operand read
	ALU –ALU Operation	ALU operation or address calculation
	MEMORY –Data Cache Access	Data cache is read on loads Data cache is written on stores
	WRITE –Register Write	Results are written

SPARC90 Chip Architecture



Memory System Integration

Memory system functions integrated on a single chip

- Caches
- MMU
- Memory bus that is shared by several users– instruction fetch, data references, MMU, DMA, refresh
- Memory bus arbiter
- DRAM fast page cache tags
- DRAM interface
- System bus interface
- Internal register and cache read/write control
- DMA interface

Advantages

Fast due to:

1. No chip crossings.
2. More parallelism because more wires are possible on chip.

Disadvantages

Complicated due to:

1. "Three ring circus" effect from greater parallelism.
2. Aborts are necessary when speculative tasks are started in parallel.

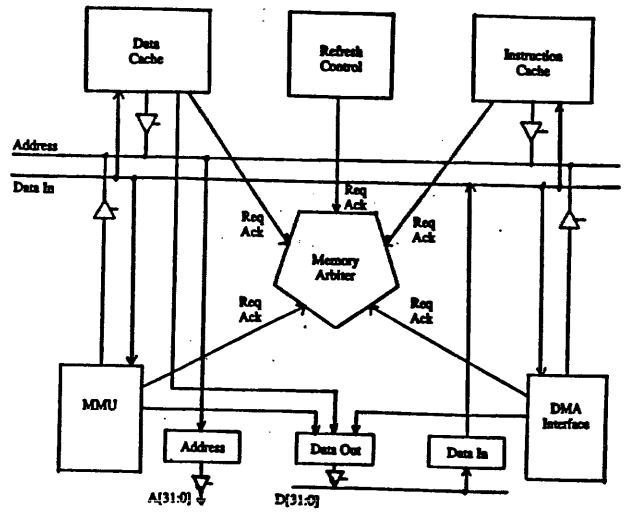
Internal Memory Bus

More Wires

- 5 symmetric request ports
  - – no arbitration to pass most request information to memory controller
    - – request
    - – size, type, lock, virtual, abort
    - – acknowledge
- Shared address lines
- Separate data out lines
- Shared data in line, data in is separate from data out

No chip crossings

- Fast early acknowledge
- Address lines driven quickly



SPARC90 Internal bus	Req	Ack	Address		Data In		
			DRAM	Access	Data In		
Typical External bus	Req	Ack	Address	Extra	DRAM	Access	Data In

Memory Controller Features

Memory Type	Physical Address Range
Byte slave devices	0x00000000 – 0x1fffffff
DRAM	0x20000000 – 0x3fffffff
Internal registers	0x40000000 – 0x7fffffff
Halfword, word slave devices	0x80000000 – 0xffffffff

5 symmetrical memory request ports

Port priorities
- MMU– highest
- Refresh
- Data references
- DMA interface
- Instruction fetch– lowest

Fast page caches
- Active rows of 2 memory banks
- Address compare for "hit" to an active row —> fast page mode access
- Virtual or physical addresses compared
- Tag:

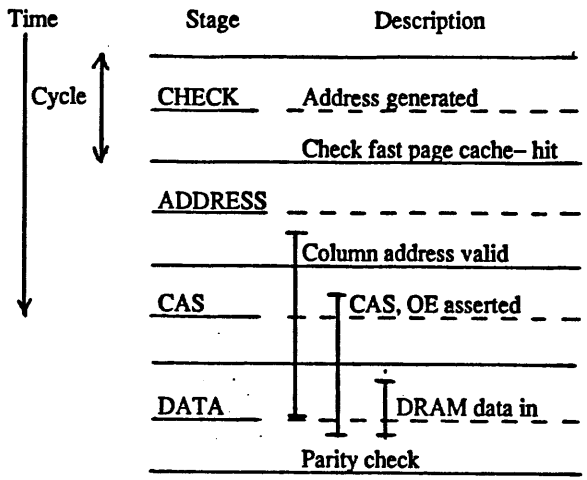
Vld	Vir	Mod	Context	Address

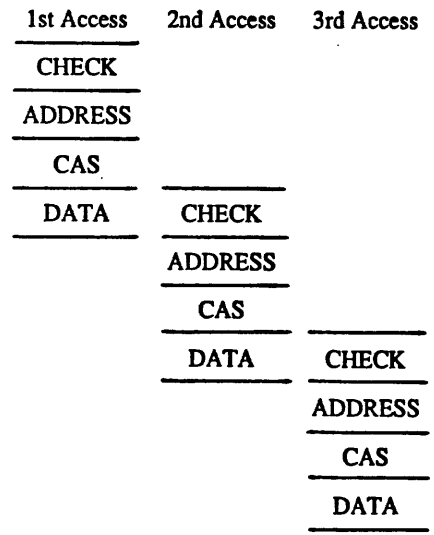
  Vld– Valid
  Vir– Virtual/physical address
  Mod– Page's "modified" bit from Page Table Entry (PTE)
  Context– Context ID
  Address– Upper address bits[31:11]

Optimized for fast page mode access
- 4 stage memory pipeline follows fast page mode timing

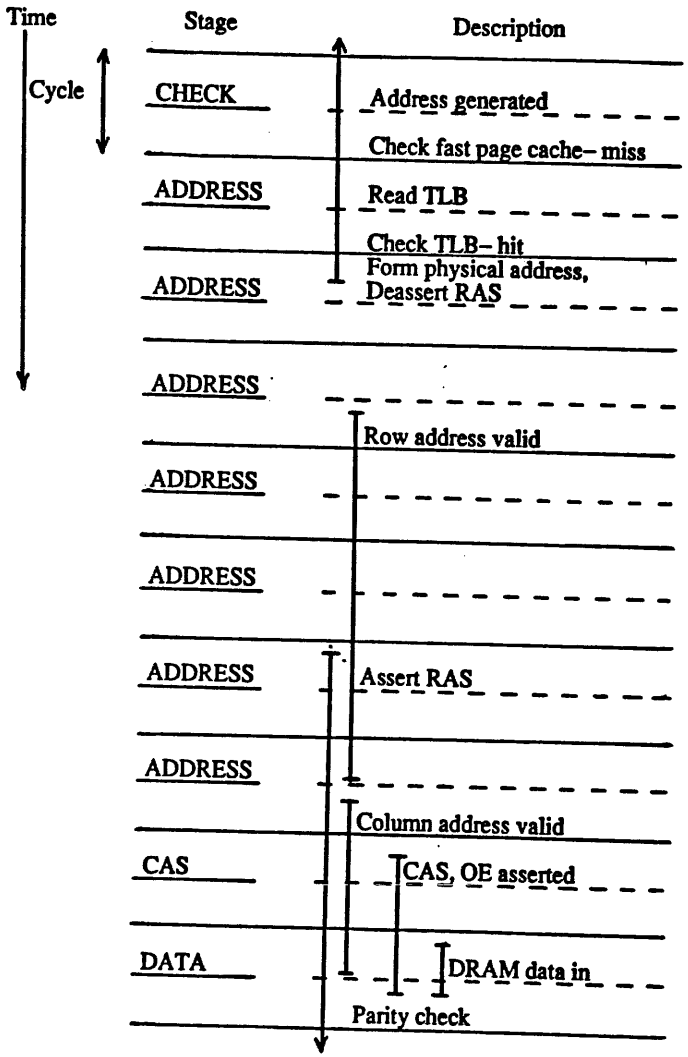
Other accesses stall the memory pipeline —> enter a state machine while stalled
- DRAM row access– 8 cycles
- System bus device– >= 8 cycles
- Internal register– 4 cycles
- External bus master– indefinite

SPARC90 Memory Pipeline

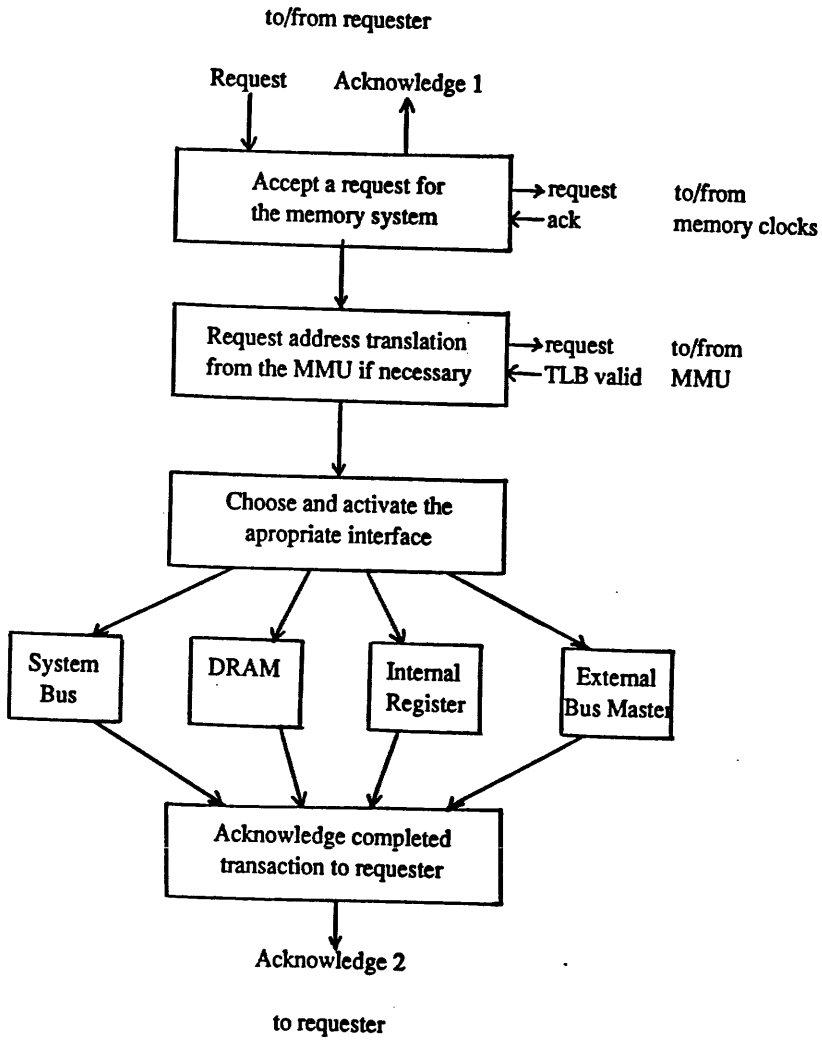




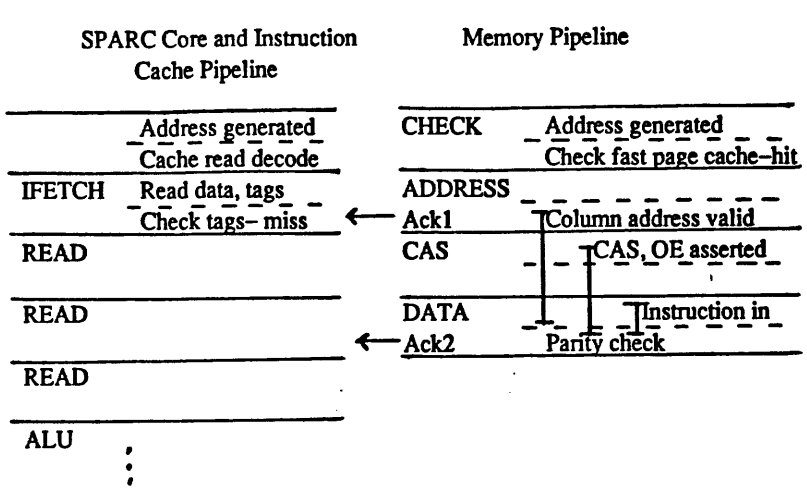
SPARC90 Memory Pipeline– Fast Page Cache Miss



Memory Controller Operation



Instruction Cache



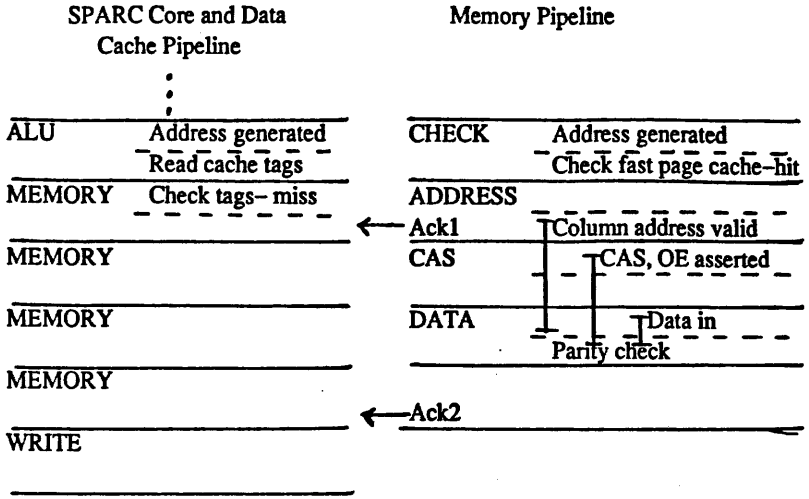
1. Cycle before IFETCH pipeline stage:
   - all potential addresses are formed and available — more wires
   - all potential memory request information available — more wires
   - memory requests asserted, arbitration — no chip crossings
   - address selected — no chip crossings
   - fast page cache tag check– miss — no chip crossings

2. All memory system overhead:
   - 1 cycle– due to more wires and no chip crossings
   - early– due to no chip crossings

3. **RESULT**
   - **—> 0 overhead cycles to fetch from main memory**
   - **—> 2 cycle miss penalty (fast page mode DRAM read)**

4. Therefore:
   - No advantage to burst mode main memory accesses that fill an entire cache line
   - Use subblocks within cache line
     - 32 bit data bus —> 32 bit subblocks
     - Valid bit/subblock

Data Cache



1. Similar to Instruction Cache
   - speed advantages from more wires and no chip crossings.
   - 0 overhead cycles to fetch from main memory.
   - Use subblocks.

2. Difference
   - 3 cycle miss penalty.
   - Extra cycle to avoid register file write on a parity error.

MMU Address Translation– TLB Hit

TLB Hit —> 0 cycle translation penalty.

8 cycle total cache miss penalty (DRAM RAS/CAS access).

This is made possible by:

1. Parallelism from having all potential memory request information available due to "more wires" with the on–chip memory system.
2. Chip crossings eliminated by the on–chip memory system.

TLB Hit

1. Cycle before MEMORY or IFETCH pipeline stage:

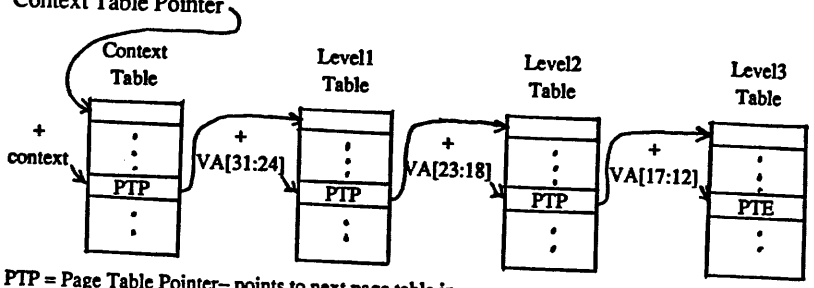
– all potential addresses are formed and available	more wires
– all potential memory request information available	more wires
– memory requests asserted, arbitration	no chip crossings
– address selected	no chip crossings
– fast page cache tag check– miss	no chip crossings

2. MEMORY or IFETCH pipeline stage:

– Caches read, tag check– miss	no chip crossings
– TLB read, tag check– hit	no chip crossings
– Physical address formed and available	no chip crossings
– DRAM cycle started	no chip crossings

MMU Address Translation– TLB Miss

SPARC Page Table Structure
Context Table Pointer



PTP = Page Table Pointer– points to next page table in memory.
PTE = Page Table Entry– contains physical page, protection and other info.

SPARC90 TLB

Caches PTEs and PTPs.
TLB mode
- PTE lookup.
- Virtual page addresses TLB.

Cache Mode
- PTP lookup.
- Physical address of PTP addresses TLB.

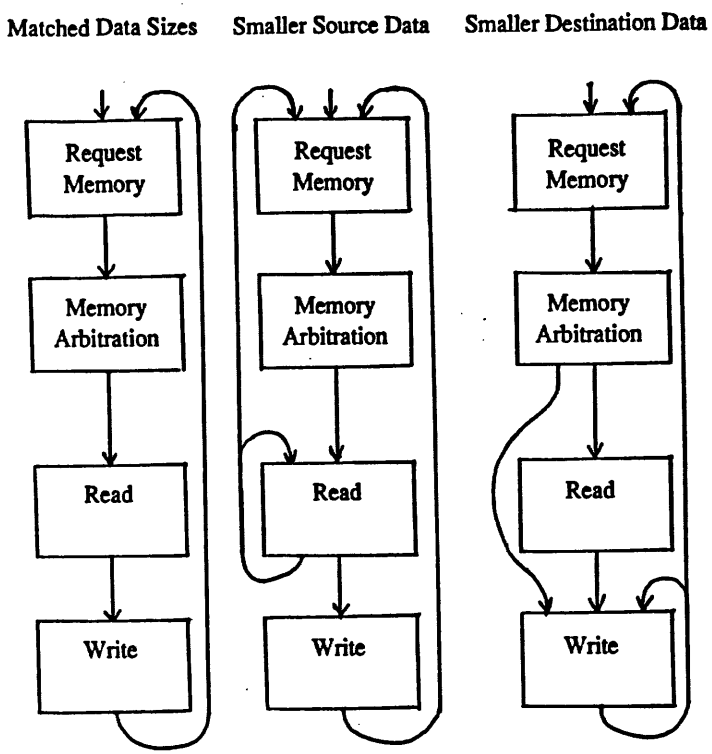
TLB tag field distinguishes PTEs from PTPs.

TLB miss

"Tablewalk" traverses page tables to retrieve PTE and fill TLB.
Original request reissued —> TLB hit.
Penalties (RAS cycled on PTE retrieval):

	PTPs Hit	PTPs Miss Fast Page Mode	PTPs Miss RAS Cycled
Level 1 PTE	15	19	25
Level 2 PTE	17	25	37
Level 3 PTE	19	31	49

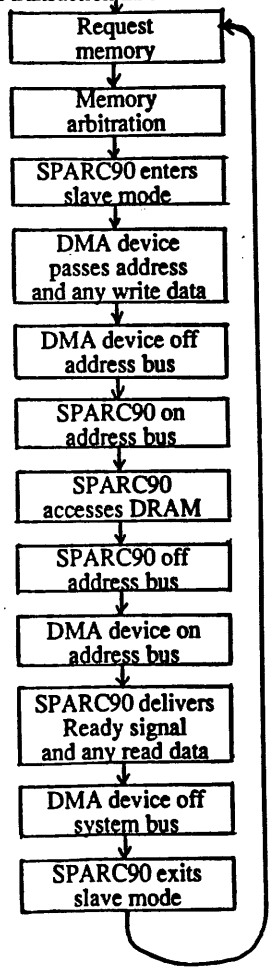
DMA Type 1– SPARC90 Generates Addresses



DMA Type 2– DMA Device Generates Addresses

SPARC90 Master Mode– SPARC90 is bus master of system bus.

SPARC90 Slave Mode– SPARC90 becomes slave of system bus, allowing a DMA device to be bus master and deliver addresses and other DMA transaction information to SPARC90.



SPARC90 Partitioning

Total Chip Partitioning

Section	mm squared	%
SPARC integer core	26.36	17.7
Floating point registers	2.56	1.7
Instruction cache	9.83	6.6
Data cache	9.80	6.6
MMU	13.20	8.8
Memory control	13.12	8.8
DMA interface	9.60	6.4
Timers	2.04	1.4
Interrupts	.99	.7
Internal routing	32.40	21.7
Pads and pad routing	28.94	19.4
SPARC90	148.60	

Core Partitioning– excludes pads and pad routing

Function	mm squared	%
SPARC integer core	33.65	28.3
Floating point registers	3.37	2.8
Memory system	78.62	65.8
Interrupts and timers	4.26	3.6
SPARC90 core	119.90	

SPARC90 Characteristics

Feature	Target
Performance	13 MIPs
DRAM bandwidth (peak)	53 MBytes/sec.
Slave bus bandwidth (peak)	
byte slave	4 MBytes/sec.
halfword slave	8 MBytes/sec.
word slave	16 MBytes/sec.
DMA type 1 bandwidth, slave <--> slave (peak)	
byte transactions	1.5 MBytes/sec.
halfword transactions	3.0 MBytes/sec.
word transactions	6.0 MBytes/sec.
DMA type 1 bandwidth, slave <--> DRAM (peak)	
byte transactions	1.9 MBytes/sec.
halfword transactions	3.8 MBytes/sec.
word transactions	7.6 MBytes/sec.
DMA type 1 bandwidth, DRAM <--> DRAM (peak)	
word transactions	10.6 MBytes/sec.
DMA type 2 bandwidth (peak)	
byte transactions	1.5 MBytes/sec.
halfword transactions	3.1 MBytes/sec.
word transactions	6.2 MBytes/sec
Pins	160 PQFP
Transistors	317,000
Size	480 x 480 mils
Power	
normal	1 W
powerdown	.4 W
Technology	2 metal, .9u CMOS