On-chip cache hierarchy for 1000-MIPS multi-superscalar processor

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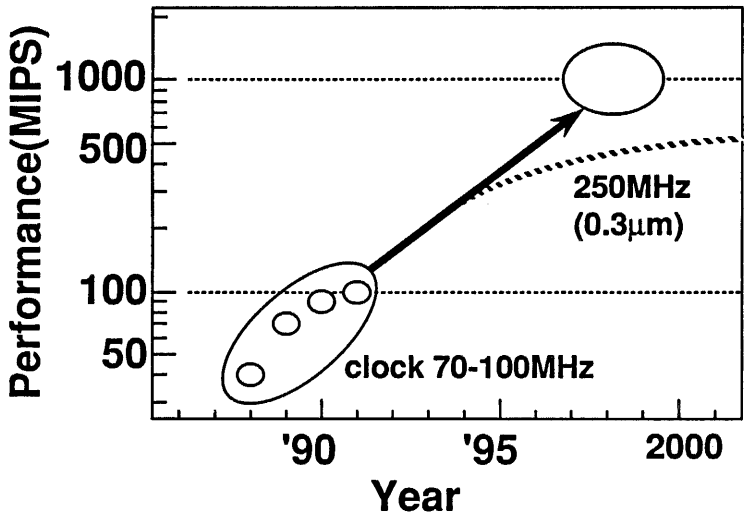
Objective of this work

To achieve a maximum processor performance on a single chip using 0.3 μm BiCMOS technology

Microprocessor performance and its prediction



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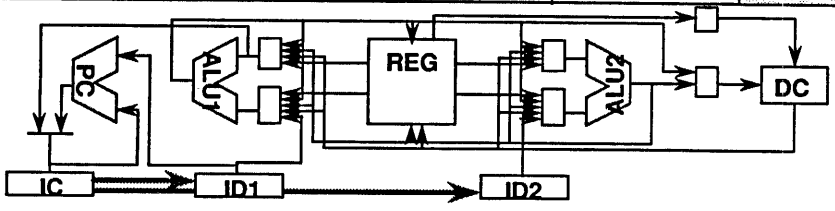
MAX 250 MHZ

Integration capacity using 0.3μm BiCMOS

	performance	area	capacity
Superscalar RISC	clock cycle 3.1 ns	6.6mm^2 /RISC	4 RISCs
FPU	3.5 ns (53bX27b Mult.+Adder)	9.1mm^2 /FPU	4 FPUs
Cache memory	2.8 ns	60mm^2 /128KB	max 256KB



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High performance single chip strategies

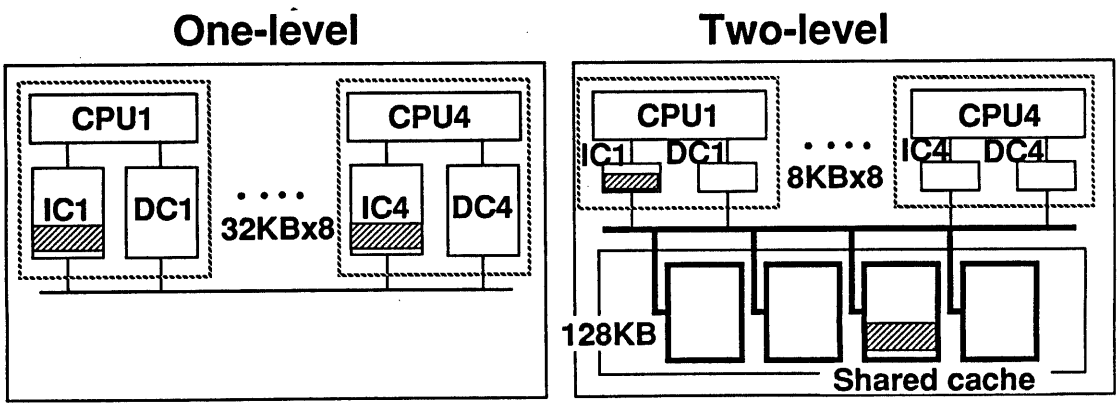
(1) Uni-processor

0.3 μm BiCMOS technology
Dual ALU superscalar architecture

(2)Multi-processor

Interleaved shared cache memory

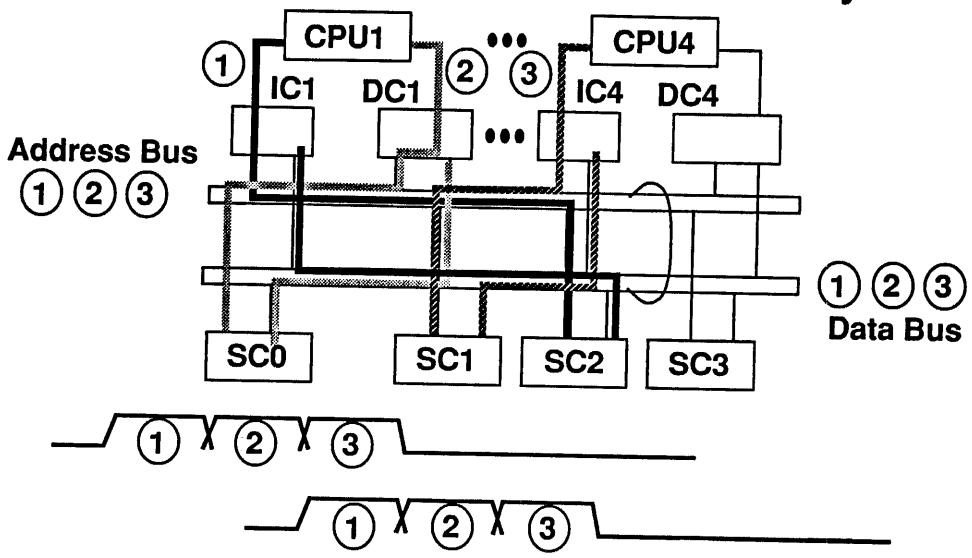
Two on-chip cache strategies



Large private caches

Small private caches and
4-way interleaved secondary cache

Split-bus with 4-way interleaved secondary cache



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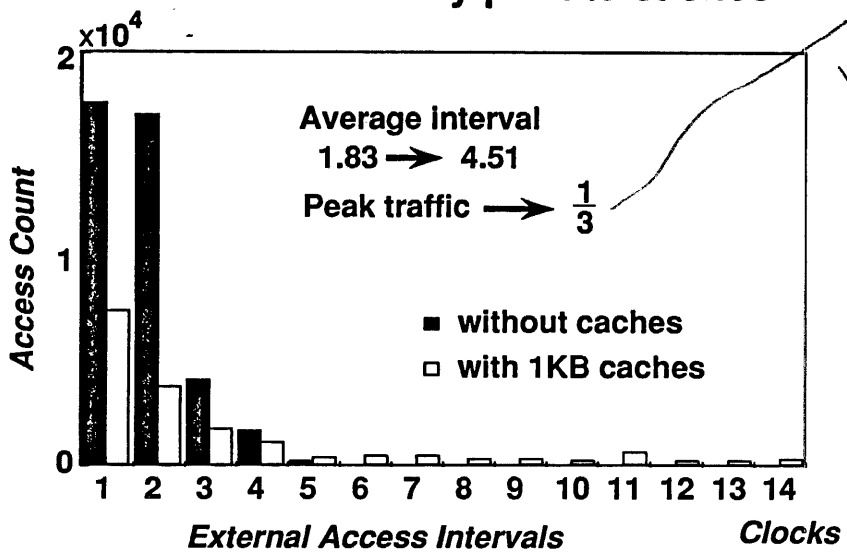
SEPARATE A,D BUSES TO REDUCE CONFLICT

Access reduction by private caches



USING I/C CACHES

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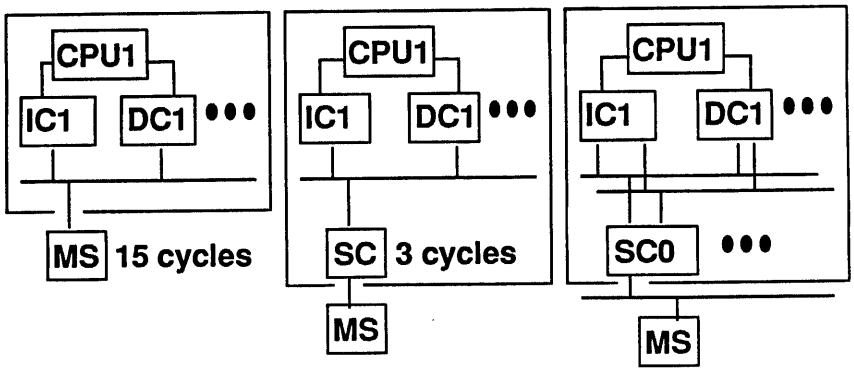
Simulation models

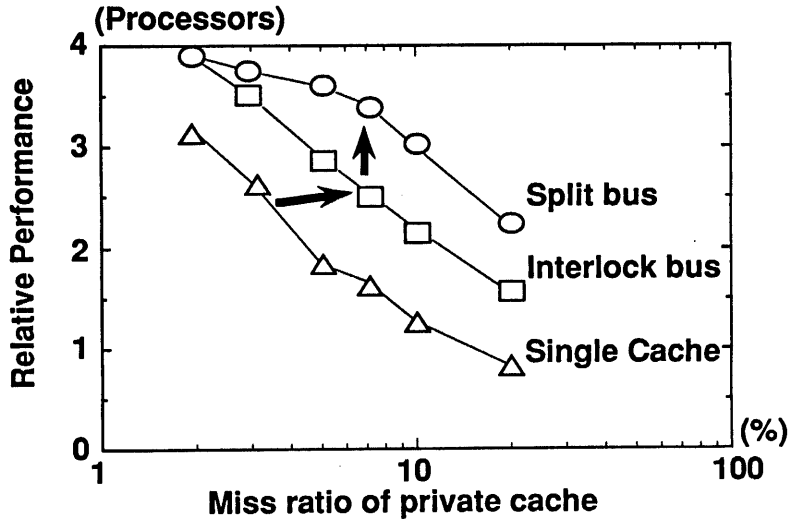


(1) Interlock bus without SC

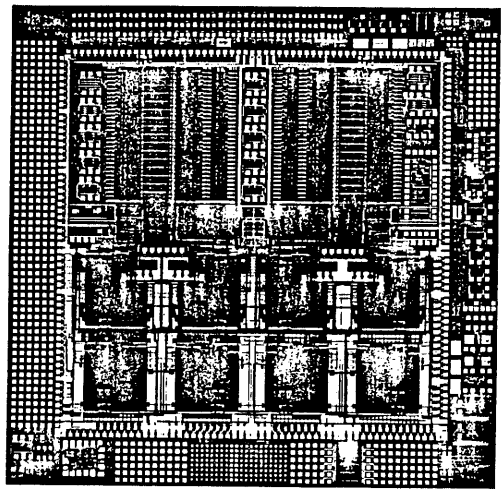
(2) Interlock bus with SC

(3) Split bus with Interleaved SC

Simulation results of three on-chip cache models



Photomicrograph of experimental chip



8.0 x 8.1mm

0.3 μm BiCMOS

1.02 MTrs.
(Bip. 20 KTrs.)

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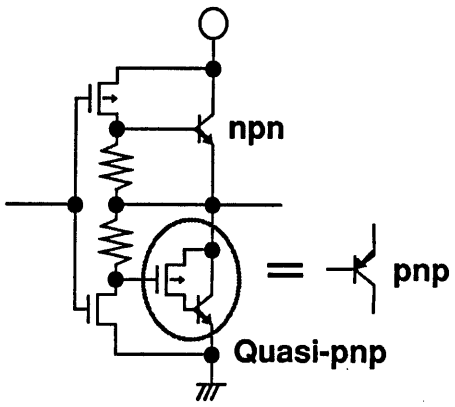
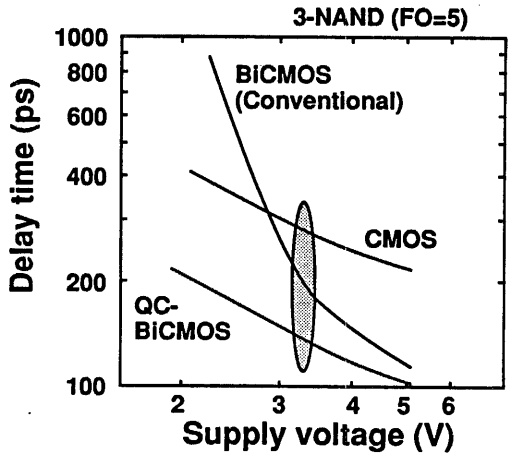
2 INT UNIT
2 8KB POWER cache

QC-BiCMOS circuit and delay time



QC-BiCMOS circuit



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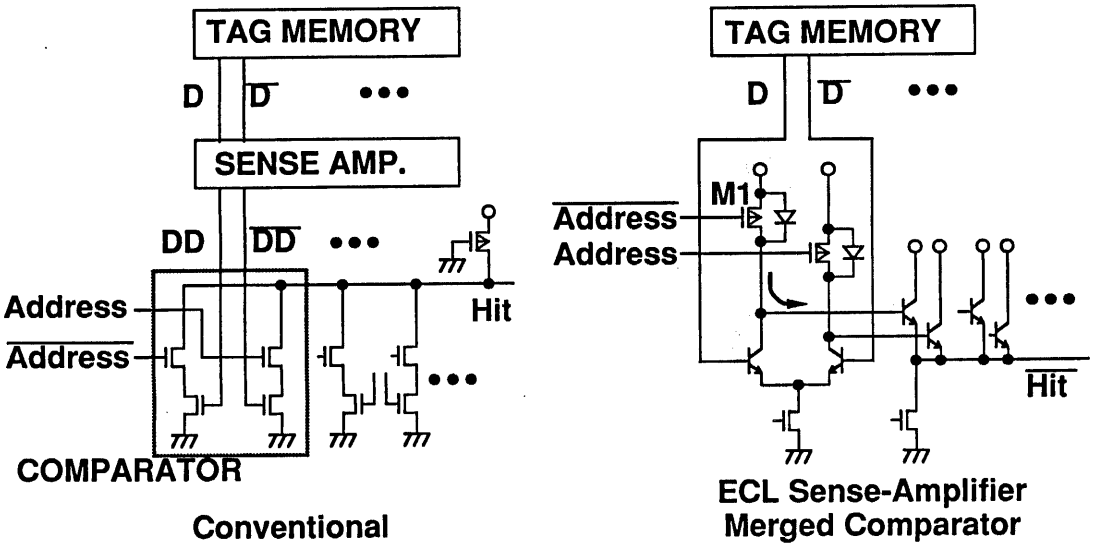
Cache / TLB tag comparator



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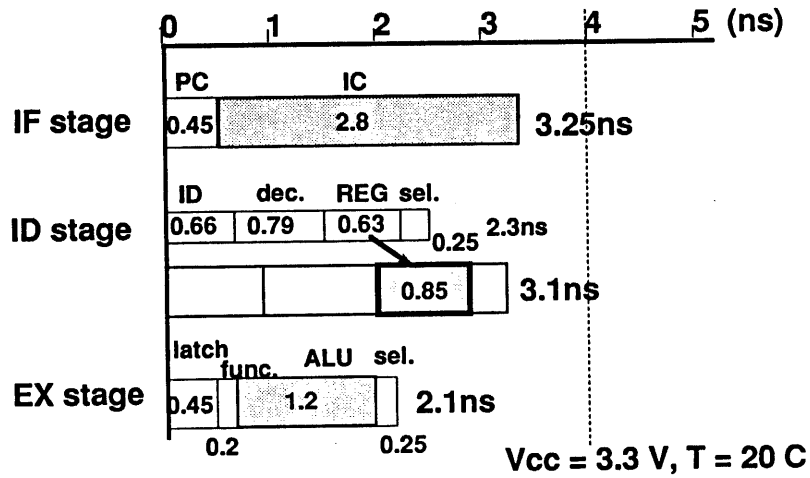
QUESTION: 3 VERSIONS SHOWN @ JSSC, ISSCC, ITRPG ALL DIFFERENT.

ASSUMED ~40W

Critical path delays



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Conclusion

A 250MHz, 1000MIPS multi-superscalar processor using QC-BiCMOS

Featuring

- On-chip interleaved secondary cache memory
- ECL-sense amplifier merged comparator and selectors

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