

# ***Multiprocessor Features of a PA-RISC Processor Interface Chip***

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**Hot Chips IV  
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Stanford, California**

- ***Introduction***
- **System Organization**
- **Multiprocessor Features**
- **Performance Results**
- **Summary**

## ***Design Goals***

- **General Purpose Multiuser System**  
Technical and Commercial Applications
- **Scalable Performance**  
Uniprocessor to > 8-way Multiprocessor
- **Platform for Multiple Generations of Systems**  
Independent Upgrades of Processor,  
Memory and I/O

## ***Design Approach***

- **Processor**  
High integer and FP throughput  
Large first-level external cache
- **Memory**  
Large physical memory  
Highly interleaved
- **I/O**  
High connectivity to mass storage  
High bandwidth bus adapter
- **Bus**  
Low latency  
High bandwidth

*1-4MB  
first level*

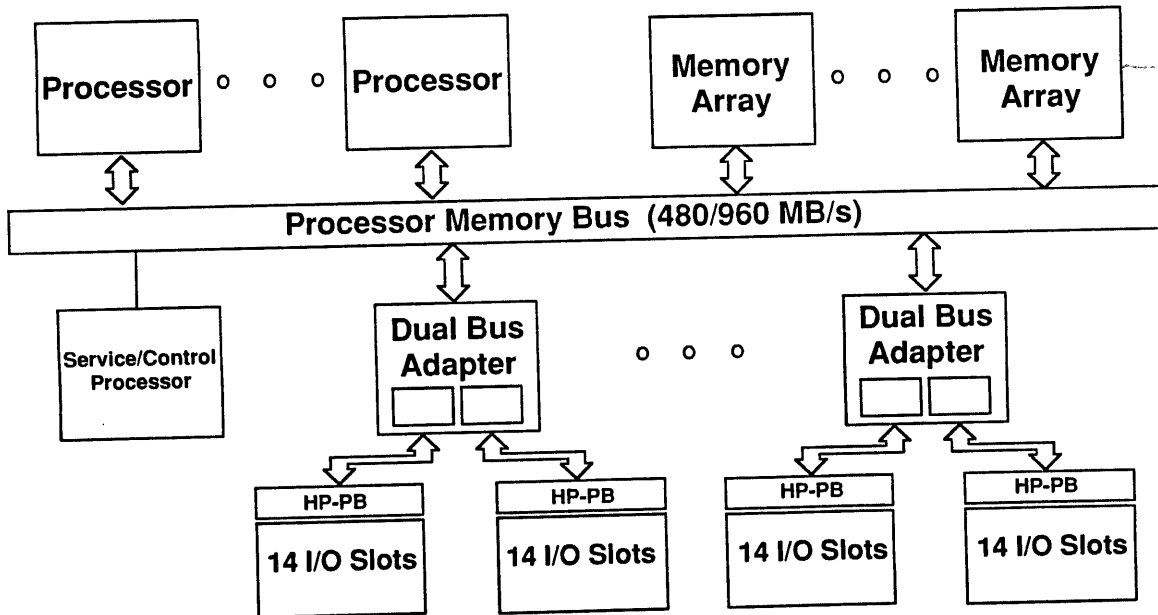
*LOW*

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- DO min DMA RETURN, CACHE SNOOPS ITING TO OCCUR AT THE SAME TIME?  
 - IS DIRTY PAGE PURG 2x min ACCESS?

## System Organization

- Shared memory snoop.  
 - WING VMSO, CUSTOM OPERATIONAL LOGS



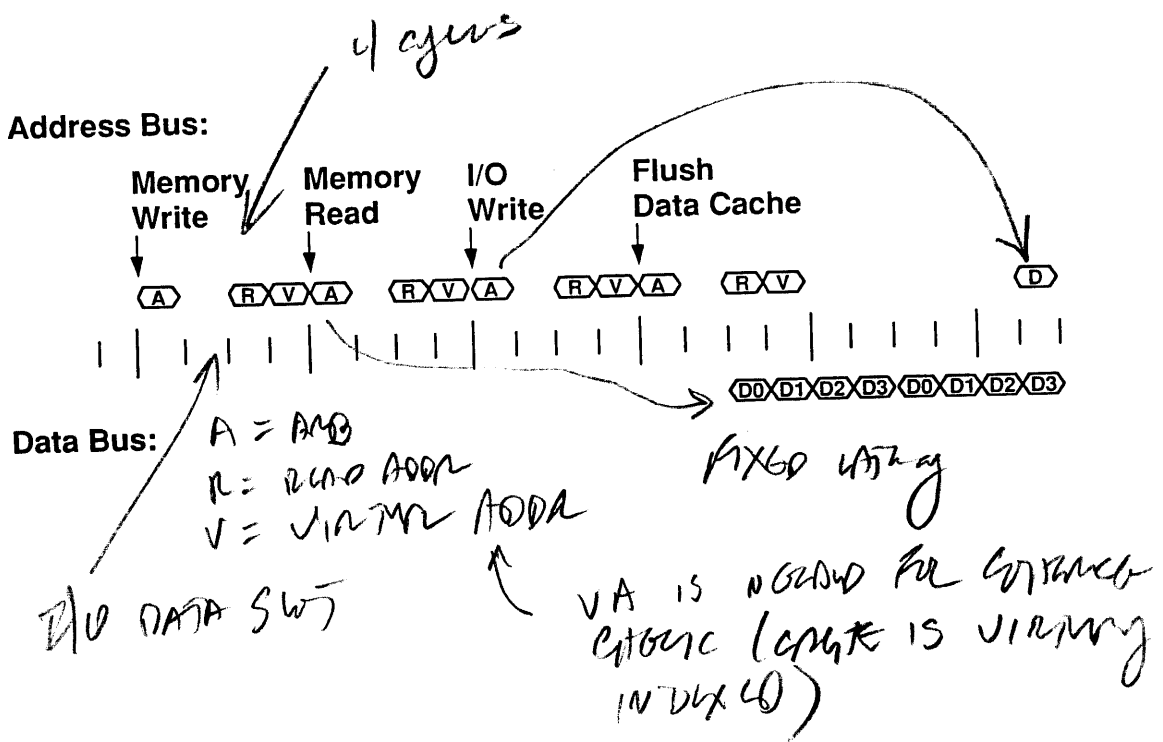


# Bus Specifications

- 16-slot backplane
- 60-MHz worst case frequency - *fully loaded, we can handle*
- 960 or 480 megabyte/second bandwidth - *128 or 64 bits*
- 128-bit or 64-bit data bus
- Separate data and address paths
- Data protected with ECC, address with parity

- DMA IS CRITICAL COMPONENT

## Synchronous Pipelined Bus



# Bandwidth Enhancement Features

- Flexible memory interleaving
  - Up to 64-way interleaving for each of 3 groups
- \* Unified memory interleaving among non power of 2 modules
- Resource-driven arbitration
  - Memory block status maintained by masters
  - Transactions not queued by memory
- Slave-driven arbitration
  - I/O re-arbitrates when data available

*Very similar to L2*

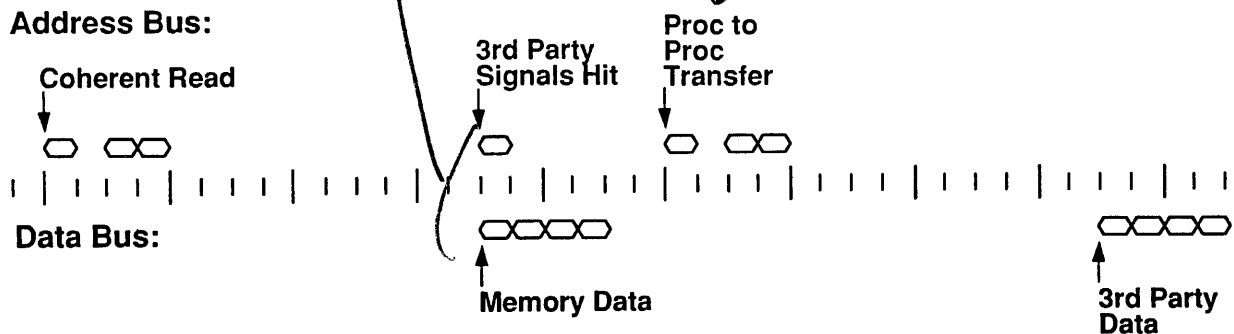
*NO! 64MB WORKING  
MEM ACCESS  
INDEPENDENT, 1st STAGE  
W/OUT MASTER  
MEM ACCESS - 200ns*

*Try as much as possible, for work up SIMULTANEOUS*

## Cache Coherence Transaction

- Bus protocol for cache and TLB coherence
- Processor-to-processor data transfer

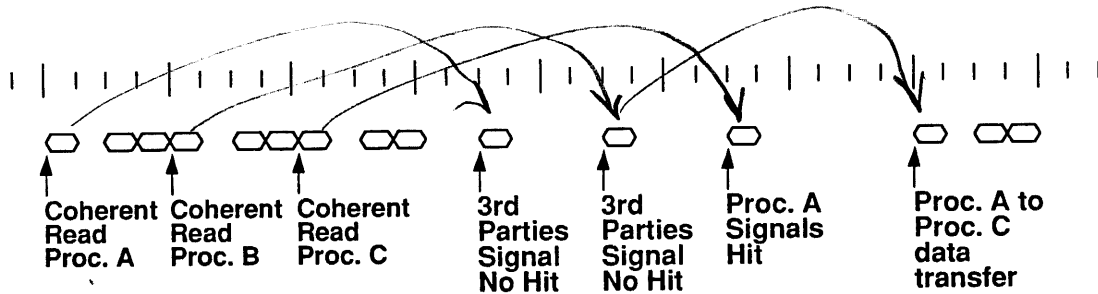
*Additional delay*



- Master Processor
- 3rd Party Processor
- Memory

# Cache Coherence (cont'd)

- Snoopy cache coherence with duplicate cache tags
- Multiple outstanding coherence checks

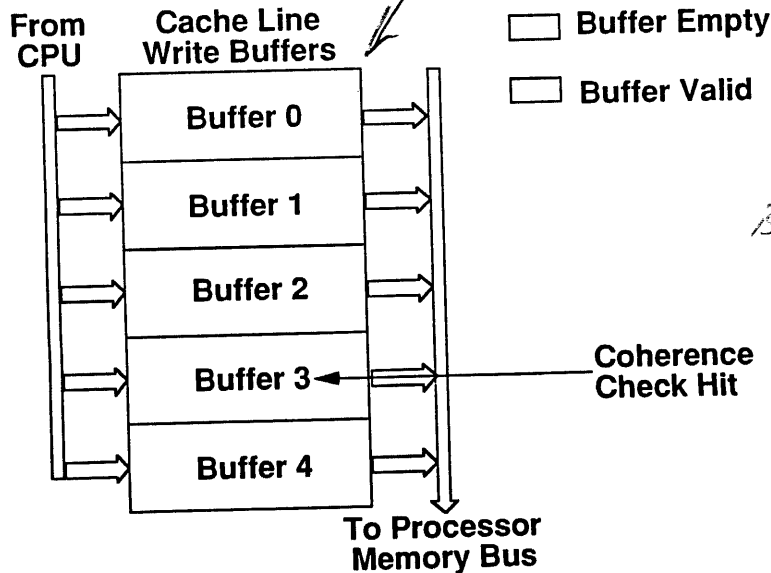


■ Processor A  
 ■ Processor B  
 ■ Processor C

*- Bus reads not into CPU*  
*write*  
*- CPU L1B size is 32 bytes.*

## Write Buffers

- Circular FIFO with random access



*3 required for bus polling.*

*HITS in buffer sufficient for hit*

# Multiprocessor Tuning Features

- Configurable bus parameters
  - Memory latency and cycle time
  - Coherence check
  - Interleave factor
- Pipeline freeze capability ← USED, E.G. FOR PARALLEL  
SUPPORT IN QCA CODES
  - Coherence exception conditions
- Performance monitoring counters
  - Multiprocessor events ← 16 EVENTS
- Support multiple generations of CPUs
  - ↳ BOOTH JURA
  - 7100 IN JAT
  - LAB

## die photograph

335 SIGMUS (D/O LINDO)  
60MHZ OPERATE  
PGA (MISSED SIZE)



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90% @ 1.750c

TPCA - 578 TPS (4-way, 60Mz CPU, 60Mhz BUS)				
SPEC RATE	1174	2360	3529	4685
FP 92	(1.0)	(2.01)	(3.0)	(3.99)
SPEC RATE	1164	2253	3306	4301
INT 92	(1.0)	(1.94)	2.84	(3.70)

→ study (Compass, Acc Don't scale with  
 Pkg to disk (MIPS)

**Performance Results** For PA RISC 1.0 (NOT 7100)

This slide will present UP  
 and MP performance results.

## ***Summary***

**Demonstrated a highly scalable  
many-way MP system using high  
performance RISC CPUs**

**Achieved 8-way MP with first silicon**

*Drawn out of 9 months.*