A 200MFLOP

Precision Architecture Processor

William Jaffe, Bob Miller, Jeff Yetter

Hewlett-Packard

Fort Collins, Colorado

HOT CHIPS IV

TALK WITH JAFFE:
- PROBABLY WILL MOVE TO ON-CHIP CACHES IN SUBSEQUENT GENERATIONS
- HAVING UNDERSTANDING WITH OUT-OF-ORDER EXECUTION COMPILER
- INTERFACE CHIP BUS PROTOCOL FOCUSES MUCH MORE ON DATA THAN CACHE BLOCK SIZE => SET UP FOR MUCH LARGER BLOCKS
- JOHN SOUL FROM APPLE LEFT FOR STARTUP; WITH TIMING TRADE SIMULATOR RULE.
- "ALMOST DONE WITH 1-CYCLE IMB CACHE", ESPECIALLY FOR COMMERCIAL SYSTEMS

WSJ/ea/920626A

HEWLETT PACKARD

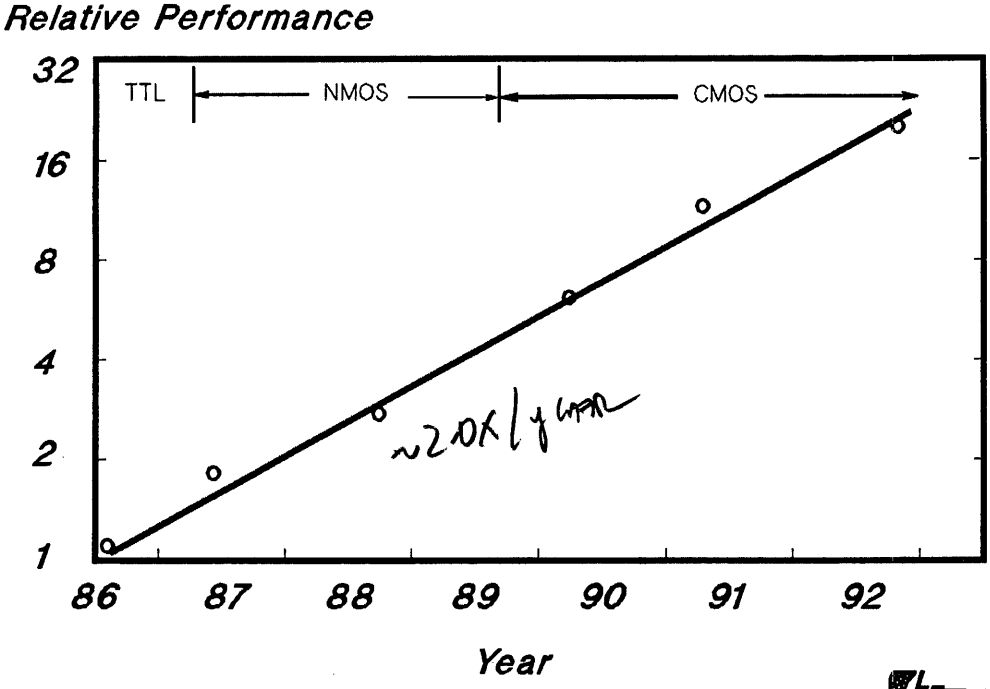
HP Processor Family

1986	*TTL*	*series*	*800*	*900*	
1987	*NMOSIII*	*series*	*800*	*900*	
1988	*NMOSIIIB*	*series*	*800*	*900*	
1990	*CMOS26*	*series*	*800*	*900*	
1991	*CMOS26*	*series*	*800*	*900*	*700*

WSJ/ea/920626B

HEWLETT PACKARD

Quest for Performance Improvement



wsj/920626c

HEWLETT PACKARD

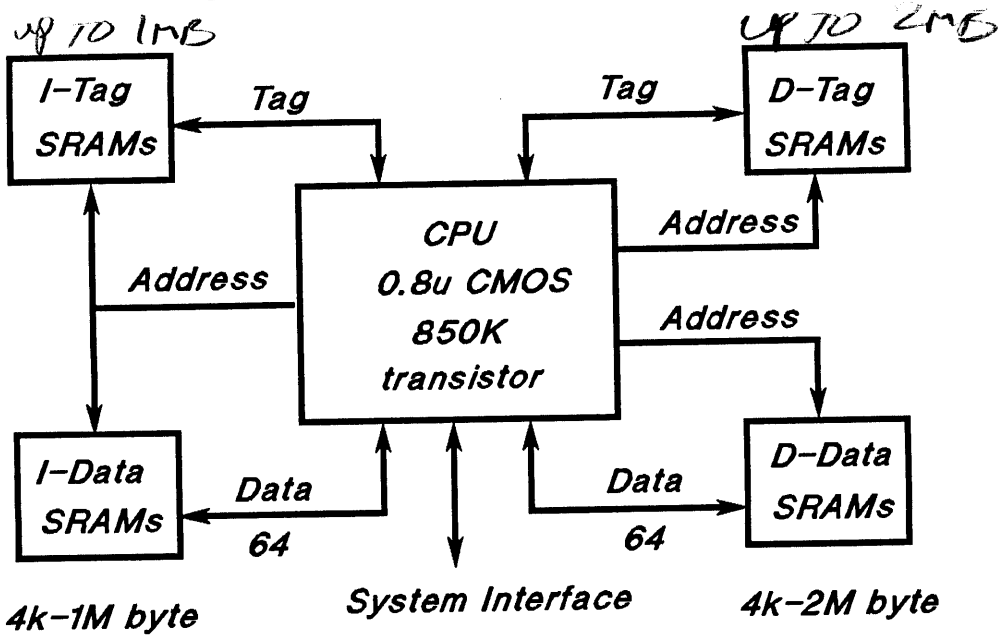
Design Goals

- *Price/Performance Improvement*
- *Scalability* (HIGH-END MP, WORKSTATIONS)
- *Compatibility* (WITH PREVIOUS GENERATIONS MANY SUBSYSTEMS)
- *Time to Market*

WSJ/ss/920626D

HEWLETT PACKARD

System Block Diagram



WSJ/ss/920020E

HEWLETT PACKARD

Chip Vital Statistics

Architecture	PA-Risc v1.2
Frequency	0-100MHz
I-Cache	4k-1M, hashed virtual indexed 64bits wide, 32 byte line
D-Cache	4k-2M, hashed virtual indexed 64 bits wide, 32 byte line
Physical Memory Address	32 bits
Virtual Memory Address	48 bits segmented
TLB	Fully associative, unified 120 page entries, 16 block entries 128-16K pages

WSJ/ss/920020F

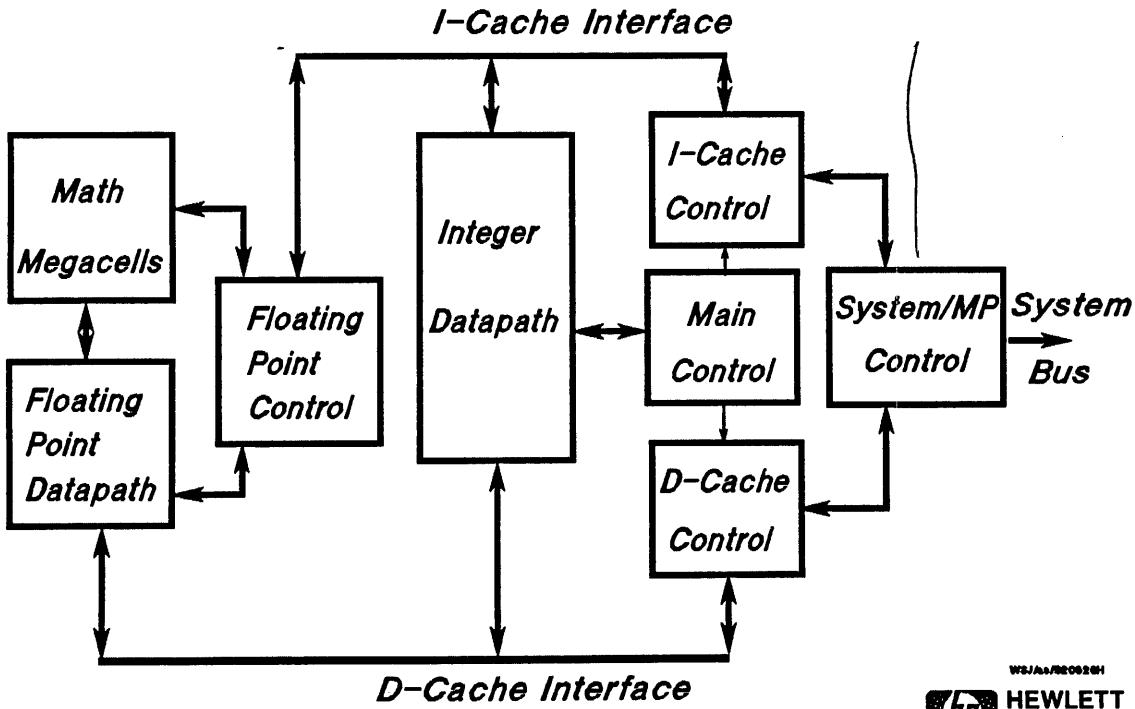
HEWLETT PACKARD

Technology Overview

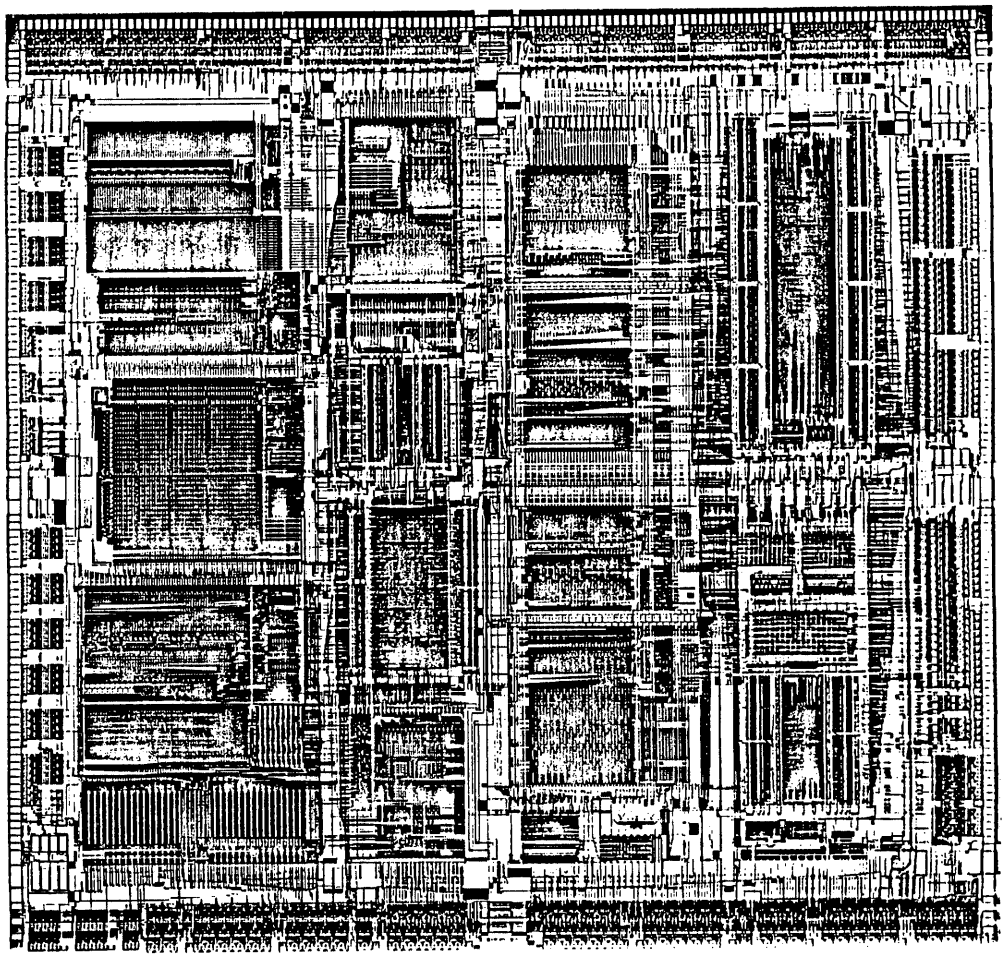
Technology	CMOS26B 0.8 micron drawn
Transistor count	850K
Die Size	14mm x 14mm
Interconnect	1 Silicide Poly
Interconnect	3 Levels Metal Aluminum
Power	5v internal
	3.3v I/O
	20W at 100MHz
Pad Count	520
Package	504 pin PGA

HEWLETT PACKARD

CPU Block Diagram



HEWLETT PACKARD



Design Methodology

- Leverage 66+ MHz Design
- Scale to 100MHz with Process shrink
- Incorporate Characterization Data
- Redesign Critical Circuits
- Add Enhanced Features
- Design on Chip Floating Point
- Faster Rams

Starting Feature Set

Integer Unit

- *Branch Prediction*
- *Extensive Bypassing*
- *Shadow Registers for TLB Miss Traps*
- *Cache Streaming* – BOTH I, D – NO CRITICAL WORD FIRST – BYPASS REQUESTED WORD TO BY REQUESTOR

Cache and TLB

- *Large off Chip I and D cache*
- *Virtual Index Hashing*
- *Fully Associative Split I/D*
- *96 Page and 4 Block Entries*

WSJ/ss/920626J

HEWLETT PACKARD

Feature Set Enhancement

- *On Chip Floating Point Unit*
- *Dual I Fetch for Superscalar*
- *Cache Miss Optimizations (Stall-on-Use)*
- *Block Copy Hint*
- *Fully Associative Unified TLB*
- *120 Page and 16 Block entries*
- *Hardware TLB miss handler* – FIRST LVL WORKUP
- *Low cost 2-way MP functionality*

WSJ/ss/920626L

HEWLETT PACKARD

FPU FUNCTIONS

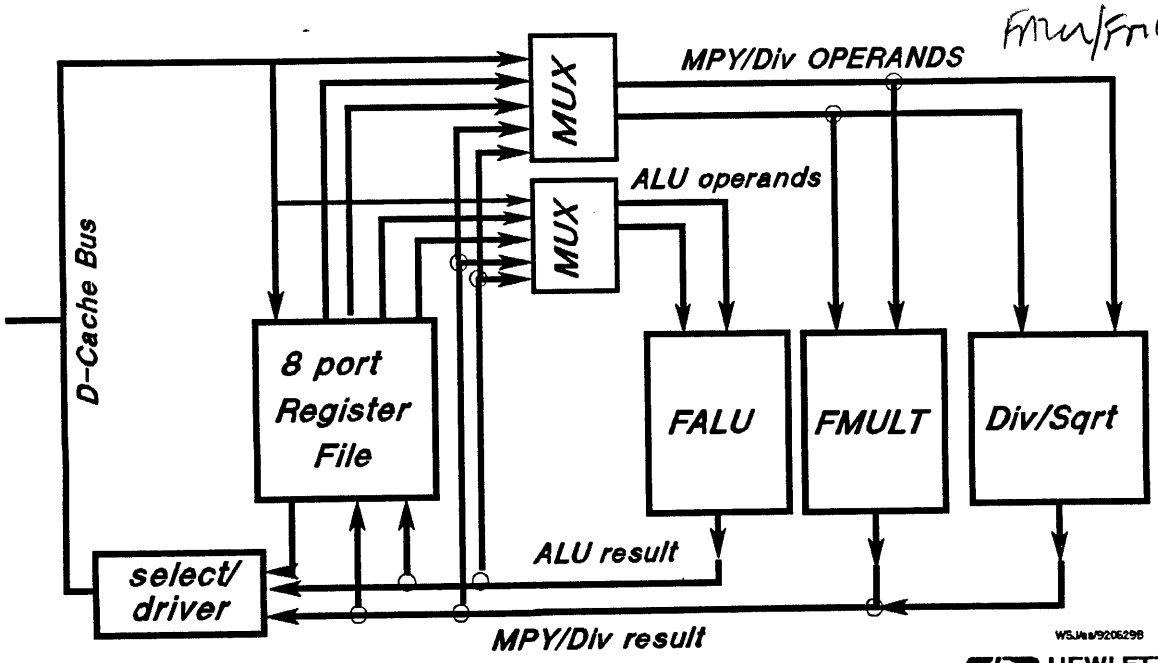
ALU Functions:	○	*Sgl/Dbl*	*Add/Subtract*
	○	*Sgl/Dbl*	*Compare/Complement*
	○	*Sgl/Dbl*	*Convert*
			(float -> int)
			(int -> float)
			(float -> float)
MPY Functions:		*Sgl/Dbl*	*Multiply*
		32-bit	*Integer Multiply*
Div Functions:		*Sgl/Dbl*	*Divide*
		Sg./Dbl	*Square Root*

WSJa/920629A

HEWLETT PACKARD

FLOATING POINT BLOCK DIAGRAM

DIV/SQRT does not share FMULT/FMULT



WSJa/920629B

HEWLETT PACKARD

Floating Point Instruction Timing

Latency/Dispatch (Cycles)

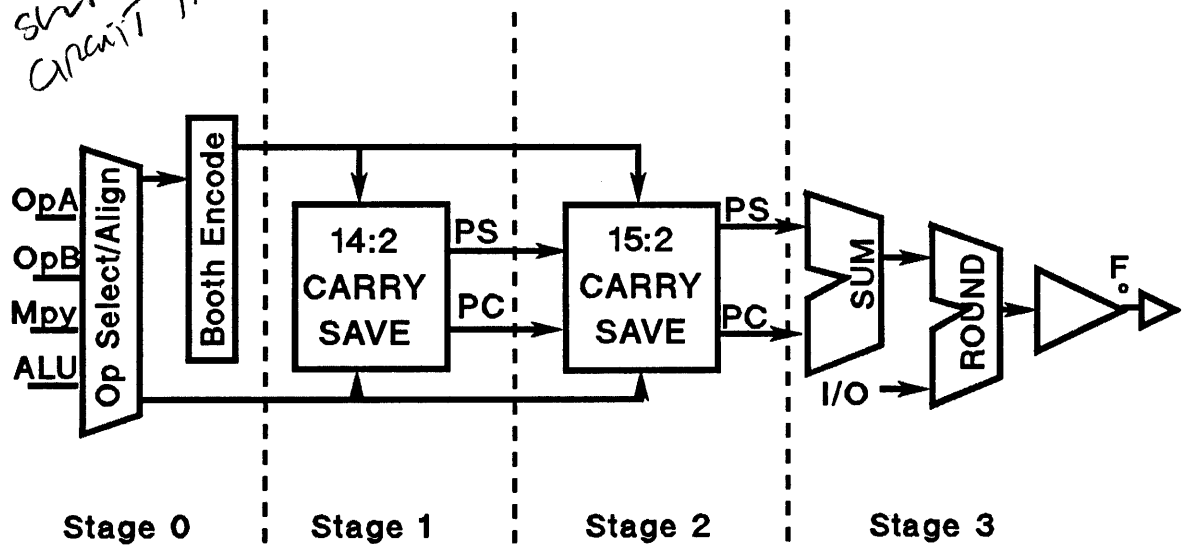
	Single Precision	Double Precision
ALU	2/1	2/1
Multiply	2/1	2/1
MPY/ALU	2/1	2/1
Divide	8/8	15/15
Square Root	8/8	15/15

200 Mflop Peak Performance at 100MHz(MPY/ALU)
Superscalar Execution with an Integer Instruction

WSJ/ss/920626N

HEWLETT PACKARD

MPY ORGANIZATION



WSJ920630B

HEWLETT PACKARD

Superscalar Execution

Instruction Pairs: A - E

E - A

E - B

A: Integer Operation

Integer Load or Store

Floating Point Load or Store

B: Branch

E: Floating Point Operation

- No Alignment Constraints

HEWLETT PACKARD

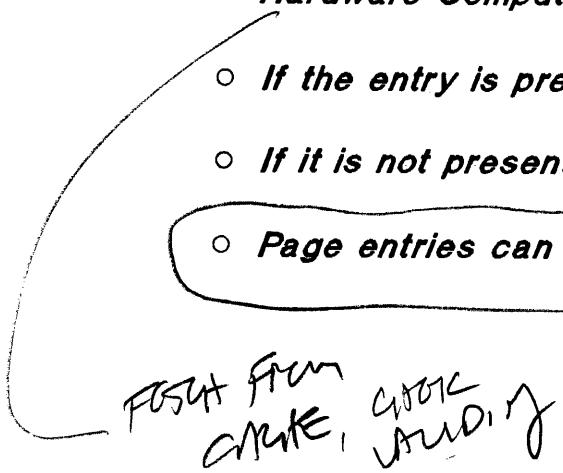
Cache Miss Optimizations

- *Stall-on-use (Hit Under Miss)*
  - *Hides Miss Penality*
  - *Implemented for loads and stores*
  - *Will Stall only for register dependency or another Miss*
- *Implemented "don't fill" cache hint*

HEWLETT PACKARD

Hardware TLB Miss Handler

- *Invoked on I/D translations that miss the on chip TLB*
- *Hardware Computes the PDIR entry address*
- *If the entry is present and vaild, it is inserted on chip*
- *If it is not present or vaild a software trap is taken*
- *Page entries can be updated in 11 states*



WSJss/920626R

HEWLETT PACKARD

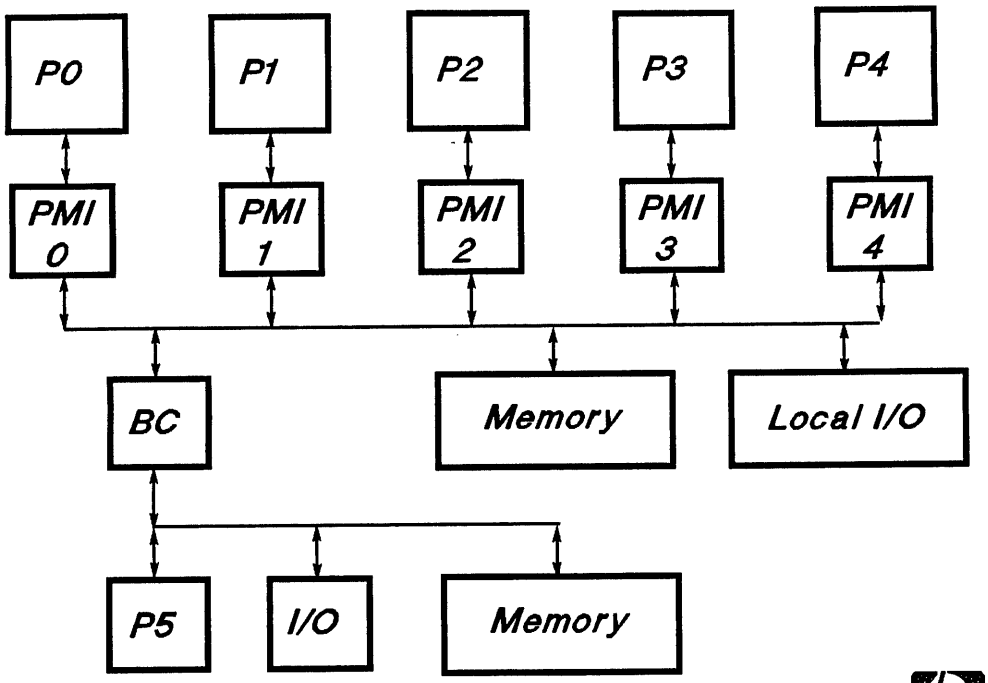
Multiprocessor Configurations

- *Full compatibility will all previous MP implementations*
- *Scalable High End*
- *Low cost 2-way Implementation*

WSJss/920626S

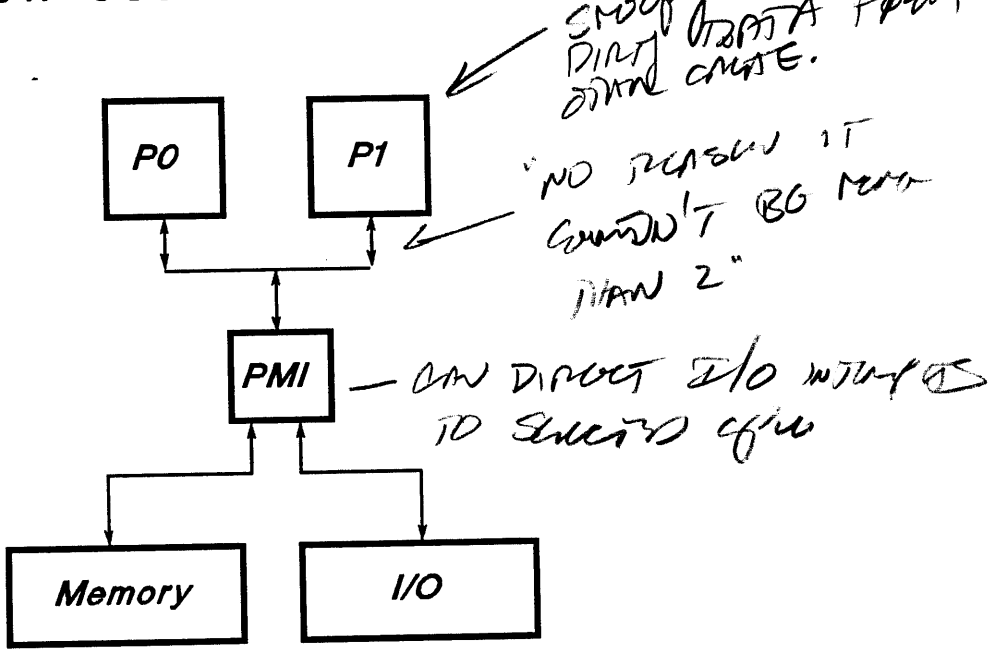
HEWLETT PACKARD

Scalable MP Configuration



HEWLETT PACKARD

Low Cost Dual Processor



HEWLETT PACKARD

2-Way Implementation

- *No Memory support or changes required*
- *Minimal Implementation Specific OS Impact*
- *All MP functionality is contained on the CPU*
- *Cache and TLB coherency over local Memory-IO bus (P-bus)*
- *Logic handles 3 freq ratios between the processor and the external P-bus*

WSJ/ss/920626T

HEWLETT PACKARD

Benchmark Performance

This slide will share the performance

of key Benchmarks

SPEC 89 >130

SPECINT92 >70

FP92 >130

mFWPS (LINPACK) >30

PEAK mFLOP 200

MIPS 115

CRAY BENCHMARK < 14 SEC

WHETSTONE SP ~160

DP ~150

100MHz WSJ1

256KB CACHE

9NS 32K x 8

WSJ/ss/920626X

HEWLETT PACKARD

Growth Paths

- *Process Improvements*
- *Faster Cache Chip Technology*
- *Circuit Enhancement*
- *More Compiler use of New Features* – EXPLOIT HIT-under-MISS, OTC.

WSJ/ss/920626Y

HEWLETT PACKARD

Summary

- *Scalable PA-RISC processor for Workstation and Multiuser*
- *Continuation of HP Processor Family*
- *Single Chip Solution*
- *Frequency as well as feature enhancements*
- *On Chip Floating Point*

WSJ/ss/920626Z

HEWLETT PACKARD