RAM PANEL DISCUSSION

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HIGH END.
TYPICAL SYSTEM DESIGN HAS HIGH THEORETICAL BANDWIDTH, LIMITED BY PROTOCOLS, DECODE, MUXING, ECC, ETC. EFFECTIVE BUS USAGE ~50% WITH UP TO ~75% WITH DEEP INTERLEAVING. MIGHT GET 2 READ ACCESSES OUT OF DRAM EVERY 200NS.

FOR WS, LESS AGGRESSIVE (BUT STILL SUBSTANTIAL) BANDWIDTH OK FOR AVERAGE MODES, BUT PEAK REQUIREMENTS (E.G., CACHE FILL) SATURATE MEMORY BUS.

PROBLEMS:
- ACCESS TIMES STILL BE LOW
- BANDWIDTH OF CPU ISN'T MATCH IT OUT INTERFACES
- WIDER DRAMS DESIRABLE FOR LOW COST SYSTEMS
- RAM SPEC COULD BE TIGHTER.

RAMBUS 512K X 9 IS 14% LONGER THAN NORMAL RAM. @16Mb = 10%, 64Mb = 5%

RAM LINK: CONTROLLER WITH RING OF DRAMS
FTP LINK hplsci.hpl.hp.com

MITSUBISHI CDRAM: TRY TO IMPROVE LATENCY & BANDWIDTH: CACHE ON DRAM; ADDS 4K x 4 SRAM TO 4M x 4 DRAM. CAN THIS BE DONE OUTSIDE DRAMS ON DOUBLE INTERFACE PROVIDER DOMINATE THIS?

TI SYNCHRONOUS DRAM: NORMAL DRAM WITH CLOCKED INPUT & OUTPUT.

RAMBUS ACCESS IS ~150-200 NS NOW BECAUSE HAVE TO DO A PRECHARGE BEFORE THE ACCESS. 16M SIZE IS ~100 NS. RAM LINK SEEMS TO BE MUCH FASTER.

* CAN ~~ATEKS121~~ ALL CACHE ARCHITECTURES BE COMBINED WITH ICSRI TO IMPROVE PERFORMANCE.