August 9, 1992 — Memorial Hall Auditorium

HOT CHIPS

Sunday Tutorial
Professor Mark D. Hill

Topic: A Quantitative Approach to Microprocessor Architecture

This four-hour tutorial will review the principles of computer architecture, emphasizing microprocessor considerations. The presentation will be strongly based on *Computer Architecture: A Quantitative Approach* by John Hennessy and Dave Patterson, and will concentrate on caches and pipelining. Some more recent material will also be presented. Hill is an assistant professor at the University of Wisconsin, Madison, and a 1989 recipient of NSF's Presidential Young Investigator Award. The Sunday tutorial is a new event at HOT Chips. There is a $10 fee for attendance.

10:00 – 11:00	**Registration at Memorial Hall**
10:30 – 11:00	**Pastries and Coffee**
11:00 – 1:00	**First Half of the Tutorial**
1:00 – 1:30	**Break for Light Refreshments**
1:30 – 3:30	**Second Half of the Tutorial**
3:30 – 5:00	**Guided Tours of the Hoover Tower**
4:30 – 7:30	**Wine & Cheese Reception in the Dohrmann Grove near the Hoover Tower**

Additional On-Site Registration will be available for an hour before the sessions begin on Monday and Tuesday.

August 10, 1992 — Memorial Hall Auditorium

Monday

8:45 – 9:00 **Welcome and Opening Remarks**
Glen Langdon, General Chair
David Patterson and John Mashey, Program Co-Chairs

9:00– 10:15 **Session 1: High-Performance Processors – 1**
Session Chair: David Patterson, University of California, Berkeley

- **DEC Alpha Architecture and 21064 Chip**
  E. McLellan, Digital Equipment Corporation
- **A 200 MFLOP HP PA-RISC Processor**
  W. Jaffe, B. Miller and J. Yetter, Hewlett-Packard

10:15 – 10:45 **Break**

10:45 – 12:15 **Session 2: Multiprocessor Interface Issues**
Session Chair: Ruby Lee, Hewlett-Packard

- **Multiprocessor Features In a PA-RISC Processor Interface Chip**
  T. Alexander, K. Chan, C. Hu, N. Noordeen, and S. Ziai
  Hewlett-Packard
- **On-Chip Cache Hierarchy for 1000-MIPS Multi-Superscalar Processors**
  T. Nishimukai, M. Hanawa, O. Nishii, M. Suzuki,
  K. Yano, and M. Hiraki, Hitachi
- **Sparcle: Today's Micro for Tomorrow's Multiprocessor**
  A. Agarwal, MIT

12:15 – 1:45 **Lunch at The Tent**

1:45 – 3:15 **Session 3: Low Cost Processors**
Session Chair: John Mashey, Silicon Graphics

- **Highly Integrated SPARC Processor Implementation**
  S. Joshi, Sun Microsystems
- **The LR33020 GraphX Processor: A Single Chip MIPS-RISC Based X Terminal Controller**
  S. Desai, LSI Logic Corporation
- **The ARM600 Processor and FPA**
  M. Muller, Advanced RISC Machines Ltd.

3:15 – 3:45 **Break**

3:45 – 5:15 **Session 4: Low Power Systems**
Session Chair: Dave Ditzel, Sun Microsystems

- **A VLSI Chip Set for Personal Communications System**
  R. Scavuzzo, AT&T Bell Labs
- **SPARC90 - Chipset on a Chip**
  J. Pendleton, Sun Microsystems
- **Cold Chip Design Techniques**
  R. Broderson, A. Chandrakasan and S. Sheng, UC Berkeley

5:15 – 7:00 **Reception Dinner at The Tent**

7:15 – 9:30 **Evening Panel Session**

DRAM Choices for the '90s: 1 Gigabyte/Second or Bust
Chair: Skip Stritter, Silicon Graphics

- Rambus — M. Horowitz, Stanford
- Ramlink — D. James, Apple
- Synchronous DRAM — W. Vokley, TI
- Cache DRAM — C. Hart, Mitsubishi

Program Committee

Co-Chairmen: David Patterson, UC Berkeley and John Mashey, Silicon Graphics

Teresa Meng, Stanford University
Uri Weiser, Intel Corporation
David Ditzel, Sun Microsystems
Ruby Lee, Hewlett Packard

August 11, 1992 — Memorial Hall Auditorium

DAY 3

7:30	**Coffee and Donuts**
9:00 – 10:30	**Session 5: Interfaces and Interrupts** Session Chair: John Mashey, Silicon Graphics • **The SBus Goldchip** M. Sodos, Sun Microsystems • **Peripheral Component Interconnect** D. Carson, Intel Corporation • **Advanced Programmable Interrupt Controller (APIC) for MP and 32-bit Operating Systems** P.K. Nizar, Intel Corporation
10:30 – 11:00	**Break**
11:00 – 12:30	**Session 6: Vector and Video** Session Chair: Dave Patterson, University of California, Berkeley • **The Vector Coprocessor Unit (VU) for the CM-5** J. Wade, Thinking Machines Corporation • **A 289 MFLOPS Single Chip Supercomputer** C. Lund for H. Lino, H. Takahashi, T. Sukemura, M. Kimura, K. Fujita and S. Mori, Fujitsu • **A Programmable Solution for Standard Video Compression** J. Fandrianto and T. Williams, Integrated Information Technology, Inc.
12:30 – 2:00	**Lunch at The Tent**
2:00 – 3:30	**Session 7: Electrons, Photons, and Neurons** Session Chair: Teresa Meng, Stanford University • **Chip Pair Creates Self-Timed Network Fabric for Paragon Parallel Supercomputers** R. Traylor and D. Dunning, Intel Supercomputer Systems • **GaAs VLSI Enhancement through Utilization of Global Optical Free Space 'Smart' Interconnects** P. Guilfoyle and F. Zeise, OptiComp Corporation • **Silicon Based Nerve Interfaces** G. Kovacs, Stanford University
3:30 – 4:00	**Break**
4:00 – 5:30	**Session 8: High-Performance Processors – 2** Session Chair: Uri Weiser, Intel • **The Second Generation SPARCore Mbus Chip** M. Gutierrez, Ross Technology • **Superscalar Architecture of the P5 - X86 Next Generation Microprocessor** D. Alpert, Intel Corporation • **The P5 Floating-Point Unit** D. Avnon, Intel Corporation
5:30	**Closing Remarks**

Organizing Committee

General Chairman:
Glen Langdon, UC Santa Cruz

Program Co-Chairmen:
David Patterson, UC Berkeley
John Mashey, Silicon Graphics

Finance Chair:
Martin Freeman, Philips Research

Registration & Local Arrangements:
Robert Stewart
Stewart Research Enterprises

Publicity Chair:
Andre Goforth, NASA Ames Research Center

Publicity Committee:
Elaine Grimes, Elaine Grimes Graphics
Doug Marquart, Santa Clara University

Publication Chair:
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At Large:
Hasan AlKhatib, Santa Clara University
John Hennessy, Stanford University
Alan Smith, UC Berkeley