National's Swordfish

A Superscalar with DSP

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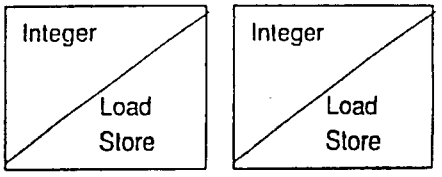
DP -1

National's RISC Philosophy

- Full RISC implementation to achieve highest raw performance
- Developed compiler together with processor to achieve optimal HW and SW tradeoffs
- On chip instruction/data caches to minimize wait states penalties
- Add on chip features targeted at embedded applications
- Simple bus interface to minimize system cost

Superscalar

2 SYMMETRICAL INTEGER PIPES
(ALMOST ANY TWO INSTRUCTIONS CAN
BE EXECUTED IN PARALLEL)



EXTERNAL DATA PATH OF 64 BITS

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True Superscalar

SWORDFISH

2 Symmetrical integer pipes (almost any two instructions can be executed in parallel)

External Data Path of 64 Bits

80960CA

Only certain instructions can be executed in parallel

External Data Path of only 32 birs (creates serious performance bottle-neck)

Load/Store Architecture

- Only load or store instructions access memory.
- All other instructions operate on registers.

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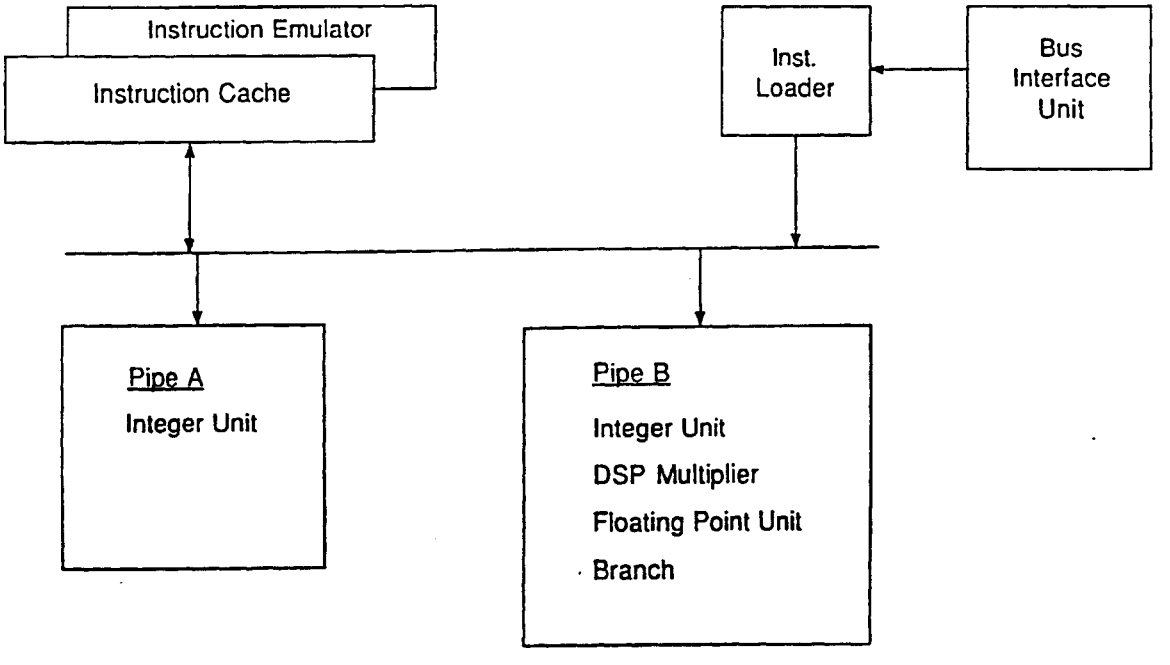
Swordfish Processor Architecture



Instruction Packing by the SF Loader

Most instructions can be paired, unless:

- One of the instructions is in a 64-bit format.
- One of the instructions is a special instruction.
- The first instruction is a branch, multiply or floating-point instruction.

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Instruction Packing Example

```
addd    r17,r23,r1      ;    subd    r23,r17,r23     ## 25 ; 26
ord     r1,c0,r17       ;    addd    r18,r2,r1       ## 27 ; 28
subd    r2,r18,r2       ;    ord     r1,c0,r18       ## 29 ; 30
addd    r19,r16,r1      ;    subd    r16,r19,r16     ## 31 ; 32
ord     r1,c0,r19       ;    addd    r16,r2,r9       ## 33 ; 43
addd    r22,r20,r1      ;    muld    r9,r26,r0       ## 34 ; 44
subd    r20,r22,r20     ;    subd    r16,r2,r9       ## 35 ; 47
ord     r1,c0,r22       ;    addd    r6,r0,r8        ## 36 ; 45
subd    r22,r17,r22     ;    muld    r9,r26,r0       ## 38 ; 48
addd    r17,r1,r1       ;    ord     c0,c0,c0        ## 37 ;
ord     r1,c0,r17       ;    addd    r18,r19,r1      ## 39 ; 40
subd    r19,r18,r19     ;    ord     r1,c0,r18       ## 41 ; 42
addd    r17,r18,r15     ;    subd    r18,r17,r9      ## 52 ; 56
ashud   $(-14),r8,r1    ;    addd    r6,r0,r8        ## 46 ; 49
ord     r1,c0,r2        ;    muld    r15,r26,r0      ## 51 ; 53
ashud   $(-14),r8,r16   ;    muld    r9,r26,r15      ## 50 ; 57
addd    r24,r0,r8       ;    muld    r19,r5,r9       ## 54 ; 62
addd    r24,r15,r0      ;    ashud   $(-16),r8,r1    ## 58 ; 55
ord     r1,c0,r17       ;    muld    r22,r27,r8      ## 60 ; 61
ashud   $(-16),r0,r18   ;    ord     c0,c0,c0        ## 59 ;
addd    r9,r8,r15       ;    muld    r22,r5,r9       ## 63 ; 66
addd    r15,r24,r8      ;    muld    r19,r14.r15     ## 64 ; 67
```

Branch Prediction

The CPU speculates on the outcome of the branch.

Static branch prediction (e.g. all branches are predicted taken) enables the compiler to generate the right kind of branch instructions.

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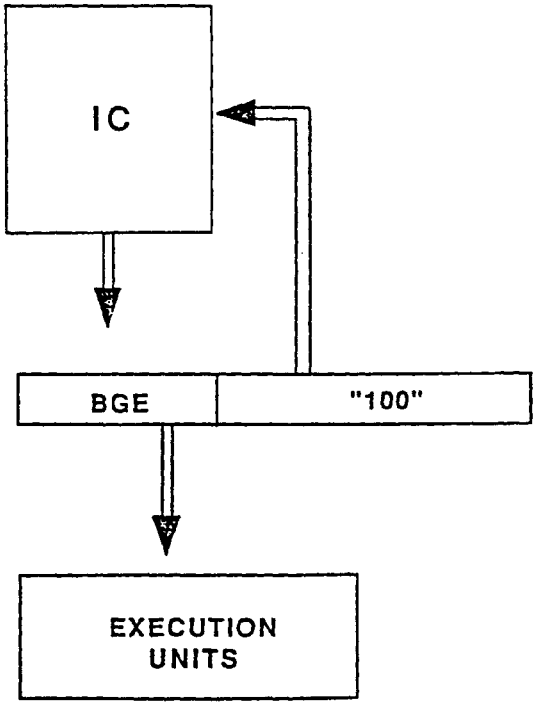
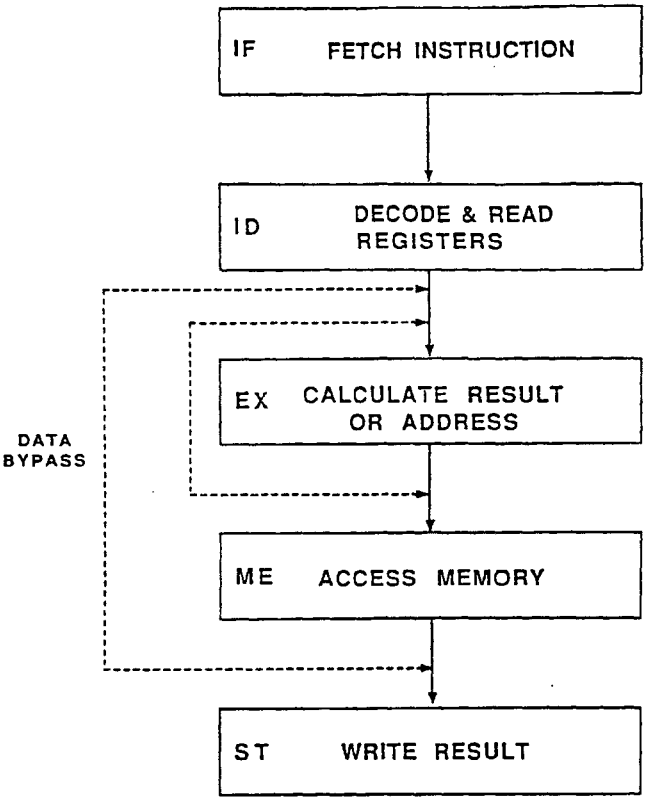
How Branch Delays are Avoided

The loader replaces : Branch, GE, -50
with : Branch, GE, "100"



Integer Pipeline Structure



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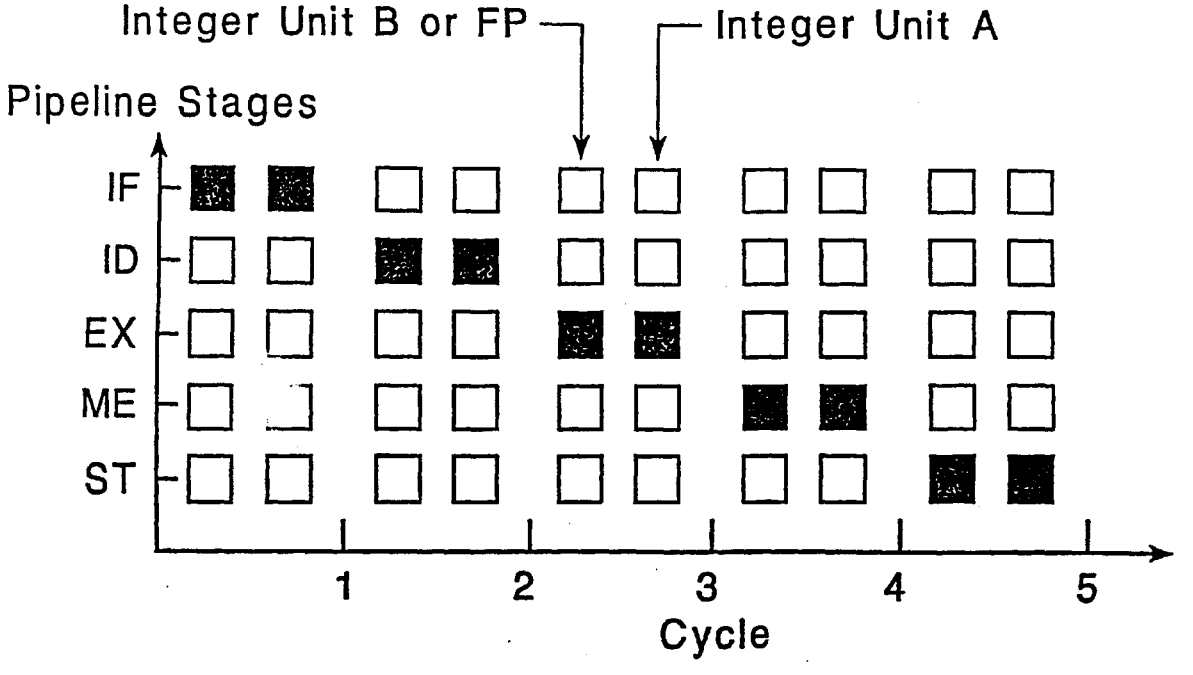
Parallel Execution



Three Operands Instruction Format

Pipe A					Pipe B				
Opc	Rs1	Rs2	Rd	Imm	Opc	Rs1	Rs2	Rd	Imm

Integer ALU

Load/Store

Integer ALU

Load/Store

FP Instr.

Branch/Jump

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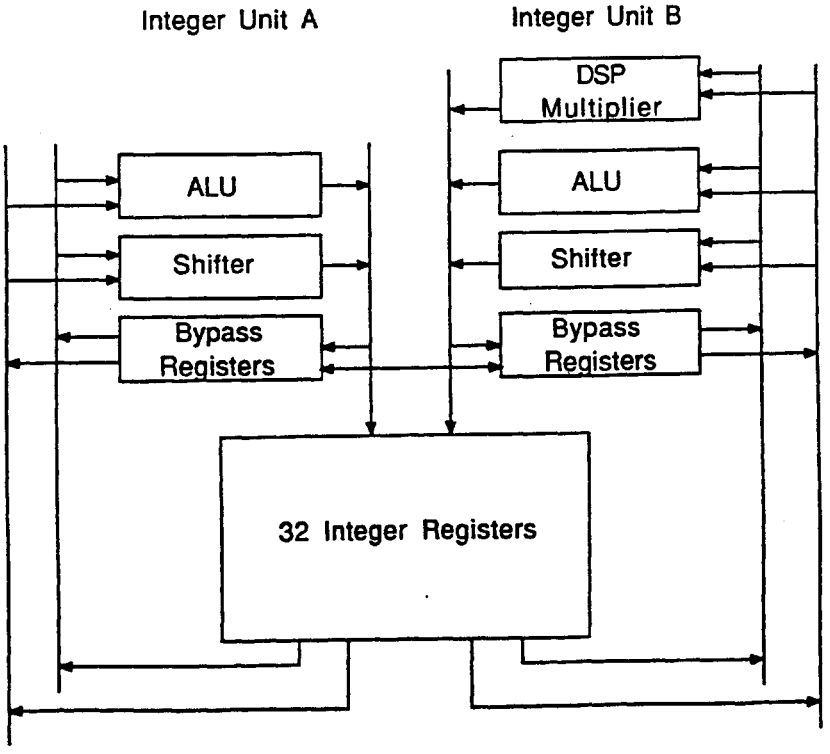
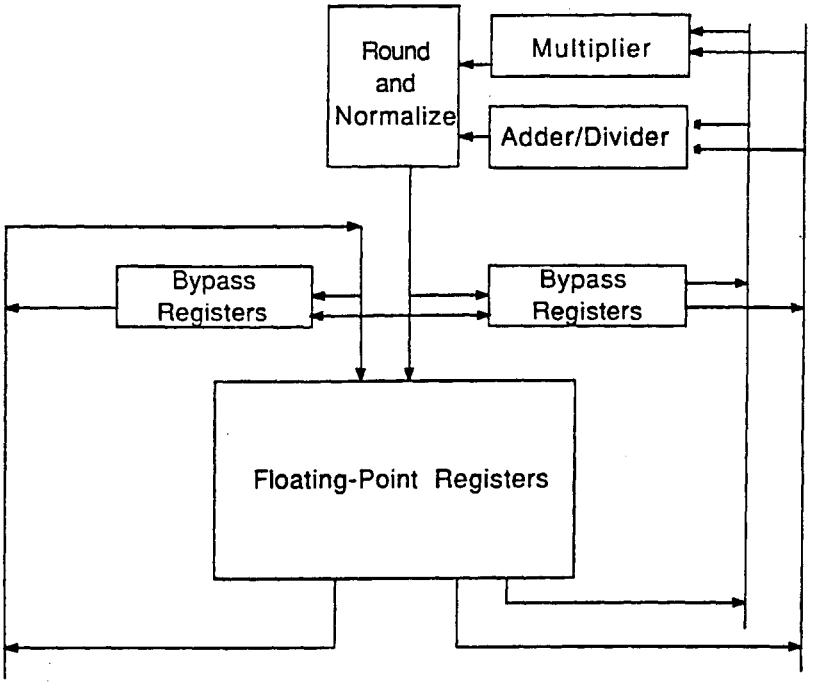
Dual Integer Unit



Floating-Point Unit



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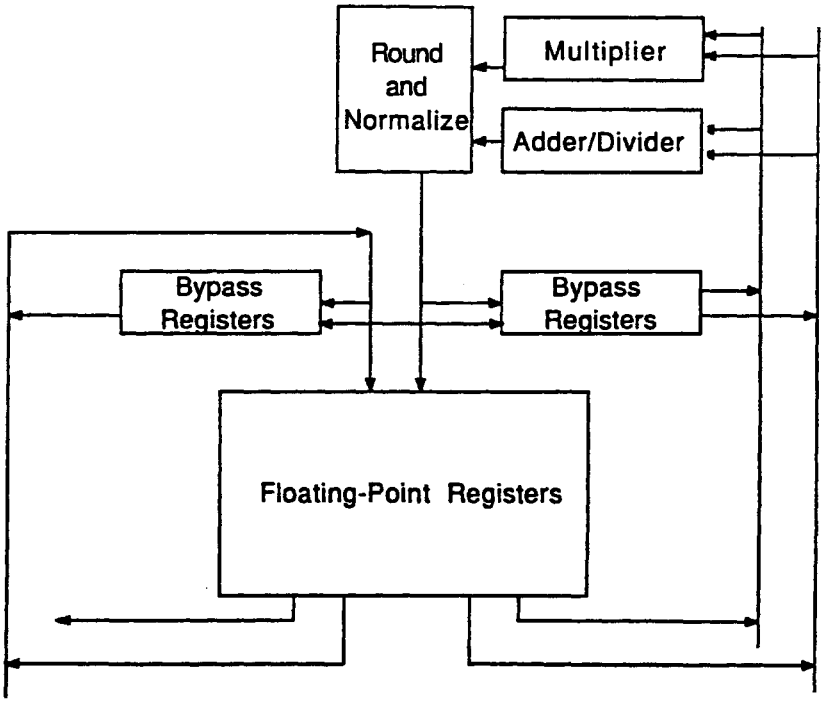
Floating-Point Unit



Added DSP Features

- Twin integer execution units support DSP.
- Wallace tree array multiplier executes in single cycle throughput
- Support for sequenced complex number calculations.
- Executable with high-level C compilers.

Bus Features

Performance

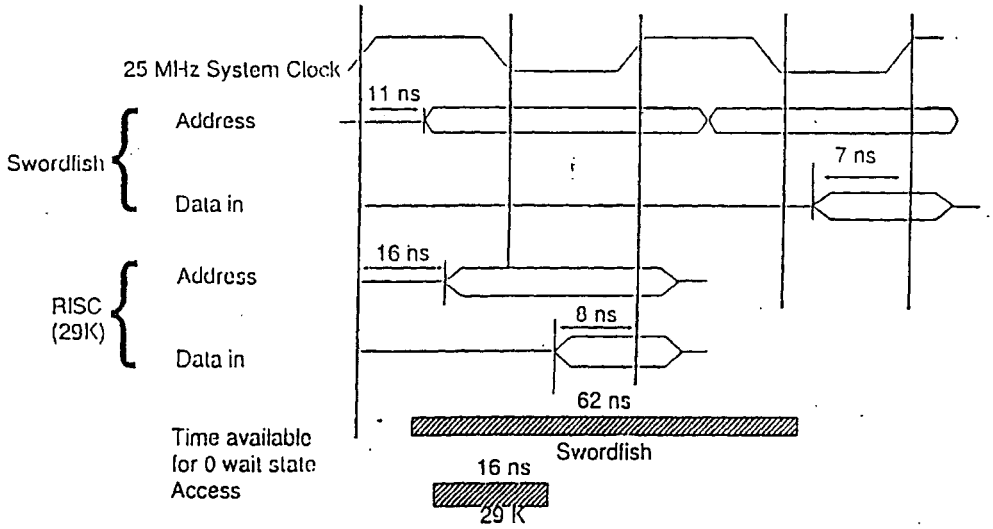
- 64-bit data
- Pipelined mode - 1-cycle throughput for address and data

Flexibility for Reduced System Cost

- Operates at half the internal clock frequency if required
- Supports interleaved memory configuration
- Interfaces directly to 8-, 16- and 32-bit buses
- Handles page-mode DRAMs

Other RISC Systems Require More Expensive Memories Than Swordfish Based Systems

0 Wait State Timing for Swordfish Operating at 50 MHz Internal Clock



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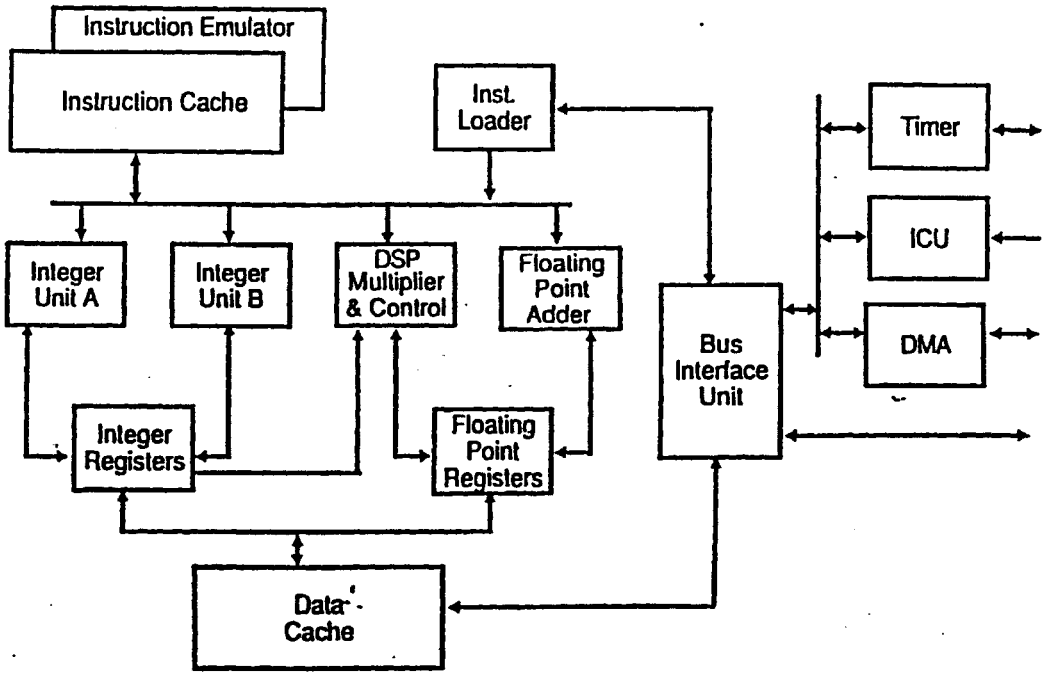
Swordfish Processor Architecture



Load Scheduling

- Load instructions do not block the CPU.
- Allows processing by the execution units to overlap external memory accesses.

Swordfish Technology

Description:	64-bit superscalar RISC Microprocessor
Process Technology:	0.8 micron CMOS
Compilers:	Very highly optimized
Size:	1.1 million transistors
Speed:	33 / 40 / 50 MHz
Package:	223 pins CPGA

Optimized Compiler

Tuned for the SF load/store superscalar architecture by:

- **Tuning register allocation**
- **Code reordering to cater to the SF pairing algorithm and reduce the number of pipeline interlocks**
- **DSP enhancements**

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Performance

BENCHMARKS

■ Dhrystone 1.1.	120.000 Dh/sec
■ Whetstone	21 MWh/sec (double precision)
■ Linpack (inner loop)	20 MFLOPS (double precision)

DSP	INTEGER	FLOATING POINT
■ 1024 Point FFT	1498 µsec	1025 µsec
■ FIR tap	0.03 µsec	0.04 µsec
■ Complex FIR tap	0.10 µsec	0.16 µsec

Integer DSP Performance

	1024 INT FFT (msec)	INT FIR (nsec/tap)	Complex Int FIR (nsec/tap)
TMS32020 @ 10 Mhz	31.8 (1.0)	200 (1.0)	800 (1.0)
NS32FX16 @ 25 Mhz	not available	320 (0.6)	320 (2.5)
NS32GX320 @ 30 Mhz	17.7 (1.8)	185 (1.1)	400 (2.0)
TMS320C25 @ 25 Mhz	14.0 (2.3)	80 (2.5)	320 (2.5)
TMS320C50 @ 57 Mhz	6.1 (5.2)	35 (5.7)	140 (5.7)
DSP56001 @ 26.7 Mhz	2.5 (12.7)	75 (2.7)	300 (2.7)
SWORDFISH @ 25/50 Mhz	1.5 (21.2)	30 (6.7)	100 (8.0)

(*) The data in the table (except SF, NS32GX320 and NS32FX16) was taken from Microprocessor report, volume 3 number 10, October 1989.

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Floating-Point DSP Performance

	1024 FP FFT (msec)	FP FIR (nsec/tap)	COMPLEX-FP FIR (nsec/tap)
TMS320C30 @ 33 Mhz	3.0 (1.0)	60 (1.0)	240 (1.0)
DSP96002 @ 27 Mhz	1.55 (1.9)	75 (0.8)	300 (0.8)
ZR34324	1.7 (1.8)	23 (2.6)	93 (2.6)
SWORDFISH @ 25/50 Mhz	1.0 (3.0)	40 (1.5)	160 (1.5)

(*) The data in the table (except SF and ZR3425) was taken from Microprocessor report,volume 3 number 10, October 1989).

Summary

Swordfish features that will be seen in next generation microprocessors

- True superscalar.
- General purpose and DSP plus modules.
- Decoupling of system clock and CPU clock - half-frequency bus.
- Very wide system bus - 64 bits.
- System control functions: support for interleaved memory, page-mode DRAMs.
- On chip floating-point unit.
- Decoded instruction cache.