A Smart Frame Buffer

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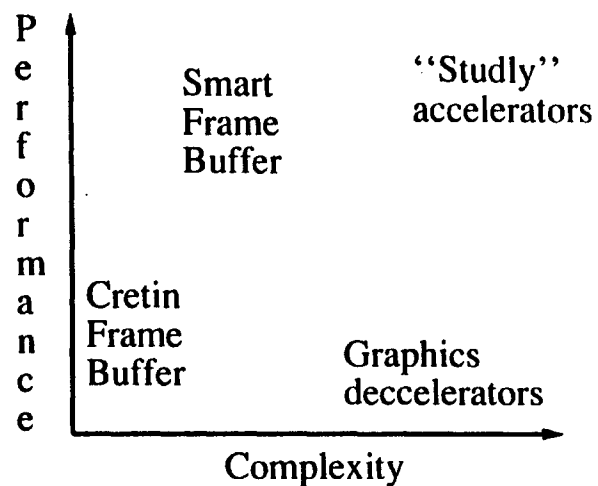

Why a Smart Frame Buffer?

DECStation 5000/200 dumb color frame buffer was quite successful, but...

- Byte writes will become read/modify/writes.

- TURBOchannel has 1/3 bandwidth of VRAM (33 vs. 100 megabytes/second).

- 2D performance of complex accelerators (can) exceed cfb.

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7.1

A 2D View of 2D Graphics

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Smart Frame Buffer

"Studly" accelerators

Cretin Frame Buffer

Graphics deccelerators

Complexity

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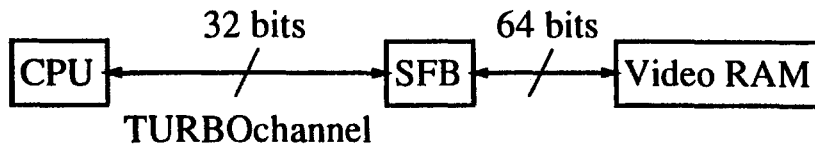A Smart Frame Buffer

Design Goals

Explicit goals:
- Time to market
- Cost
- Performance

How to get there:
- Simple: minimize development time.
- Cheap: use a small gate array with few pins.
- Make full memory bandwidth available.
- Use full-word writes, avoid reads.
- No operation takes longer than a bus timeout.

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Bus and Memory Interfaces

```
        32 bits           64 bits
CPU ◄────/────► SFB ◄────/────► Video RAM
      TURBOchannel
```

Sfb access to VRAM:

- 64 bit path to memory.
- 80 nsec. to read or write VRAM in page mode.
- 240 nsec. to read or write new page in VRAM.

CPU access to sfb:

- 120 nsec. to write (unless sfb stalls for time).
- Lots of nsec. to read.

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Frame Buffer Mode

Just like dumb cfb, but...

- Hardware planemask
- 16 Boolean functions

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Philosophy Behind Other Modes

Write 32 bits of data to sfb, which interprets the data according to the current mode:

- Each bit specifies what happens to one pixel.
- Destination address is an 8-byte-aligned pointer into screen memory.

Benefits:

- Reduce bus transactions by 8x to 16x, increase bandwidth by 4x to 8x.
- Allow small-scale parallelism.
- Use existing cfb code as template for sfb code.

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Transparent Stipple Mode

Transparent stipple expands 32 data bits to pixels:

- 0 means do nothing
- 1 means use the foreground pixel

0 0 0 1 1 0 1 1
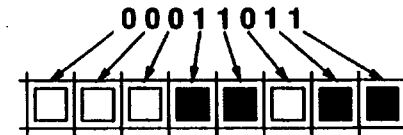
For solid fill, use a data word of all 1's.

Use 0 bits at left and right edges of span.

	Cfb	Sfb	GX	CRX
Solid 10x10 (kobj/sec)	88	145-213	150	278
Solid fill (Mbyte/sec)	22	90	98	110
Stipple 10x10 (kobj/sec)	34	96-155	150	136
Stipple fill (Mbyte/sec)	11	90	98	69
PolyText 6x13 (kchar/sec)	101	213-315	91	313
PolyText TR10 (kchar/sec)	107	174-267	111	391

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Opaque Stipple Mode

Opaque stipple expands 32 data bits to pixels:

- 0 means use the background pixel
- 1 means use the foreground pixel
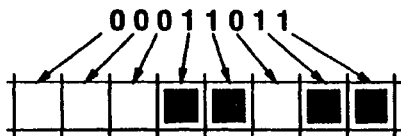
For left and right edges, write 32 bits to the pixel mask register, then write 32 data bits. Pixel mask resets to all 1's after use.

	Cfb	Sfb	GX	CRX
Stipple 10x10 (kobj/sec)	31	96-129	150	136
Stipple fill (Mbyte/sec)	21	85	98	69
ImageText 6x13 (kchar/sec)	114	225-335	78	257
ImageText TR10 (kchar/sec)	70	161-230	89	320

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Copy Mode

Uses pairs of 32-bit data words to copy up to 32 pixels:

- Read the pixels specified by first data word into the on-chip buffer.
- Shift by -8 to +7 pixels to align to destination.
- Write the pixels specified by the second data word back to the screen.

May also transfer data between main memory and screen memory by using direct TURBOchannel access to on-chip buffer.

	Cfb	Sfb	GX	CRX
Screen to screen (Mbyte/sec)	5	32	18	40
Main to screen (Mbyte/sec)	10	12	9	31
Screen to main (Mbyte/sec)	6	6	4	5
Main to main (Mbyte/sec)	11	11	11	25

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Line Mode

- Initialize with usual Bresenham parameters.

- Write 16 bits of data to paint 16 pixels.

- Transparent stipple for solid and dashed lines; opaque stipple for double-dashed lines.

- Needn't reload start address for connected lines.

00011011
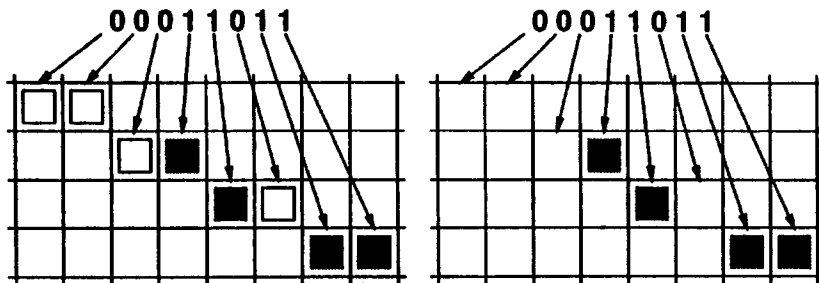
	Cfb	Sfb	GX	CRX
10-pixel segments (kline/sec)	134	248-460	157	648
10-pixel dash seg (kline/sec)	70	102-286	47	318
10-pixel polylines (kline/sec)	161	298-582	226	911

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Configurations

Pixel depths

- 8 bits/pixel: 256 entry colormap

- 16 bits/pixel: 4/4/4 RGB or 512-entry colormap, 3 overlay planes

- 32 bits/pixel: 8/8/8 RGB or 512-entry colormap, 3 overlay planes

Monitor configurations

- 1600x1280 @ 76, 72 Hz.

- 1280x1024 @ 76, 72, 66 Hz.

- 1024x864 @ 66, 60 Hz.

- 1024x768 @ 72, 66, 60 Hz.

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Conclusions

- Memory bandwidth is usually the limiting factor to 2-D graphics performance.

- A simple smart frame buffer increases bandwidth over a dumb frame buffer, and increases small-scale parallelism.

- Software does yucky control flow using cfb-based algorithms.

- Performance is comparable to much more complex accelerators.

- Sfb can be extended for cheap 3-D, imaging, and higher performance.

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