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THE MEGACELL DIFFERENTIATED FLOATING POINT PRODUCT FAMILY

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A G E N D A

- FLOATING POINT FAMILY STRATEGY
- METHODOLOGY
- BENEFITS
- MEGACELLS
- FIRST IMPLEMENTATION
- SUMMARY

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FLOATING POINT FAMILY STRATEGY

- IEEE 754 FLOATING POINT STANDARD
- DOUBLE PRECISION DATAPATHS
- PROPRIETARY LOW LATENCY ALGORITHMS
- SUPPORT INTEGER FORMATS
- SUPPORT LOGIC OPERATIONS
- FLEXIBILITY TO VARY CLOCK FREQUENCY, THROUGHPUT, AND LATENCY TO MEET SYSTEM NEEDS

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METHODOLOGY

- KEY DATAPATH AND MEMORY MEGACELLS ARE DESIGNED IN FULL CUSTOM
- "C" MODELS FOR EACH MEGACELL ARE AVAILABLE FOR SIMULATION
- CUSTOMER IS PROVIDED WITH PROCESS COMPATIBLE GATE ARRAY TECHNOLOGY
- SYSTEM SPECIFIC LOGIC IS DESIGNED BY CUSTOMER
- GATE ARRAY NETLIST IS ROUTED AT TI TO DESIRED ASPECT RATIO
- I/O'S, GATE ARRAY, AND DESIRED MEGACELLS ARE COMBINED IN A CUSTOM ENVIRONMENT

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BENEFITS

- MEGACELLS PROVIDE FULLY COMPACTED, HIGH PERFORMANCE DATAPATHS AND MEMORY UNITS
- GATE ARRAY PROVIDES EASE OF USE AND QUICK–TIME–TO–MARKET FOR CUSTOMER SPECIFIC LOGIC
- CUSTOMER'S RESOURCES ARE FOCUSED ON THEIR SYSTEM NEEDS
- TI'S DESIGN RESOURCES ARE FOCUSED ON THE MEMORY AND DATAPATH ELEMENTS AS WELL AS THE DEVICE TECHNOLOGY
- SUPPORTS SCALAR, PIPELINE AND SUPER PIPELINE ARCHITECTURES
- CONFIGURABILITY TO OPTIMIZE COPROCESSOR, PARALLEL PROCESSOR AND GRAPHIC ARCHITECTURAL SUPPORT
- HIGH PERFORMANCE LOW POWER 0.8 µM PROCESS

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MEGACELLS

- DOUBLE PRECISION ALU
- SINGLE PRECISION ALU
- DOUBLE PRECISION MULTIPLIER
- SINGLE PRECISION MULTIPLIER
- VARIOUS REGISTER FILES
- DATA CACHE
- INSTRUCTION CACHE

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ALU AND MULTIPLIER MEGACELLS

- COMPATIBLE WITH IEEE STANDARD 754 FOR
  - ADDITION
  - SUBTRACTION
  - MULTIPLICATION
  - DIVISION
  - SQUARE ROOT
- EACH MEGACELL IS TOTALLY INDEPENDENT WITH SEPARATE INSTRUCTION, DATA, AND STATUS BUSSES
- STATUS, CONTROL, AND DATA REGISTERS ARE PIPELINED IN PARALLEL
- MULTIPLIER CONTAINS A SEPARATE SEQUENCER
- GLOBAL COMMUNICATION WITH EACH OTHER DIRECTLY OR THROUGH REGISTER FILE
- DURING MULTICYCLE OPERATIONS THE SEQUENCERS WILL ASSERT SIGNALS THAT CAN BE USED TO STALL THE EXTERNAL INSTRUCTION STREAM
- ALL INTERNAL REGISTERS ARE SCANABLE
- DUAL MACHINE CAPABILITY OR NONDESTRUCTIVE SCAN CAPABILITY
- ALL INTERNAL REGISTERS CAN BE HALTED OR MADE TRANSPARENT

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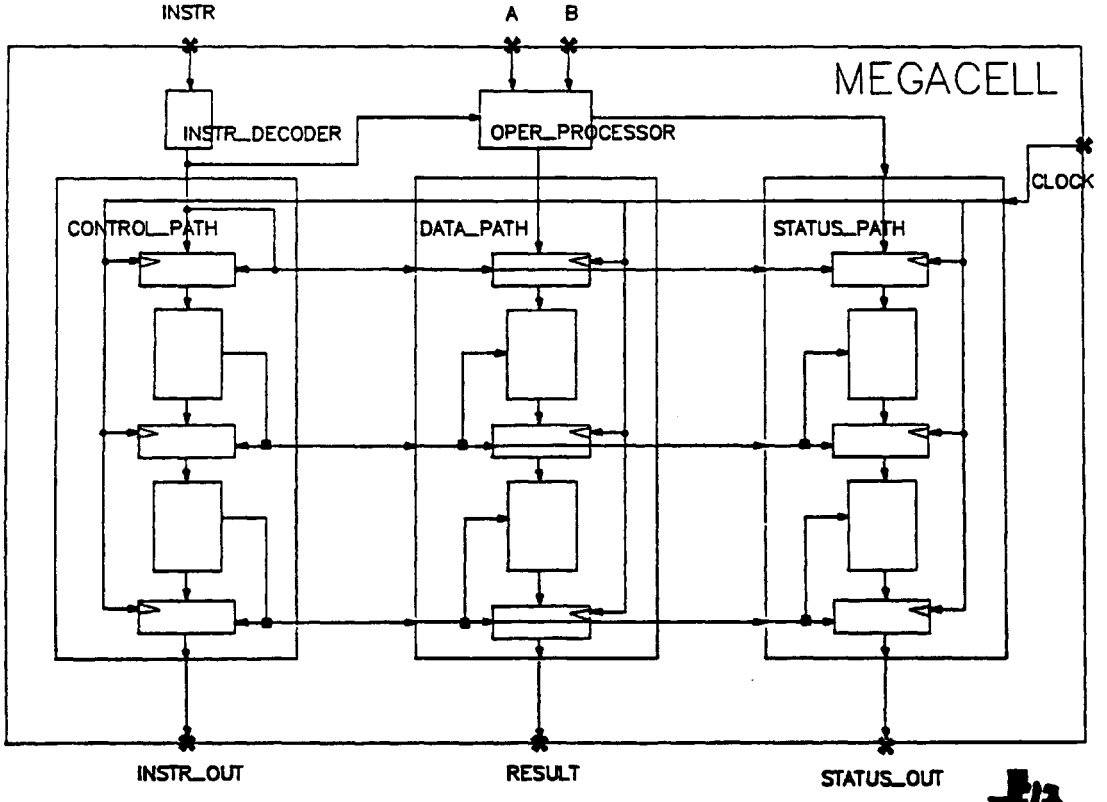

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MEGACELL FLOATING POINT NUMBER FORMATS

- NORMAL
- DENORMAL
- ZERO
- INFINITY
- SIGNALING NANs
- QUIET NANs
- 32–BIT SINGLE PRECISION
- 64–BIT DOUBLE PRECISION
- 80 AND 128–BIT EXTENDED PRECISION FOR PRIMITIVE OPERATIONS
- SIGNED INTEGERS
- UNSIGNED INTEGERS

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ALU MEGACELL

- 64–BIT MANTISSA PROCESSING
- 12–BIT EXPONENT PROCESSING
- ALL INSTRUCTIONS ARE SINGLE CYCLE EXCEPT INTEGER DIVISION
- OPERATIONS CAN BE SPECIFIED IN THE GENERAL FORM:
  { +, −, ||, −|| }A OP { +, −, ||, −|| }B
- DENORMAL NUMBERS ARE PROCESSED IN TWO WAYS:
  IEEE MODE – GRADUAL UNDERFLOW
  FAST MODE – CONVERT TO ZERO

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ALU MEGACELL INSTRUCTIONS

MNEMONIC	FUNCTION
ADD	FLOATING POINT AND INTEGER ADDITION
ADDO	FLOATING POINT AND INTEGER AND ZERO TO A OPERAND (CAN GENERATE ABS, NEG, –ABS)
ADDC	INTEGER AND WITH CARRY
AND	LOGICAL AND
SHIFTRA	ARITHMETIC SHIFT RIGHT BY N
CIC	CLEAR INTEGER CARRY
CLASS	NUMBER CLASS FUNCTION
CMP	COMPARE AND SET STATUS
CVTX_XXX_YYY	SINGLE CYCLE FORMAT CONVERSIONS
IDIV1	UNSIGNED INTEGER DIVIDE STEP 1 AND NORMALIZE INTEGER
IDIV2	UNSIGNED INTEGER DIVIDE STEP 2
IDIVI	UNSIGNED INTEGER DIVIDE ITERATE
IDIVT	UNSIGNED INTEGER DIVIDE TERMINATE
IREMT	UNSIGNED INTEGER REMAINDER TERMINATE
EXE	EXTRACT BIASED EXPONENT
EXM	EXRACT MANTISSA
LMRA	LOAD ALU MODE REGISTER
SHIFTRL	LOGICAL SHIFT RIGHT BY N
MERGEF	MERGE EXPONENT AND MANTISSA
NAND	LOGICAL NAND
NOPA	NO OPERATION INSTRUCTION
NOR	LOGIC NOR
OR	LOGICAL OR
PASSAQ	PASS WITH NO STATUS FLAGS, (CAN GENERATE FLOATING POINT ABS, NEG, –ABS)
PENC	PRIORITY ENCODE INTEGER
SIC	SET INTEGER CARRY
SHIFTL	SHIFT LEFT BY N
XNOR	LOGICAL XNOR
XOR	LOGICAL XOR

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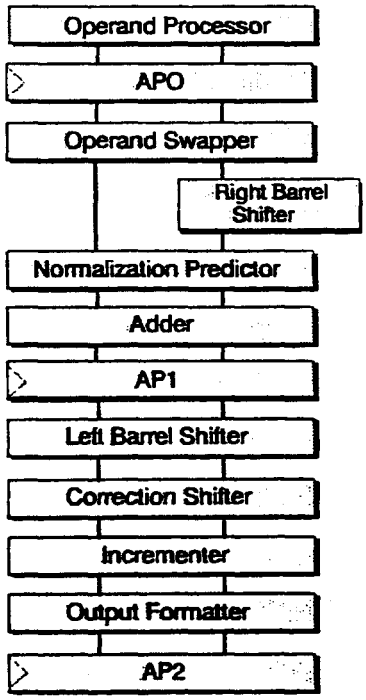
ALU DATAPATH



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MULTIPLIER MEGACELL

- OPERATIONS CAN BE SPECIFIED IN THE GENERAL FORM:
  { +, −, ||, −|| }A OP { +, −, ||, −|| }B
- DENORMAL NUMBERS ARE PROCESSED IN THREE WAYS:
  - IEEE MODE − GRADUAL UNDERFLOW
  - FAST MODE − CONVERT TO ZERO
  - WRAP MODE − MULTIPLIER ACCEPTS AND PRODUCES WRAPPED NUMBERS AS OPERANDS AND RESULTS
- HIGH SPEED SUM OF PRODUCTS OPERATIONS CAN BE ACHIEVED IN COMBINATION WITH THE ALU

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MULTIPLIER MEGACELL INSTRUCTIONS

MNEMONIC	FUNCTION
NOPM	NO OPERATION INSTRUCTION
PASSMQ	PASS A, NO STATUS UPDATE
MULT	MULTIPLY (MICROCODED EXCEPTIONS)
MULT1	MULTIPLY BY ONE (MICROCODED EXCEPTIONS)
DIV	FLOATING POINT DIVIDE (MICROCODED)
INV	FLOATING POINT RECIPROCAL OF B (MICROCODED EXCEPTIONS)
SQRT	FLOATING POINT SQUARE ROOT (MICROCODED)
AINVSQRTB	1 / SQRT(B)
LMRM	LOAD MULTIPLIER MODE REGISTER

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MULTIPLIER MEGACELL THROUGHPUT

INSTRUCTION	THROUGHPUT IN CLOCK CYCLES
32X32 INTEGER MULTIPLY	1
64X64 INTEGER MULTIPLY	
UPPER HALF OR LOWER HALF	1
128–BIT RESULT	2
IEEE FLOATING POINT MULTIPLY	1
IEEE FLOATING POINT DIVIDE	
SINGLE	4
DOUBLE	5
IEEE FLOATING POINT SQRT	
SINGLE	6
DOUBLE	7
FLOATING POINT 1/SQRT	
SINGLE	5
DOUBLE	6

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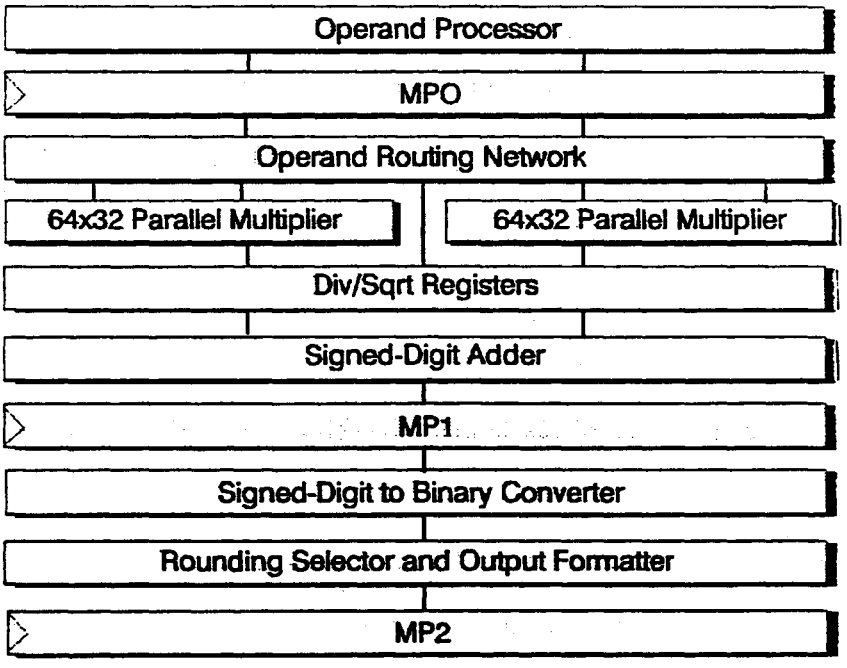
MPY DATAPATH



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REGISTER FILE MEGACELL

- 32–DEEP BY 64–BIT WIDE
- LONG–WORD ADDRESSABLE
- STORE 64 SINGLE PRECISION OPERANDS OR
  32 DOUBLE PRECISION OPERANDS
- 2 READ PORTS AND 1 WRITE PORT DEDICATED TO THE ALU
- 2 READ PORTS AND 1 WRITE PORT DEDICATED TO THE MULTIPLIER
- 1 READ PORT AND 1 WRITE PORT DEDICATED TO THE I/O
- SPECIAL FEEDTHROUGH PATHS
- ARITHMETIC PROCESSING CAN OCCUR AT THE SAME TIME AS I/O TRANSFERS
- ALL PORTS CAN BE USED IN ANY CLOCK CYCLE AND AT ANY RATE

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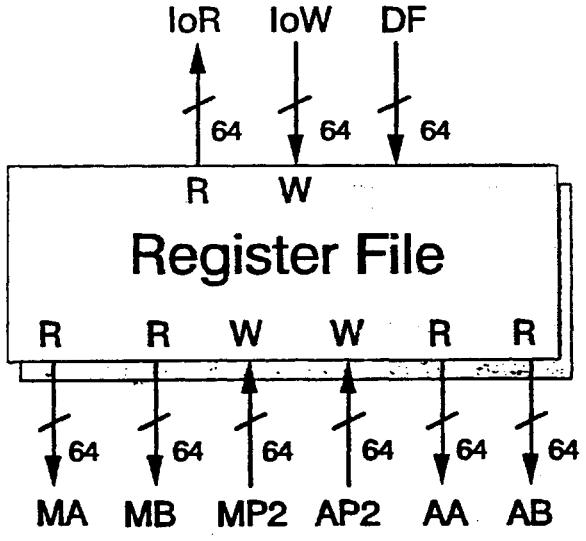
REGISTER FILE ARCHITECTURE



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GATE ARRAY

- NETLIST IS DESIGNED USING THE CUSTOMER'S EXPERTISE
- DESIGNED IN A GATE ARRAY ENVIRONMENT
- LIBRARY CONTAINS OVER 200 CELLS
- PROPAGATION DELAYS ARE TYPICALLY 0.5NS PER GATE
- FULL STATIC CMOS GATES
- LOW POWER CONSUMPTION
- DESIGNS OF 30K GATES ARE POSSIBLE
- VARIABLE ASPECT RATIO AND SHAPE

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0.8 um DLM CMOS PROCESS

METAL 1 PITCH:	2.0 um (NO CONTACTS) 2.6 um (WITH CONTACTS)
METAL 2 PITCH:	2.0 um (NO VIAS) 2.6 um (WITH VIAS)
DRAWN POLY WIDTH:	0.8 um
POLY SPACE:	1.0 um (OVER FIELD) 1.5 um (OVER DIFFUSION)
CONTACT SIZE:	0.8 X 0.8 um**2
VIA SIZE:	0.8 X 0.8 um**2

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0.8 um DLM CMOS ELECTRICAL PARAMETERS

Leff, p = 0.7 um Leff, n = 0.6 um

SILICIDED POLY RESISTANCE: 2.0 ohms / sq

SILICIDED DIFFUSION RESISTANCE: 2.0 ohms / sq

REFERENCE:

CHAPMAN, RICHARD A., "AN 0.8 UM CMOS TECHNOLOGY FOR HIGH PERFORMANCE LOGIC APPLICATIONS", IEDM 1987.

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FIRST IMPLEMENTATION

- COPROCESSOR FOR A PA–RISC PROCESSOR USED IN HP'S SERIES 700 WORKSTATION FAMILY
- MEGACELL'S FLEXIBILITY MEET CUSTOMER'S REQUIREMENTS
  - FREQUENCY
  - ARCHITECTURE
  - LATENCY (3 CYCLE)
  - THROUGHPUT (2 CYCLE)
- ADDITIONAL INSTRUCTIONS WERE ADDED TO MAXIMIZE PERFORMANCE
  - 3–REGISTER MULTIPLY
  - INDEPENDENT 2 REGISTER ADD OR SUBTRACT
  - ACCELERATED CLIP TEST
  - RECIPROCAL SQUARE ROOT
  - INTEGER MULTIPLY

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FIRST IMPLEMENTATION RESULTS:

DIE SIZE: 502 X 518 MILS

TRANSISTOR COUNT: 640K

PACKAGE: 207 PIN CERAMIC PGA

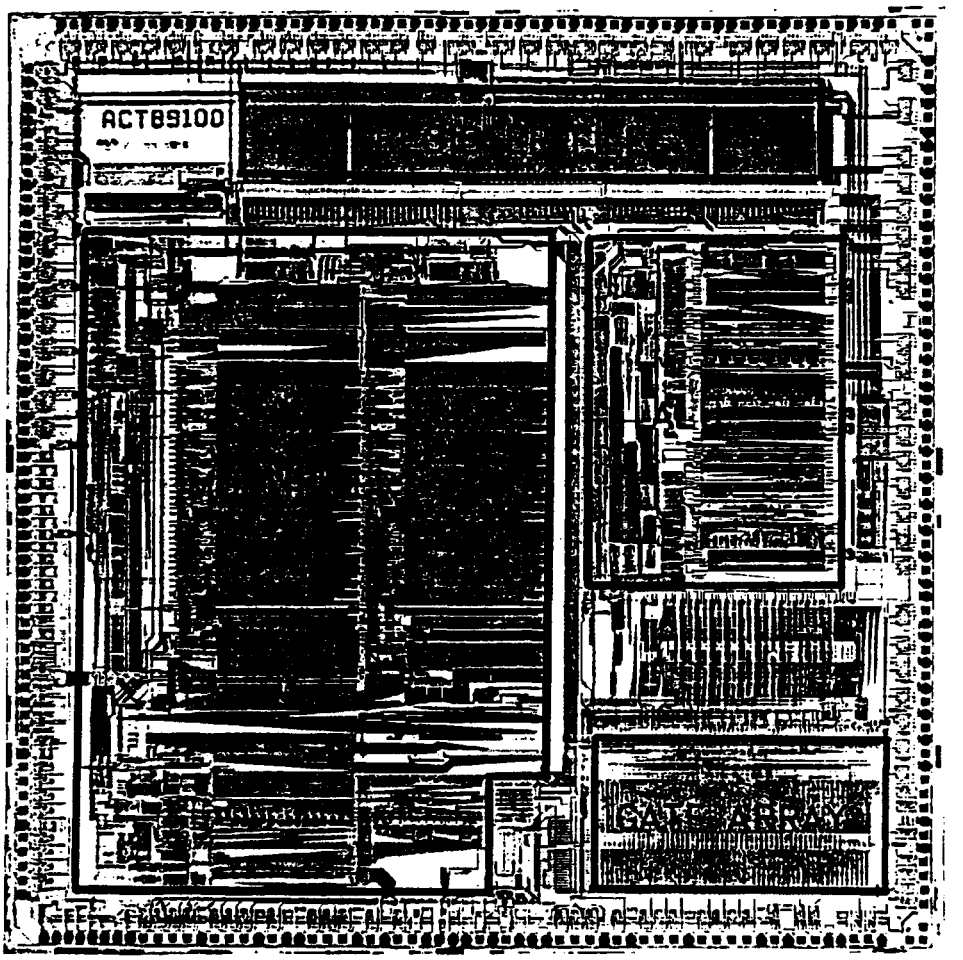
POWER: 5.0 WATTS AT 66 MHZ

SPEED: 66 MHZ, WORST CASE CONDITIONS

LINPACK BENCHMARK (100 X 100)
SINGLE PRECISION: 33.2 MFLOPS
DOUBLE PRECISION: 23.0 MFLOPS

Architecture		PA-RISC	PA-RISC	RS/6000	SPARC	MIPS	88000	68040	486	i860
Clock Rate (MHz)		50	66	30	40	33	33	25	33	40
Integer	gcc	35.2	46.5	21.0	19.6	25.9	18.3	13.8	18.8	15.1
	espresso	42.5	55.2	24.9	19.0	26.3	23.0	13.4	17.1	22.3
	li	38.1	50.3	23.7	23.2	32.1	23.9	15.5	23.3	21.7
	eqntott	40.6	52.6	26.7	21.5	24.7	20.7	9.8	14.8	18.9
Floating-Point	spice2g6	46.9	60.9	33.2	16.8	21.0	14.8	13.1	12.0	18.1
	doduc	48.6	64.0	33.1	18.4	27.1	12.2	8.1	7.7	18.8
	nasa7	58.0	73.7	43.4	27.4	29.6	17.5	12.1	7.8	57.6
	matrix300	210.0	273.3	26.5	28.1	21.7	21.5	11.5	12.8	28.1
	fpppp	81.4	107.0	65.8	23.7	33.8	15.3	13.4	10.2	25.7
	tomcatv	52.9	67.4	91.0	17.8	25.8	14.9	9.1	6.3	43.8
Geometric Means	SPECmark	55.5	72.2	34.7	21.2	26.5	17.8	11.8	12.1	24.7
	Integer-Only	39.0	51.0	24.0	20.8	27.1	21.4	12.9	18.2	19.3
	FP-Only	70.2	91.0	44.3	21.6	26.1	15.8	11.0	9.2	29.2

Table 1. SPEC benchmark results. These represent the highest clock rates currently available in systems, except for IBM's 41.6-MHz RS/6000 Model 550 which was excluded because it is not in the same price class. Note PA results are for June '91 compiler release. The systems are the HP 9000 Model 720; HP 9000 Model 730; IBM RS/6000 Model 540; Sun SPARCstation 2; MIPS RC3360; Motorola Delta Series Model 8612; HP 425s; and Alacron AL860. All machines except i860 have external cache.



TEXAS INSTRUMENTS 0390-77

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SUMMARY

- QUICK TIME–TO–MARKET
- HIGH PERFORMANCE
- FLEXIBLE ARCHITECTURE
- MEGACELL SOLUTION WORKS AT 66 MHZ IN UNIX SYSTEM
- FUNCTIONAL ON FIRST SILICON