

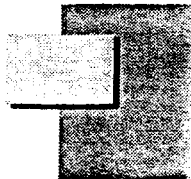
**ECHELON**  
Corporation



IEEE Hot Chips Symposium, August 26-27, 1991

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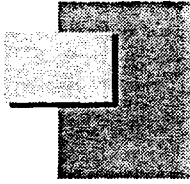
## Agenda

- **Distributed control systems**
- **Overview of NEURON<sup>®</sup> CHIP<sup>™</sup> features**
- **Implementation techniques to reduce chip cost**
- **Role of NEURON CHIPS in systems**

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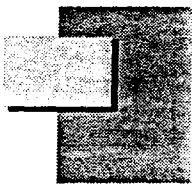
## Trends toward increasingly distributed computing

- **Traditional data processing**
  - Mainframe to department mini to personal computer
  - Benefits of dedicated compute cycles
  - Better price/performance
  - Defacto standards to share information
- **Control systems have similar needs, but lag behind...**
  - Compute cost is often prohibitive when amortized over only one or two sensor/actuators
  - "Pioneers" have taken next step, but with specialized, non-extensible solutions – complex development

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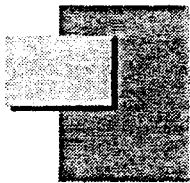
## The building block for highly distributed control systems

- **Designed to address cost of intelligent distributed control:**
  - Base model targeted for \$2 - \$3 by the mid 1990's
  - Medium independent communications interface to facilitate wire replacement, control system retrofit
  - High current drive pads to reduce external components
  - Configurable I/O block provides over 25 control functions internal to the chip
- **Designed to address implementation difficulty of highly distributed control**
  - Firmware for full communications protocol
  - Firmware for real time scheduler
  - Scalable from simple, single point nodes to high end controllers
  - Features for network installation and error detection

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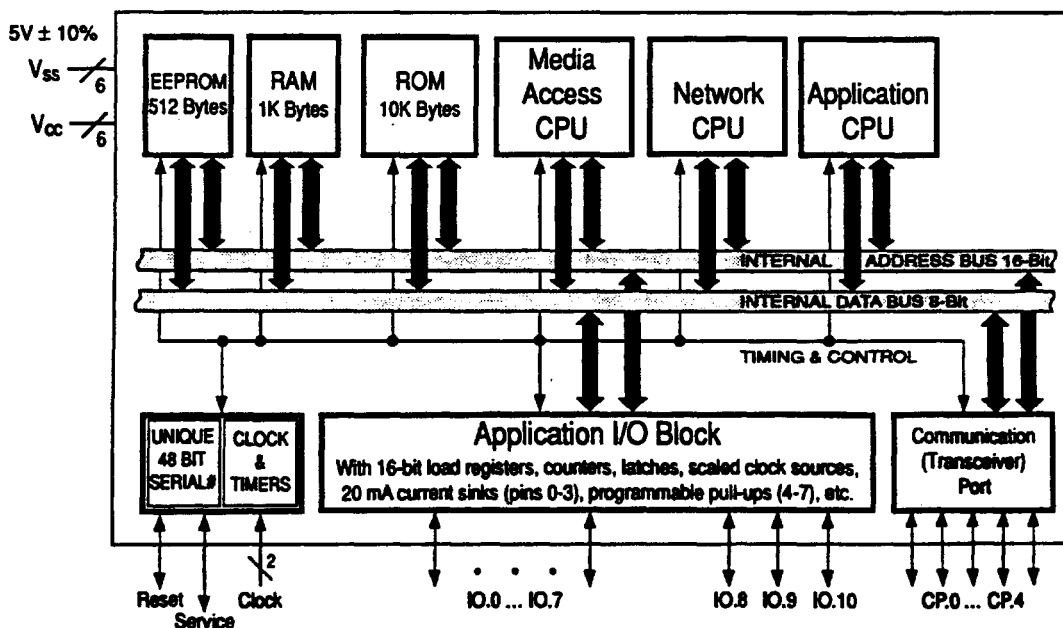
# NEURON CHIP Features

- 3 independent, symmetric CPU's
- Communication rates 1.25 MBPS down to 4800 BPS
- Large on-chip RAM
- Configurable Comm port for multiple transceivers
- High current pads for comm and applications I/O
- Unique 48 bit ID for each chip / Service pin
- Multiple clock rates and sleep mode for power management
- Can send up to 350 packets/sec
- Can transfer over 190 KBPS of application data per second
- Dual 16 bit timer counters with overflow
  - Pulse width modulation, period measurement, quadrature input, triac control, frequency measurement, totalizing, etc.

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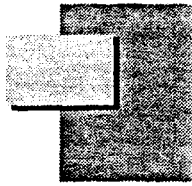


# NEURON 3120™ CHIP

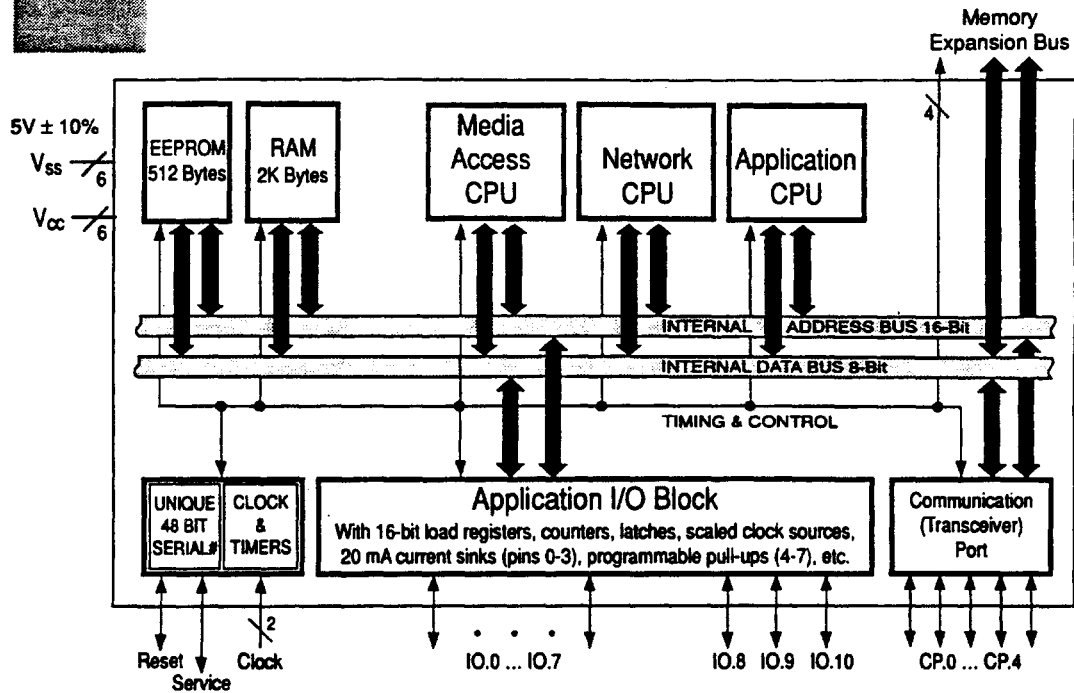


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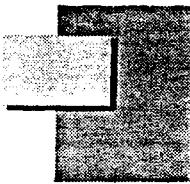




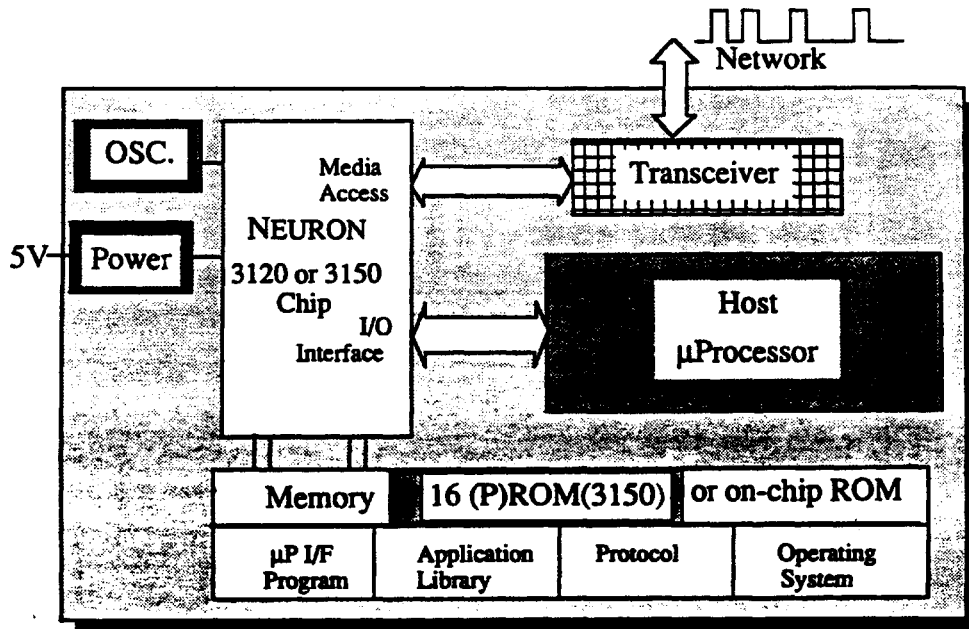
# NEURON 3150™ CHIP



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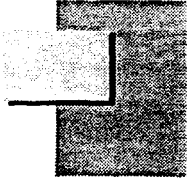


# NEURON 3120/ 3150 CHIP with attached microprocessor



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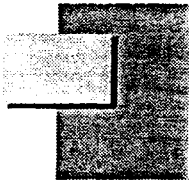
## Scaling the LONWORKS™ Architecture

- **Basic applications:**
  - Single Chip for small applications
- **Larger applications:**
  - Single Chip plus external memory for more demanding applications
- **Computation and/or memory intensive applications:**
  - Single Chip plus any microprocessor for the most demanding applications

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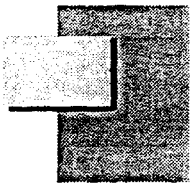
## Pipelined multiprocessors

- **Stack based instruction set**
  - smaller programs
  - small register set to replicate for additional processor
- **Each  $\mu$ cycle has one of the processors using one of the following:**
  - PLA
  - ALU
  - Memory
- **Special "Fast I/O" instruction to enable fast data transfer**

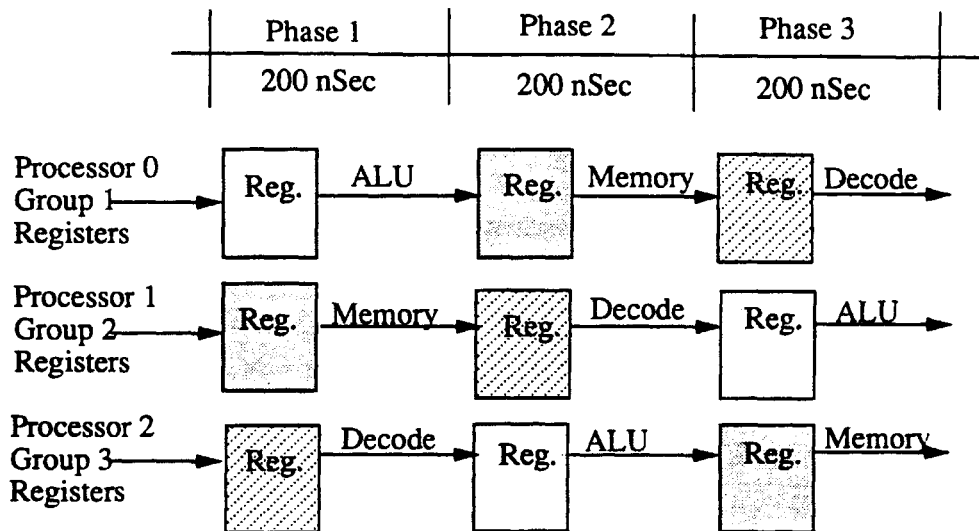
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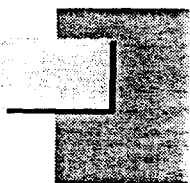
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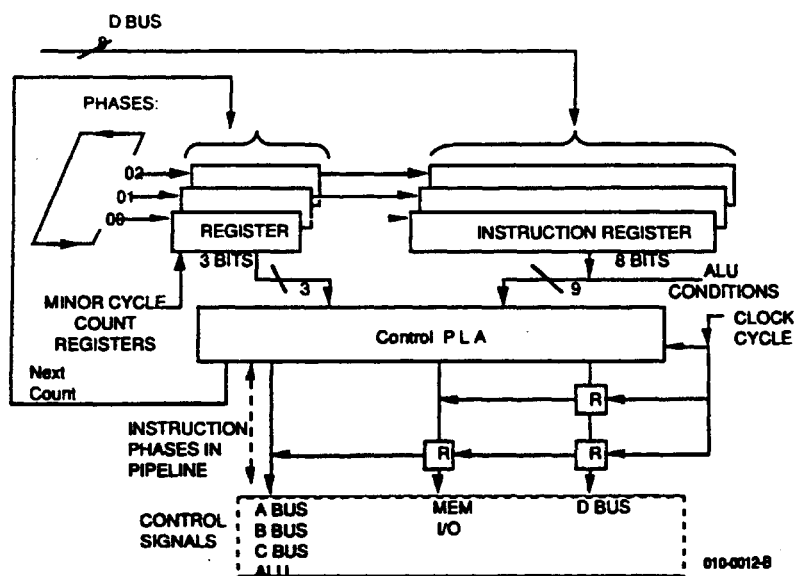
# Pipelining in NEURON CHIPS

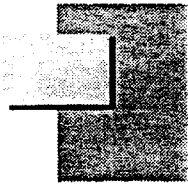


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# Processor Timing Control



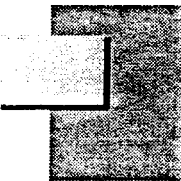


## Comm Port -- 5 pin interface

- **Direct, Differential Drive**
  - 40 mA drivers
  - Differential Manchester encoded data
  - 8 programmable hysteresis settings
  - 4 programmable post hysteresis filtering settings
- **Direct, Single Ended Drive**
  - Differential Manchester encoded data
  - Data in, data out, transmit enable, collision detect
  - Bidirectional sleep
- **Special purpose mode**
  - Up to 7 bytes transceiver configuration data written
  - Up to 7 bytes transceiver status read
  - Continuous status & data frames between NEURON CHIP and associated transceiver
  - Transceiver controls preamble, encoding, comm data rate

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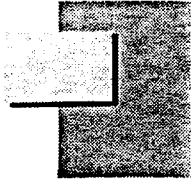
## Applications I/O

- All 11 pins have TTL level inputs with hysteresis
- 4 have configurable pullups, 4 have 20 mA current sinks
- Simple inputs, serial I/O, or parallel I/O
- Fast I/O for 2.5 MBPS parallel data transfer
- Dual 16 bit timer/counters
  - Timer/counter clock sources scaled with input frequency for constant values

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# Role of NEURON CHIPS in Systems

- **Heating, ventilation, air conditioning**
  - Sensing temperature controlling dampers, chillers, etc.
- **Commercial lighting**
  - Timed on/off, dimming, occupancy sensing, security
- **Medical Monitoring**
  - ICU networks, mobile patient monitoring
- **Factory Automation**
  - Preprocessing sensor data, self calibration
- **Identification / Asset management**
  - 48 bit ID, asset history in EEPROM, asset tracking
- **Office Equipment**
  - printer, copier control
- **Automated utility meter reading, load shedding**
  - billing data, remote shutdown of loads
- **And others...**

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