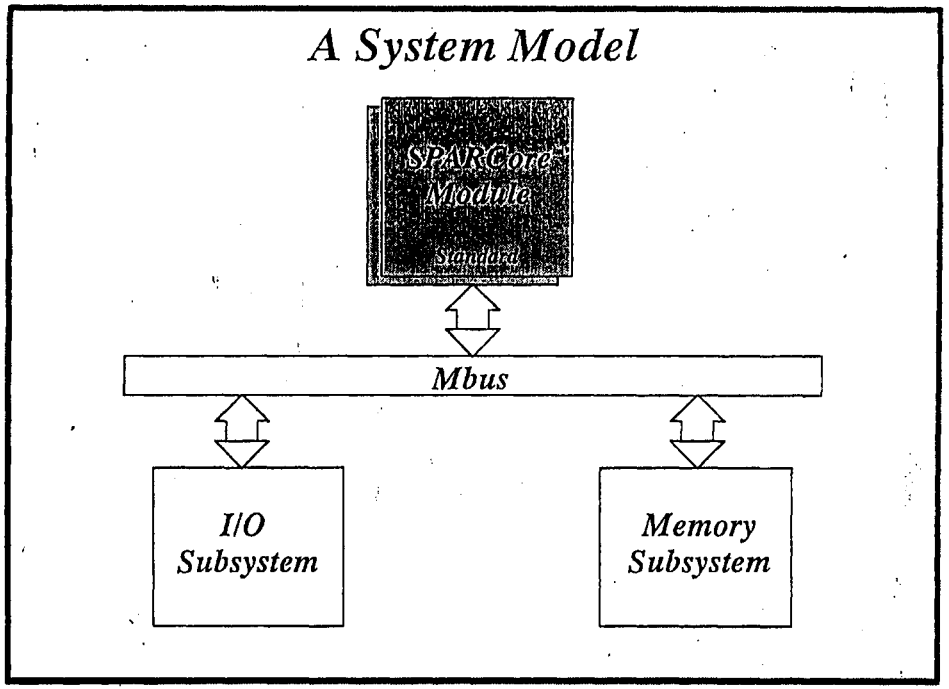
SPARCore™ Modules

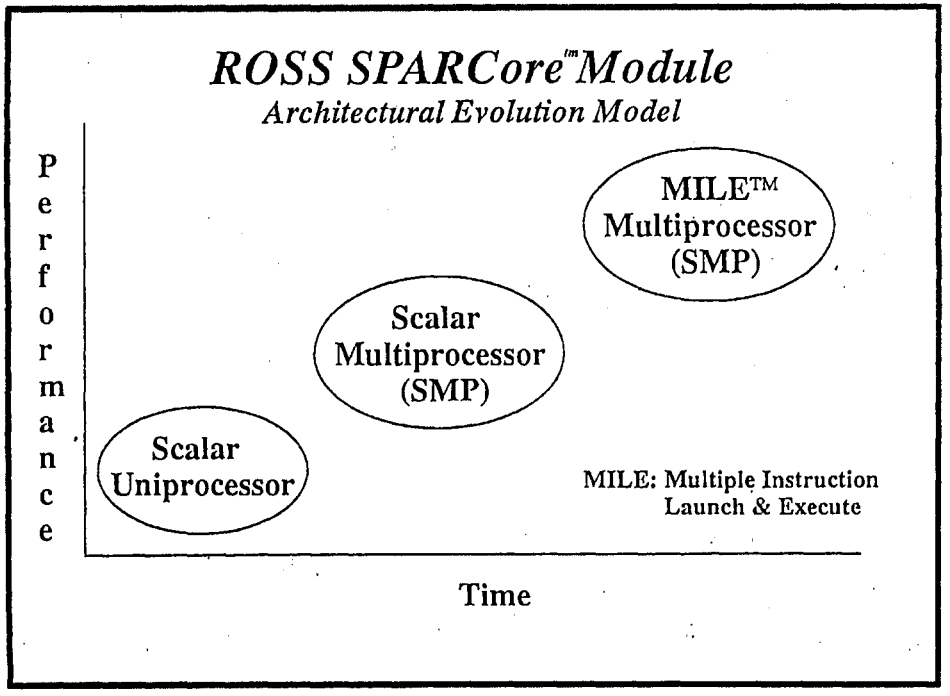
Raju Vegesna
Chief Architect

Hot Chips III
Stanford University
August 26, 1991

SPARCore™ Modules
Agenda

- Global Concepts
  - Philosophy
  - Features
- SPARCore Modules
  - Single CPU CYM6001K
  - Dual CPU CYM6002K
  - Next generation module


A System Model
SPARCore Module
Standard
Mbus
I/O Subsystem
Memory Subsystem


ROSS SPARCore™ Module
Architectural Evolution Model
Performance
MILE™ Multiprocessor (SMP)
Scalar Multiprocessor (SMP)
Scalar Uniprocessor
MILE: Multiple Instruction Launch & Execute
Time

SPARCore™ Module

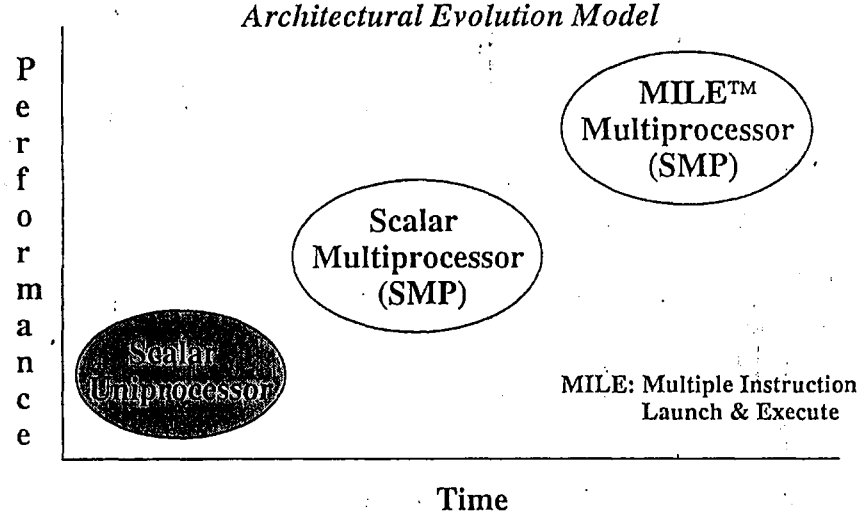
Dual CPU channels

Each CPU channel supports ...

- SPARC integer functions
- SPARC floating point functions
- SPARC reference MMU
- Performance driven Cache system
- SPARC Mbus interface

ROSS SPARCore™ Module

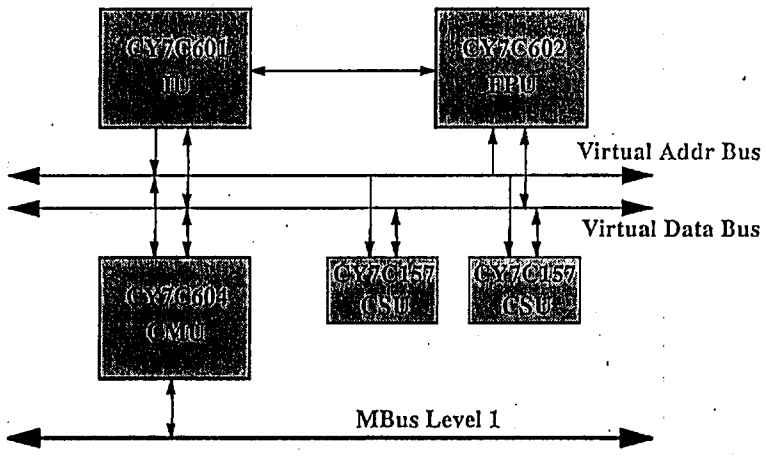
Architectural Evolution Model



4.24

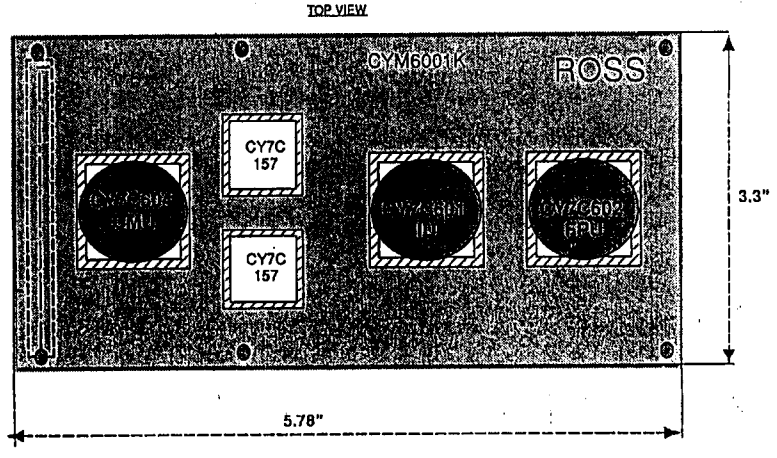
CYM6001K Module

Single CPU



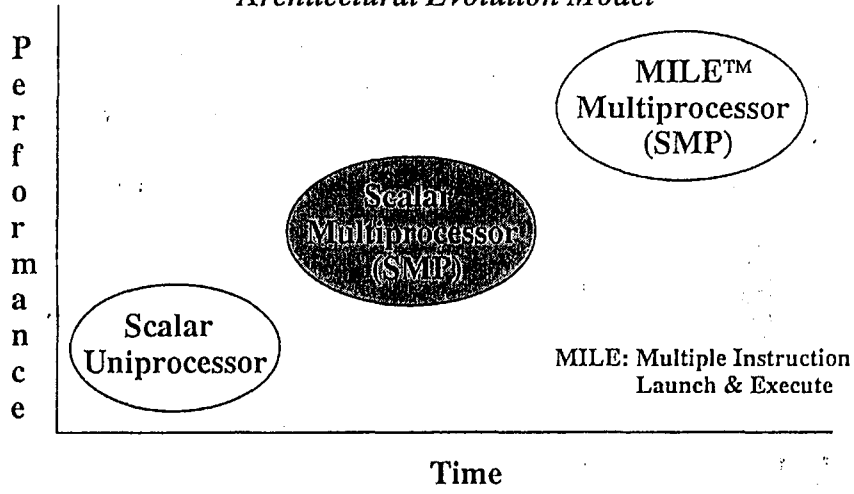
CYM6001K Module

Module Design



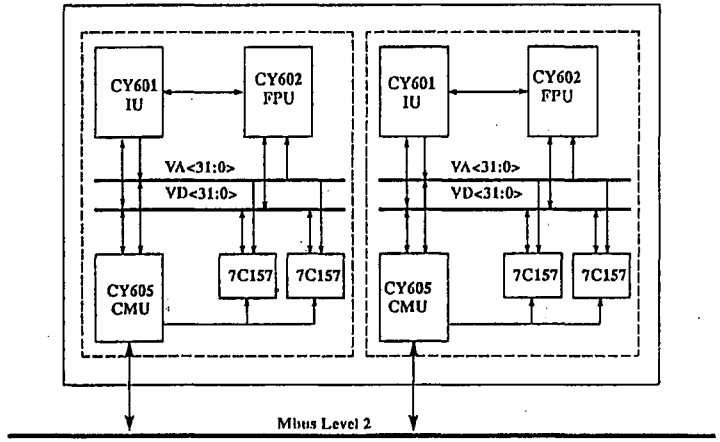
ROSS SPARCore™ Module

Architectural Evolution Model



CYM6002K Module

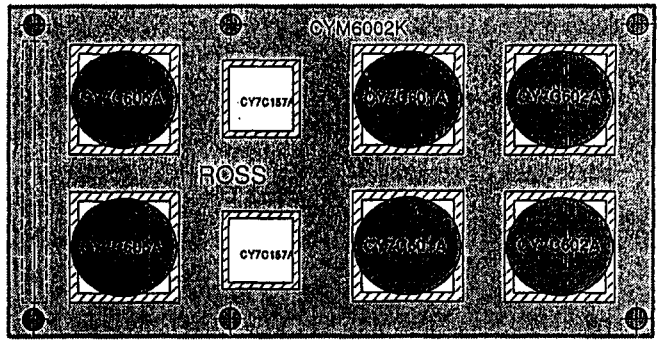
Dual CPU



4.25

CYM6002K Module

Module design



SPARCore™ Module

Module design

- Conforms to SBus card form factor (3.3" X 5.78")
- All components surface mounted
- SPARC – standard Mbus module connector
  - High reliability
  - Excellent electrical performance

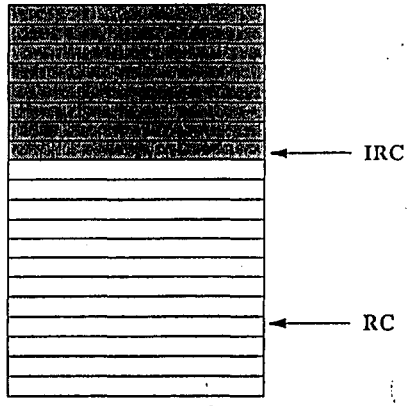
SPARC Reference MMU

- Demand page memory management
- 32-bit virtual to 36-bit physical address
- Support for 4096 contexts
- Linear address mapping

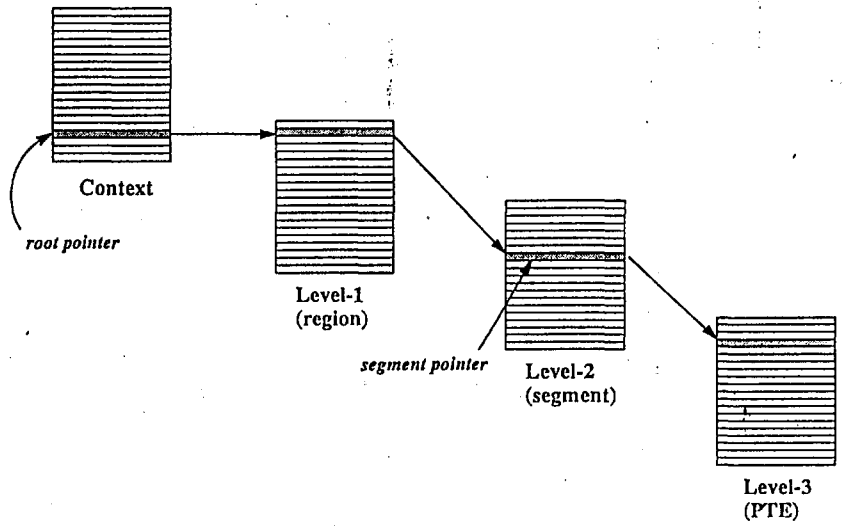
SPARC Reference MMU

- Fully associative 64 entry address translation cache (ATC)
- Hardware table walk
- Invalidation support for multiple ATC entries

ATC Entry Locking



PTP Caching



Cache Sub-system

Uni-processing

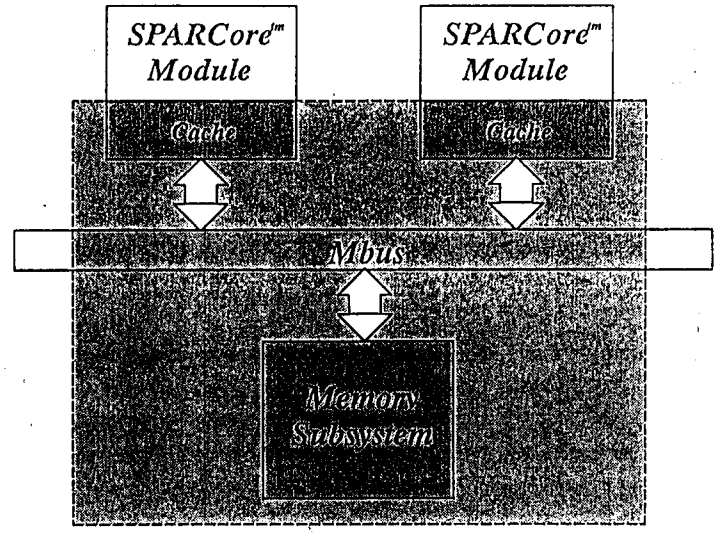
- 64-Kbytes of zero wait-state, direct-mapped virtual cache
- Write-back with write-allocate
- Write-through with no write-allocate
- Separate 32-byte read and 32-byte write buffers
- Parallel operation of read and write buffers

Cache Sub-system

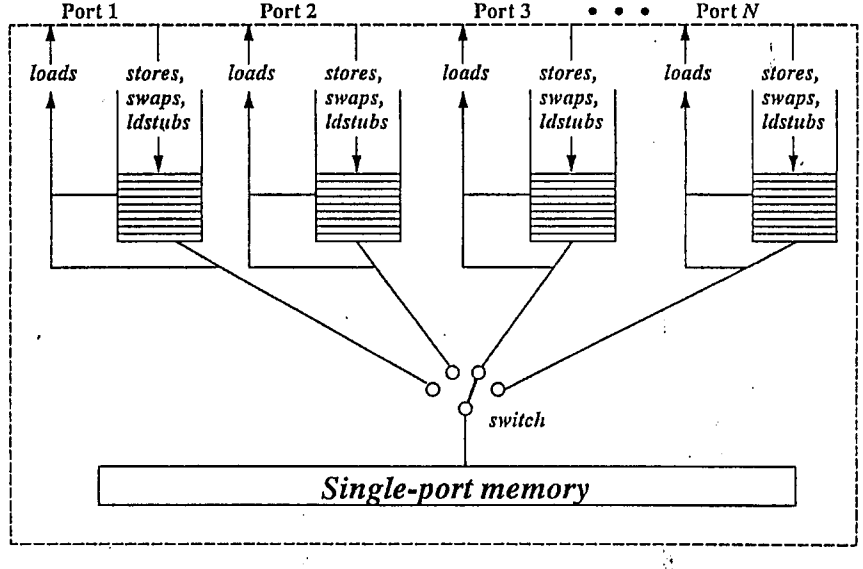
Multi-processing

- 64-Kbytes of zero wait-state, direct-mapped virtual cache
- Fully concurrent bus snooping
- Two independent cache tags:
  - Processor side
  - Mbus side

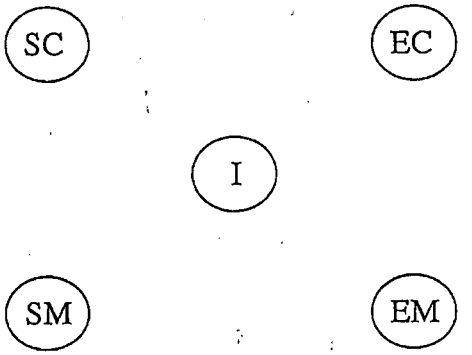
Shared Memory Image



Total Store Ordering

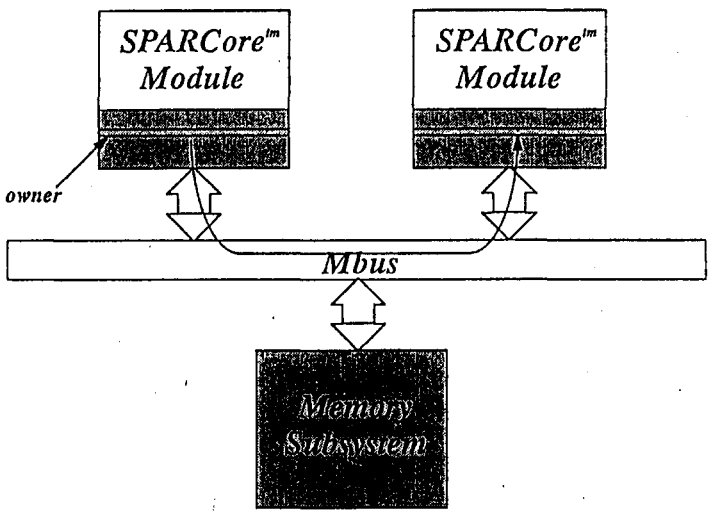


Cache-Line States



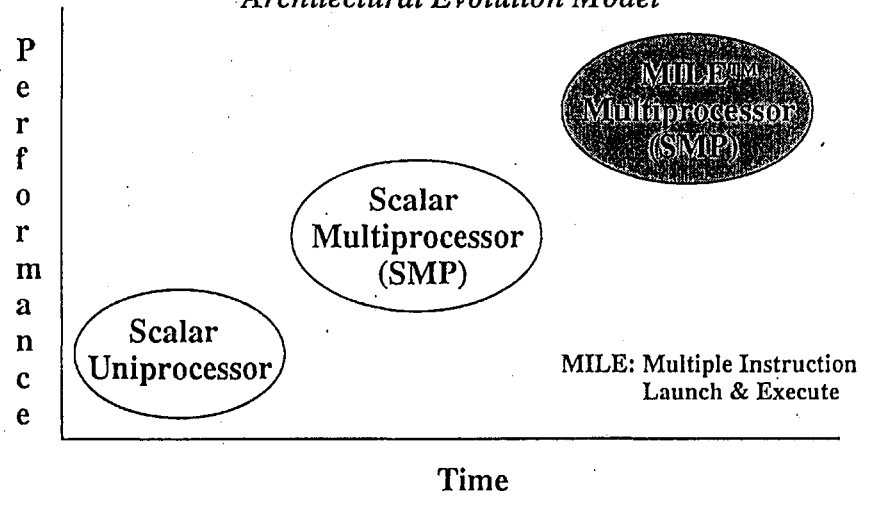
SC – shared clean
EC – exclusive clean
SM – shared modified
EM – exclusive modified
I – invalid

Direct Data Intervention and Reflective Memory



ROSS SPARCore™ Module

Architectural Evolution Model



Next Generation Module

- Architectural advancements (MILE™)
  - Superscalar
  - Superpipelining
  - Symmetric multiprocessor
- Semiconductor process advancements
  - Submicron
- Packaging technology innovations
  - Multi–Die