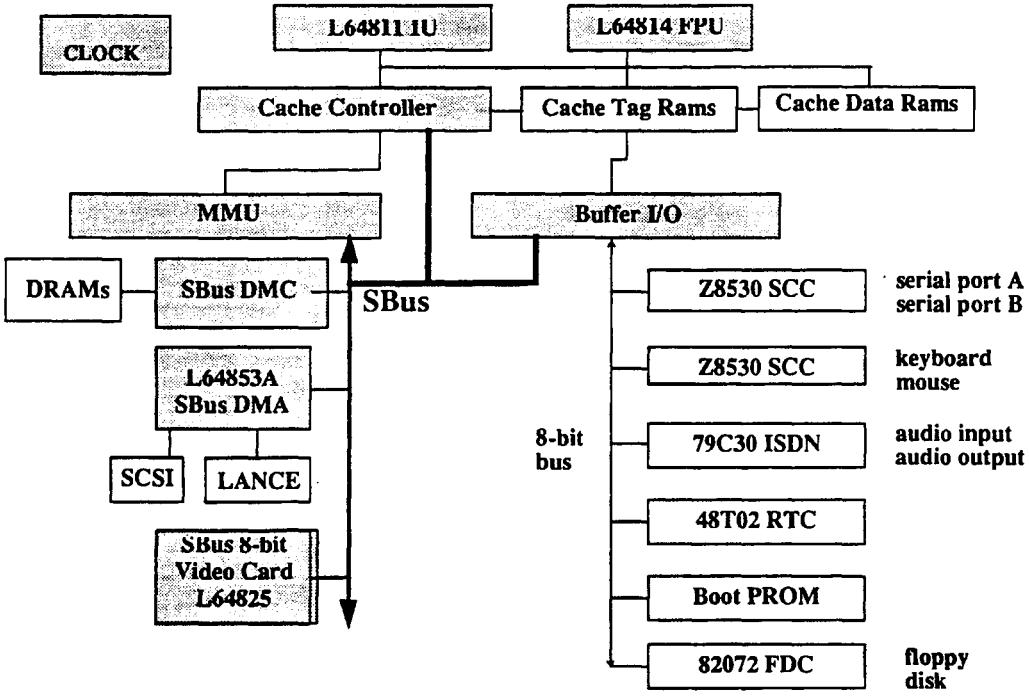
The SparKIT™ Chipset

- Background
- SBus and Mbus
- The SparKIT Chipset
- System Integration

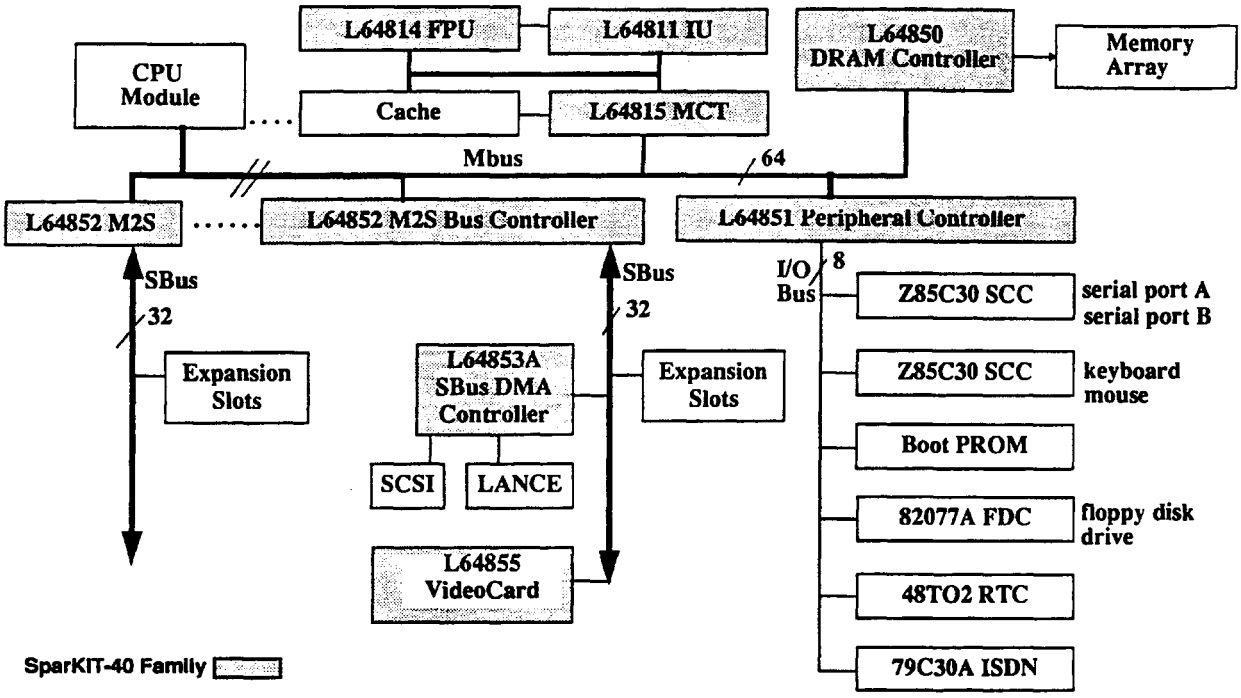
SPARCstation Architecture



SBus Features

- Synchronous I/O Bus
- Up to 25 MHz bus clock frequency
- 32-bit Data bus
- 32-bit Virtual Address for SBus masters
- Geographical device selection
- Supports Burst transfers up to 64 bytes
- Error and Rerun protocols
- Supports up to 8 masters

The SparKIT™ Architecture



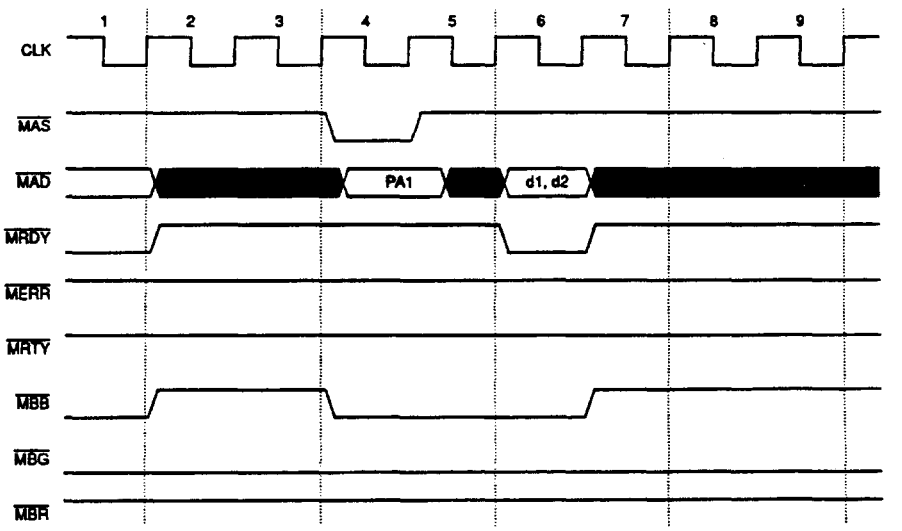
The SparKIT™ Advantage

- Modularity: Plug different CPU Modules with different speeds and Implementations
- Standards: 3rd party SBus Cards and Mbus Modules
- Simplicity of Interface: Mbus and SBus synchronous interfaces provide a simple high speed interface to other busses (i.e. Futurebus+, VME)
- HighIntegration: Reduction in overall system cost

Mbus Features

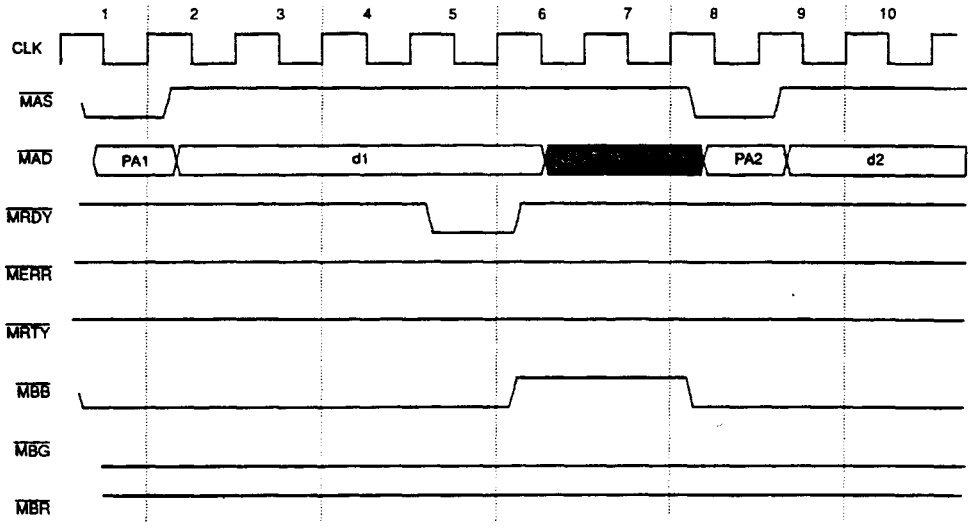
- Synchronous Multiprocessor/Memory Bus
- High speed, up to 40 MHz bus clock frequency
- 64-bit data bus
- Multiplexed Address & control/Data bus
- 36-bit Physical Address (up to 64 Gigabytes)
- Supports Burst transfers up to 128 bytes
- Supports Multiple Masters
- Error and Rerun protocols

Mbus Transactions: Read



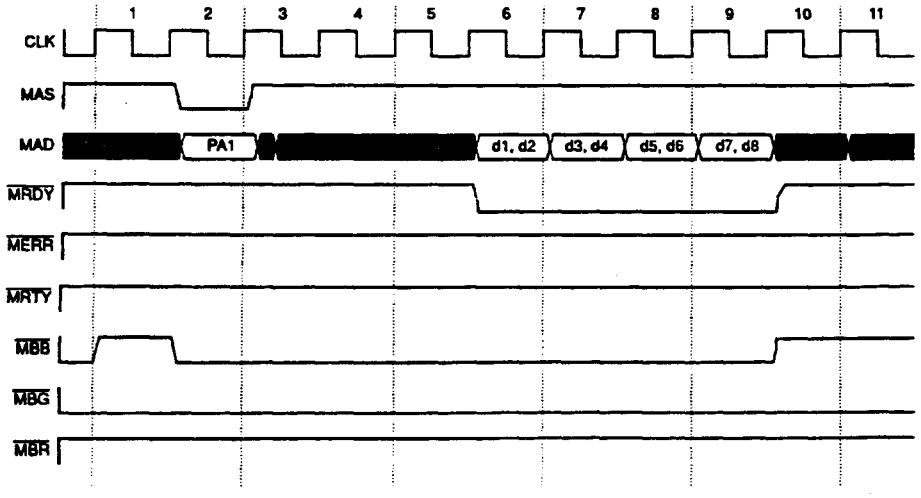
Word Read
(Mbus Request and Grant, not shown)

Mbus Transactions: Write



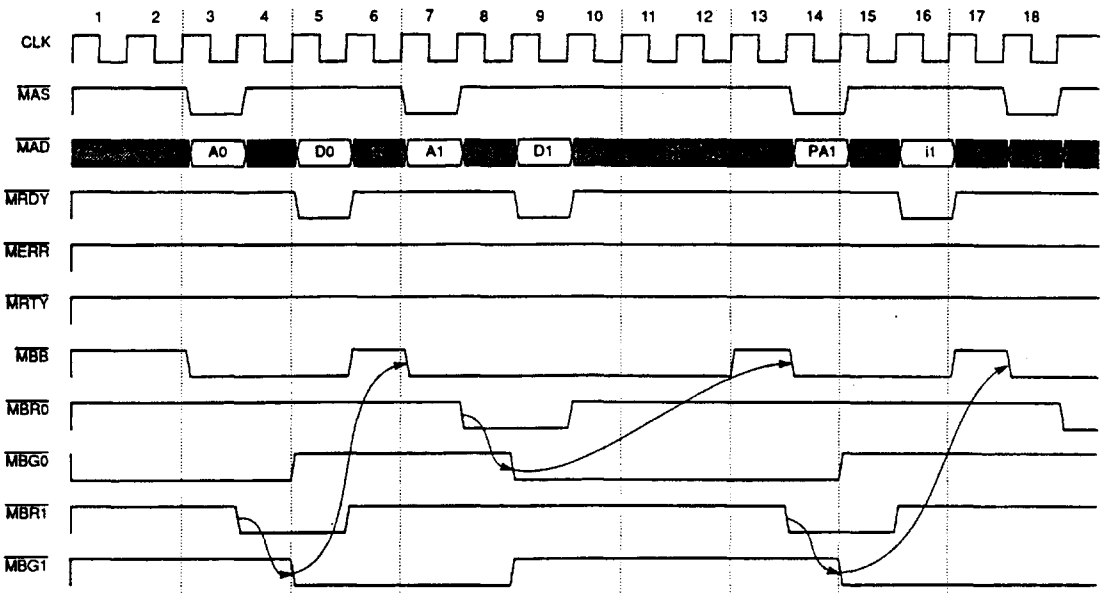
Word Write
(Mbus Request and Grant, not shown)

Mbus Transactions: Burst Read



Burst Read
(Mbus Request and Grant, not shown)

Mbus Transactions: Bus Arbitration



Dev 0 has the bus, it asserts /MBB. The Mbus controller has asserted /MBG0

Dev 1 requests the bus, when Dev 0 de-asserts /MBB, the Mbus controller grants the bus to Dev 1 by asserting /MBG1 and de-asserting /MBG0

SparKIT

- CPU core chips
  - **L64811 Integer Unit (IU)**
  - **L64814 Floating Point Unit (FPU)**
  - **L64815 MMU, Cache Control, Cache Tags (MCT)**
- Peripheral chips
  - **L64850 DRAM Memory Controller (DMC)**
  - **L64851 Peripheral Controller (STDIO)**
  - **L64852 Mbus to SBus Controller and IO MMU (M2S)**
  - **L64853ASBus DMA Controller**

L64811 Integer Unit

- 136 general purpose registers
- 8 overlapping register windows
- 2 coprocessor interfaces
  - **Floating point unit**
  - **User definable coprocessor**
- Operating frequency: 25, 33, 40 MHz
- Performance: 18-29 MIPS

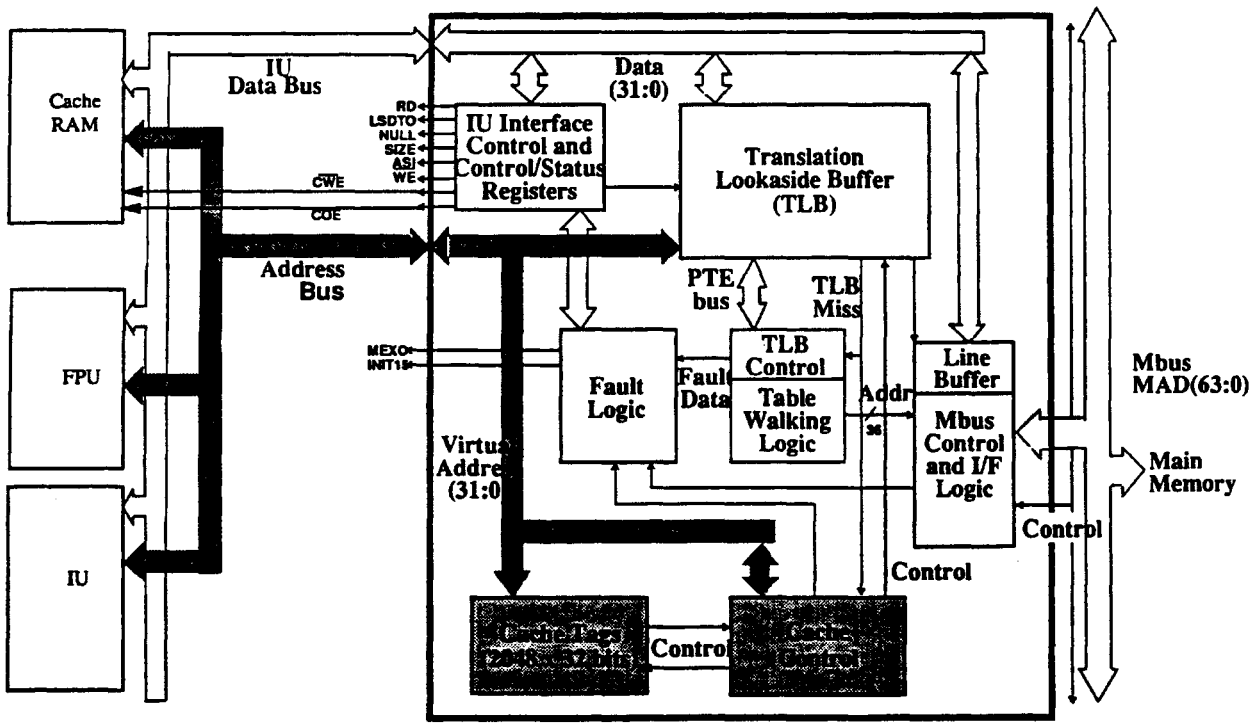
L64814 Floating Point Unit

- Single chip floating point coprocessor
- Interfaces directly to L64811 Integer Unit
- 64-bit internal data path for all operations
- IEEE exception handling directly in hardware
- Operating frequency: 25, 33, 40 MHz
- Performance up to 6.0 MFlops @ 40 Mhz

L64815 MMU, Cache Controller, Tags (MCT)

- SPARC reference MMU compatible
- Address Translation performed by Hardware (tablewalk)
- 64 entry TLB utilizing LRU replacement Algorithm
- Write through Cache Controller
- 64K and 128K Cache size support
- 2048 On-Chip Cache Tags
- Support for Cypress, Motorola and 386 type SRAMs
- High performance 64-bit Mbus
- Support of Block Copy and Block Zero functions
- Operating frequency 25, 33, 40 MHz

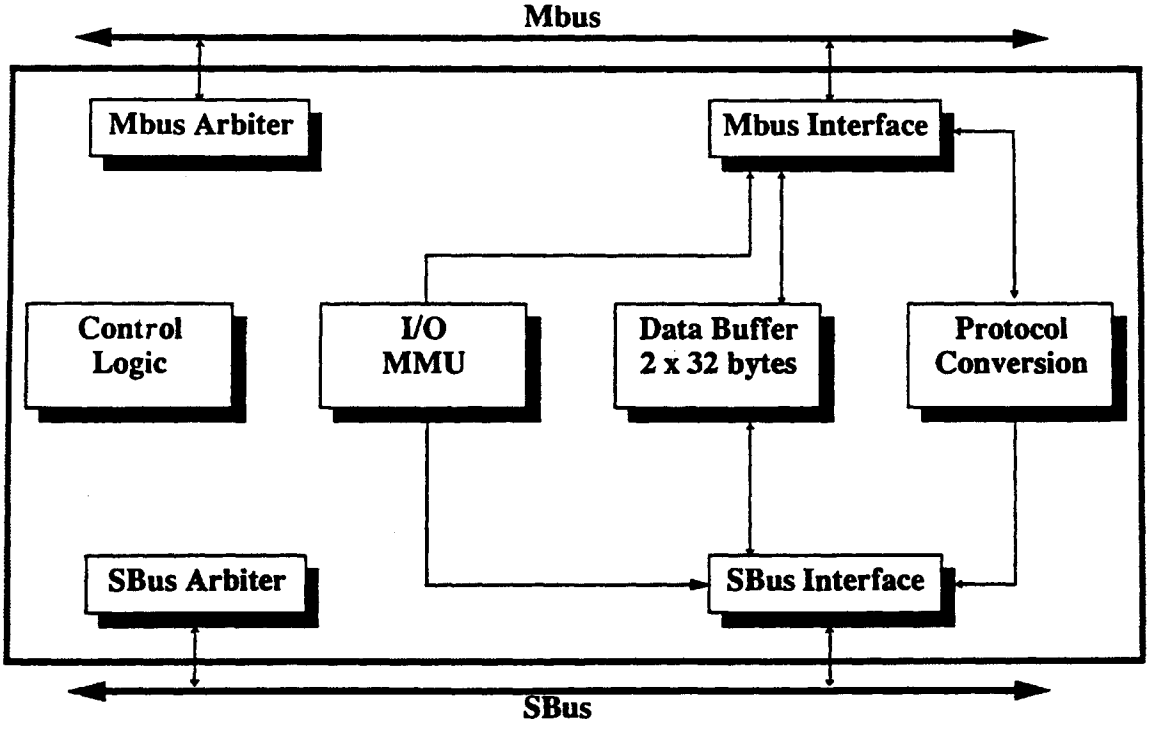
MCT Block Diagram



L64852 Mbus to SBus Controller (M2S)

- Provides Mbus Arbitration
- Provides SBus Arbitration
- On-board I/O MMU for SBus DVMA masters
- Mbus to SBus protocol conversion
- 32 Mbytes I/O space
- Perform Split-Read, Buffered Writes to optimize bus B/W
- Contains Watchdog timer

M2S Block Diagram



MBus Support

MBus Arbiter

- Supports Up to Four MBus Masters (i.e. M2S and three CPUs)
- Linear and Round Robin Prioritization Scheme
- MBus Master in M2S Receives Highest Priority (Ethernet Latency)
- Round Robin Arbitration Used for All Other MBus Masters
- Provides MBus Request and Grant Lines for Each Master
- Observes Bus Parking Feature Used by MBus Protocol

SBus Support

SBus Arbiter

- Supports Up to Six SBus Masters (i.e. M2S, DVMA, and four Slots)
- Linear and Round Robin Prioritization Scheme
- DVMA Receives Highest Priority (Ethernet Latency Requirements)
- Round Robin Arbitration Used for All Other SBus Masters
- Provides SBus Request and Grant Lines for Each Master

I/O Memory Management Unit

Overview

- Provides Virtual to Physical Address Translation
- Allocates Upper 32-Mbytes of the 4-Gbyte Virtual Address Space for I/O Devices Residing on SBus
- Allows for Single I/O Process Allocation of All 32-Mbytes
- Page Size Configuration of 4-Kbytes
- Single-Level Page Table Entry (PTE)
- Contains a 16 entry LRU TLB for I/O MMU

L64850 DRAM Memory Controller (DMC)

- Supports 1M x 9 and 4M x 9 DRAM Modules
- Supports up to 64 Mbytes total Memory space
- Supports Up to 2 banks (8 bytes/bank)
- Fast Page Mode (Mbus Burst transfers)
- On-board Data buffers
- Parity Error detection
- Cascadable
- Implements CAS before RAS Refresh scheme

L64851 Peripheral Controller (STDIO)

- Supports up to eight 8-bit Slave-type peripherals (I/O)
- Provides 64-bit Mbus interface to I/O devices
- 8-byte packing/unpacking
- Provides Interrupt Level encoding for up to 13 devices
- Provides 1 Megabyte address space per I/O device (8 Mbytes total)
- Contains Mbus Arbiter and Time-out Functions
- Up to 40 MHz maximum clock frequency

L64853/A SBus DMA Controller

- Single chip SBus Interface
- Supports 8/16-bit peripherals
- Handles 32-bit packing and unpacking
- Support for 16byte SBus Burst transfers
- Support for DMA chaining
- Supports byte, half word, or word transfers on SBus
- Supports SBus Rerun Acknowledgments
- 25 MHz clock frequency
- Low cost 120-pin Plastic Flat Pack (PQFP) package

The Rest of the Complete Solution

- Schematics (Manufacturing Kit)
- SunOS Port