"TRW CPUAX SuperChip"

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Introduction

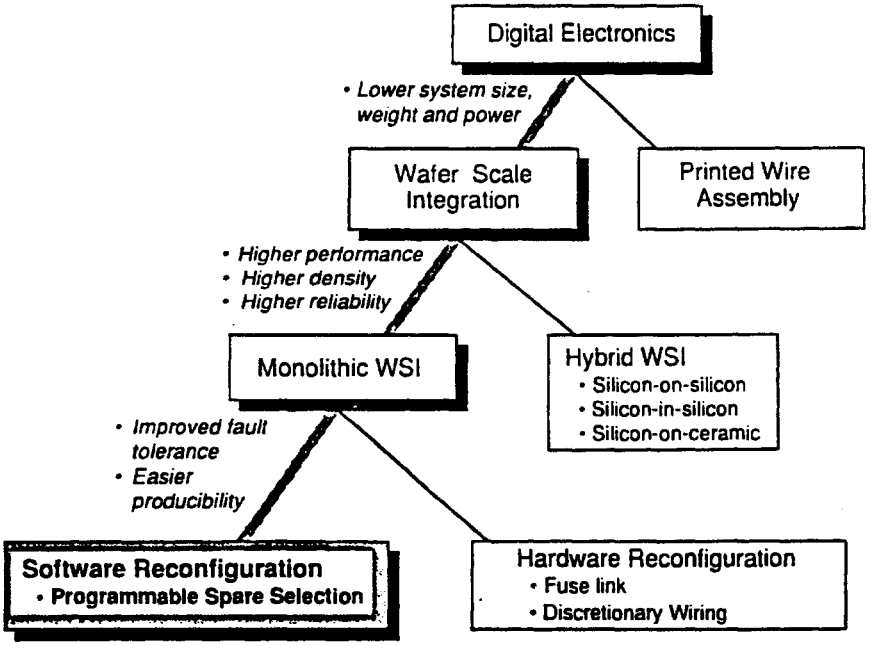
► **VHSIC Phase II Program**

- 1985/1991 Start/Completion
- Motorola/TRW Team
- Submicron CMOS Technology
- Central Processor Unit - Arithmetic Extended (CPUAX) SuperChip
- Three Support Chips - Universal Processor, Microcontrol Unit & Bus Interface Unit

► **Objectives**

- Monolithic Wafer-Scale Integration
- 0.5µm CMOS Process
- 100 MHz Clock Rate
- Functional Throughput Rate 10^{13} gate-Hz/cm^2
- Built-In Self-Test (BIST)
- On-Chip Redundancy & Programmable Reconfigurability

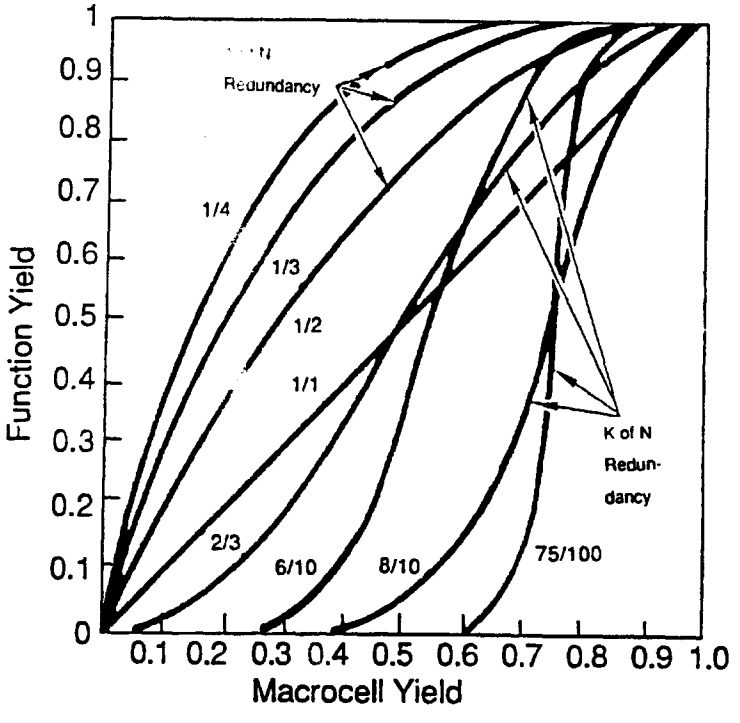
Evolution Of Digital Electronics



Software Reconfigurable Monolithic WSI Approach

- **Redundant VLSI Sparing**
  - Macrocells are functional building blocks
  - Macrosets contain N macrocells
  - K of N macrocell sparing to provide high yield
- **Triple Modular Redundant (TMR) Interconnect**
  - Macrosets communicate through TMR interconnect
  - Logically equal wires separated and voted
- **Built-In Self-Test**
  - Initiates, controls, monitors macrocell and interconnect tests
  - Configures SuperChip at system power-up

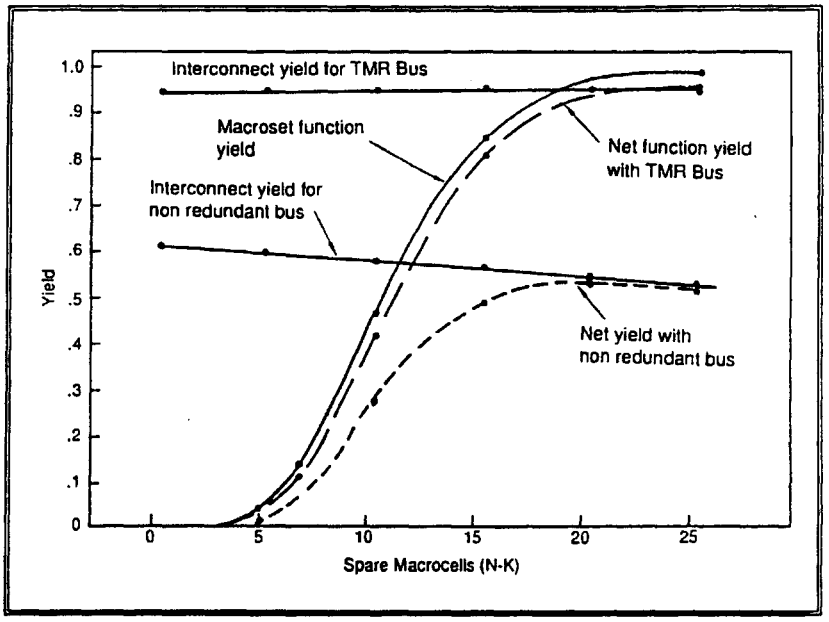
K of N Macrocell Sparing



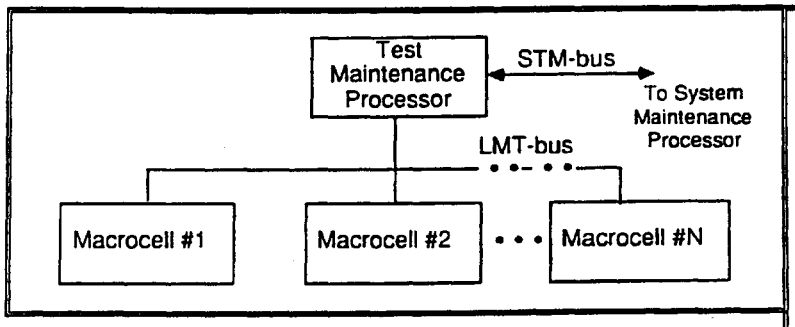
K - Number of macrocells in a macroset

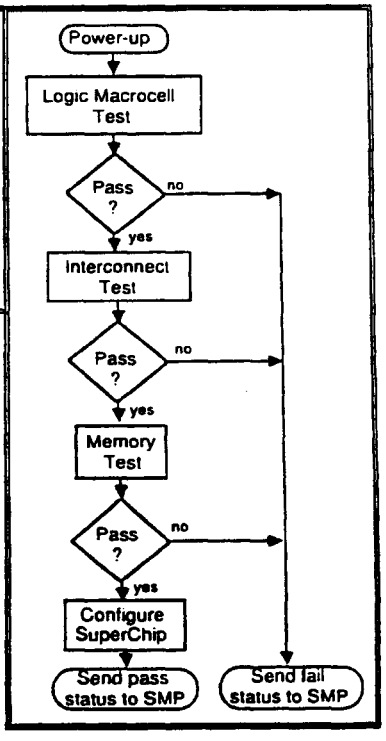
N - Minimum number of macrocells required for functionality

Triple Modular Redundant Interconnect



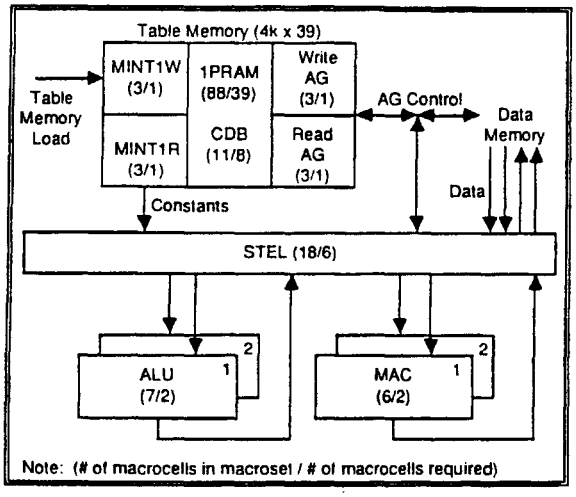
Built-In Self-Test Features





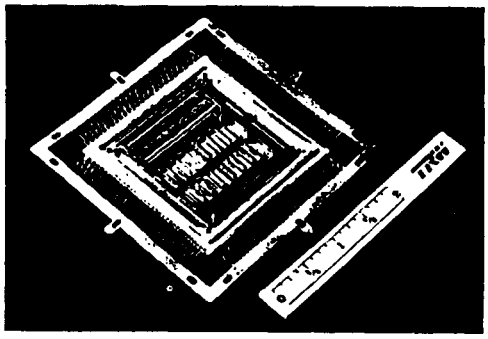
- BIST firmware initiates, controls and monitors macrocell testing and SuperChip configuration upon system power-up
  - Performed in four stages: logic macrocell test, interconnect test, memory test and configuration
  - Firmware is executed in less than 6 seconds by UP macrocell and support logic which forms the Test and Maintenance Processor (TMP)
- Logic Macrocell Test Bus (LMT-bus) passes messages between UP (master) and slave macrocells
- TMP sends 'pass' or 'fail' status to the off-chip System Maintenance Processor (SMP)

CPUAX SuperChip Features

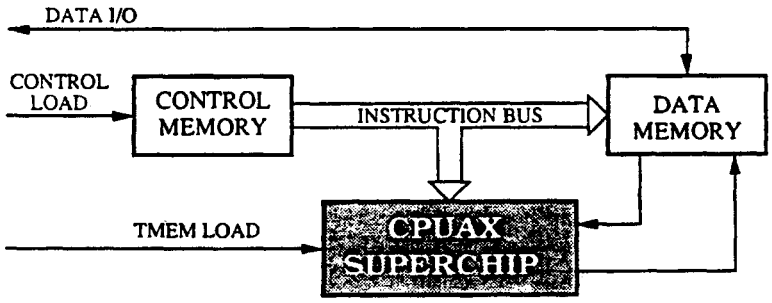


- 0.5 µm LOCOS CMOS
- 142 macrocells
  - 61 active macrocells (81 redundant)
  - 4.1 M devices with 1.7 M active
- 1.5 in. x 1.6 in. die size
- 8.5 W nominal power dissipation
- 275 I/O pins

- Executes digital signal processing algorithms
  - Dual floating point ALUs
  - Dual floating point MACs
  } (MIL-STD-1750A format)
  - 4 KW x 39-bit table memory (32-bit data + 7-bit SECDED)
  - Six storage elements (each 16 words x 32 bits)
- 200 MFLOPS maximum throughput
- External interface to data memory
  - AG control with two 32-bit input and output ports
- Instruction code provided by external control memory
- Supports built-in self-test functions

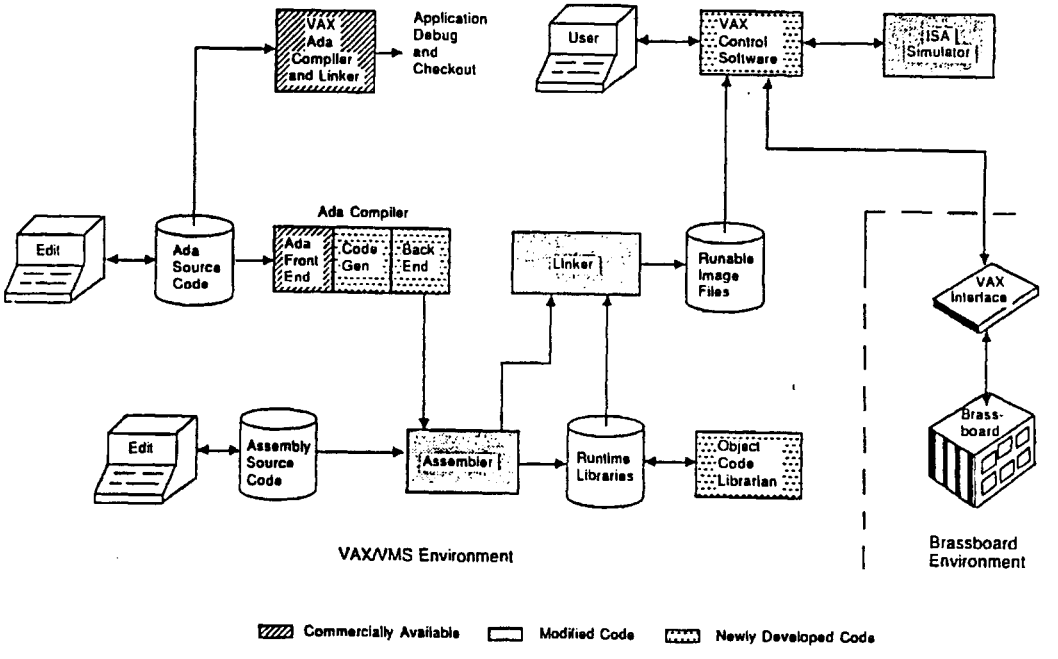


CPUAX SuperChip System Architecture

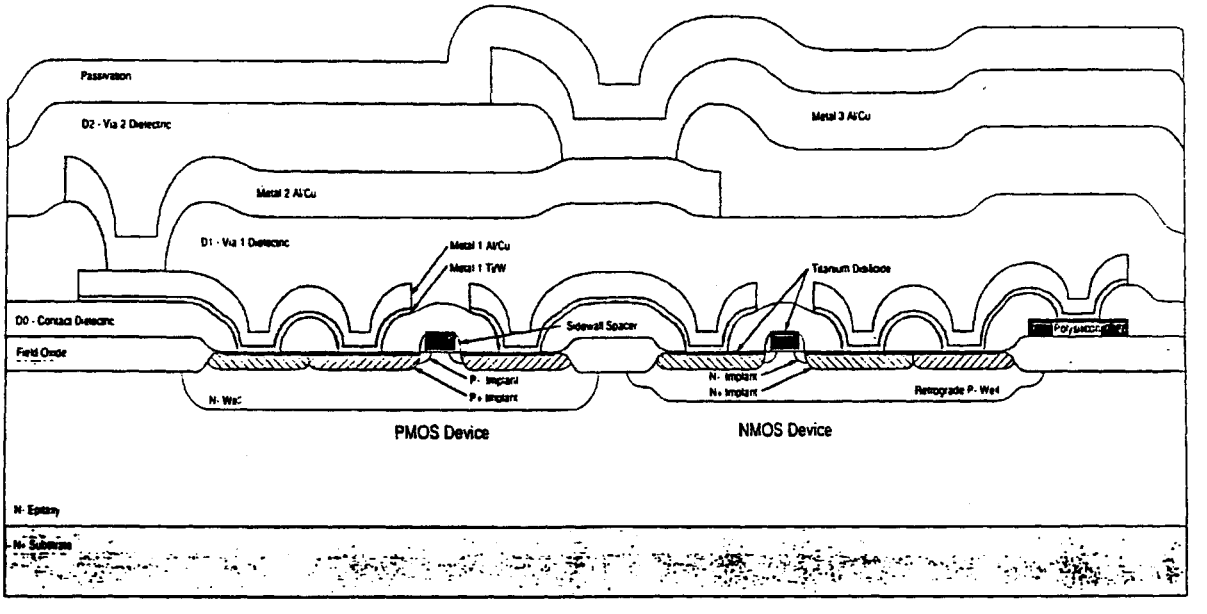


- Typical CPU architecture with the CPUAX as the processing node
- CPUAX will support an I/O bandwidth of 200 million words per second (MWps)
  - Optimized for dual-port data memory

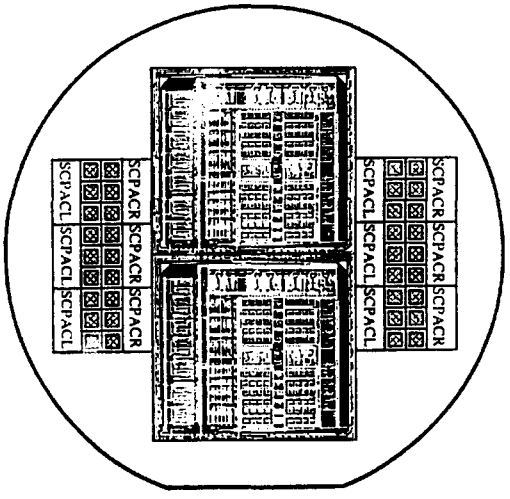
Support Software Environment



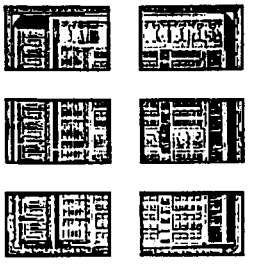
0.5µm CMOS Technology



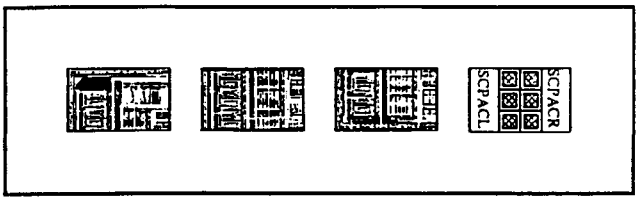
CPUAX Fabrication Techniques



CPUAX Wafer Layout

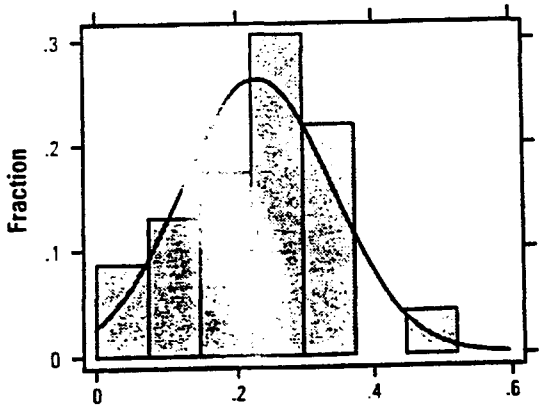


CPUAX Exposure Fields

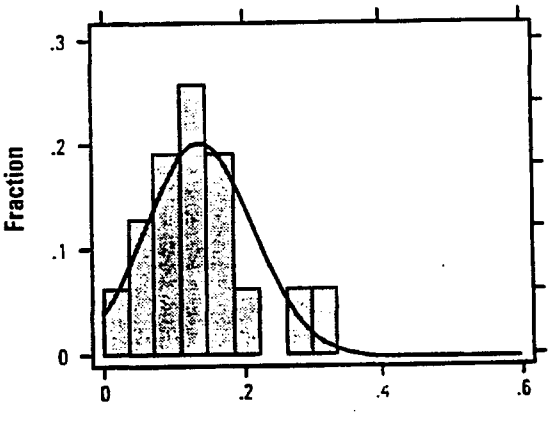


Ultratech 1500 Reticle

Optical Stepper Interfield Boundary Stitching Accuracy

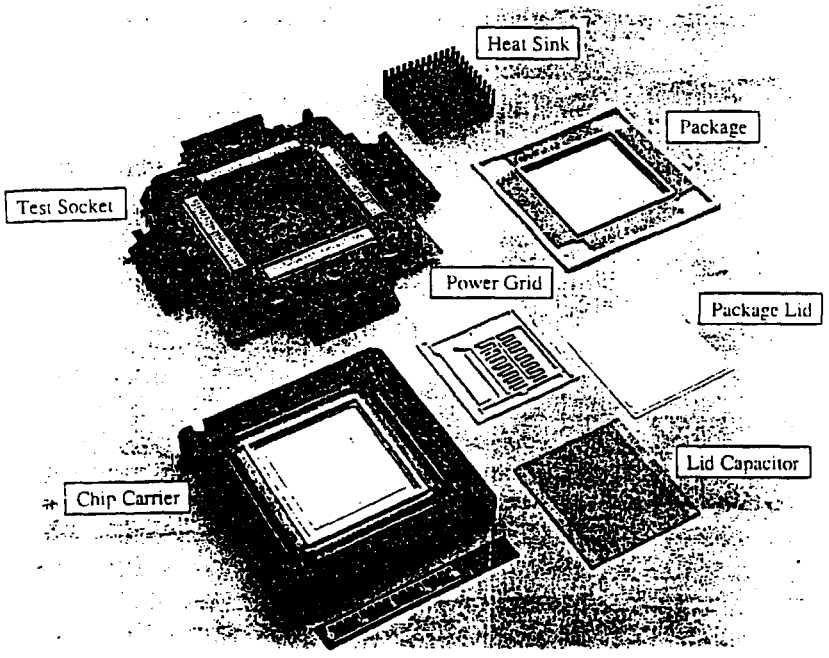


Horizontal error (µm)

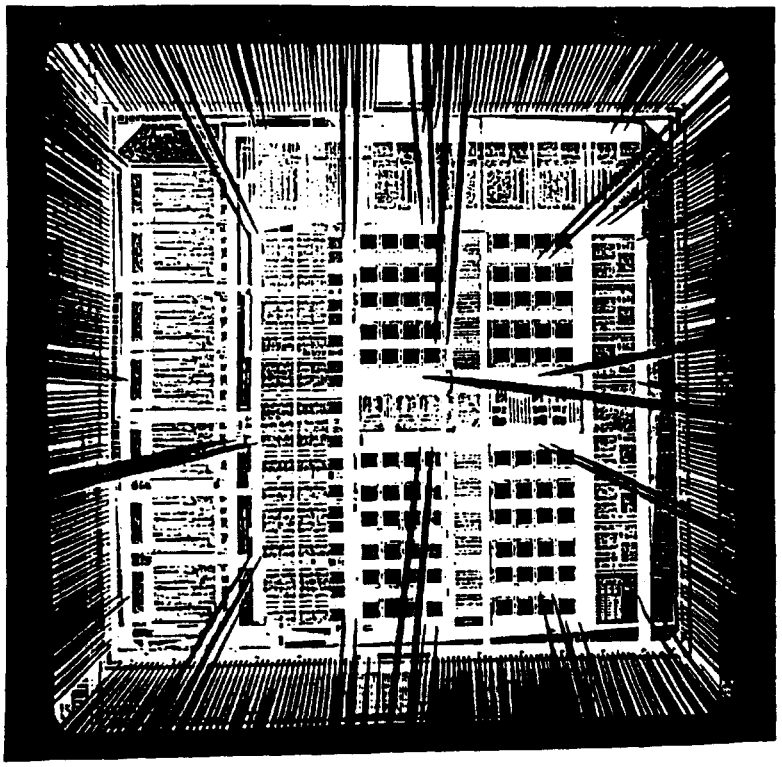


Vertical error (µm)

CPUAX SuperChip Assembly

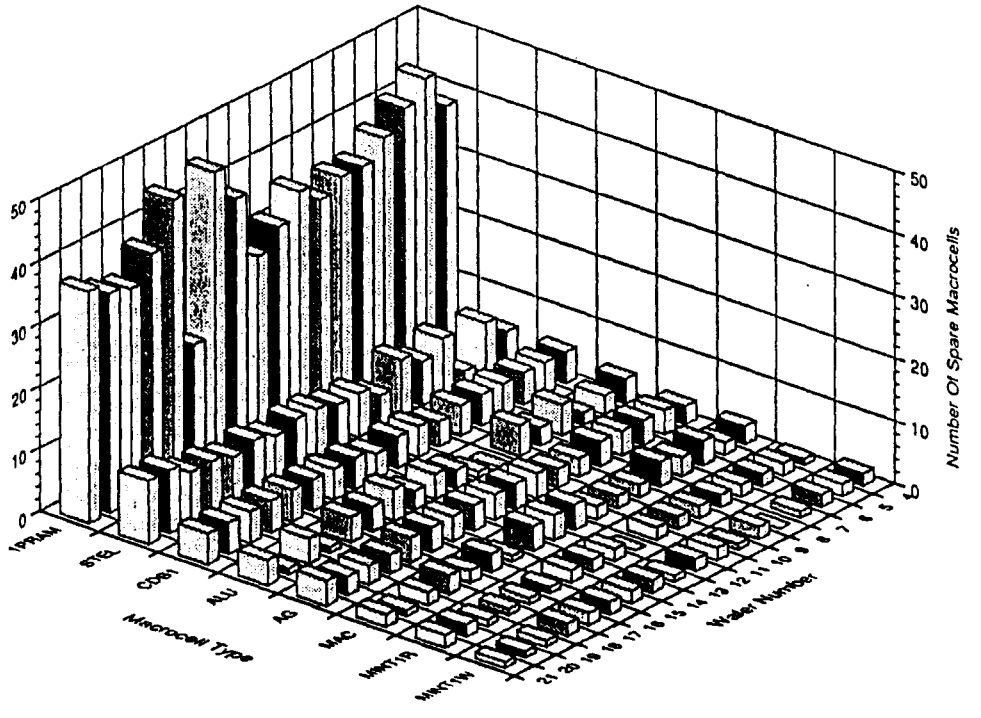


CPUAX SuperChip Probe Test

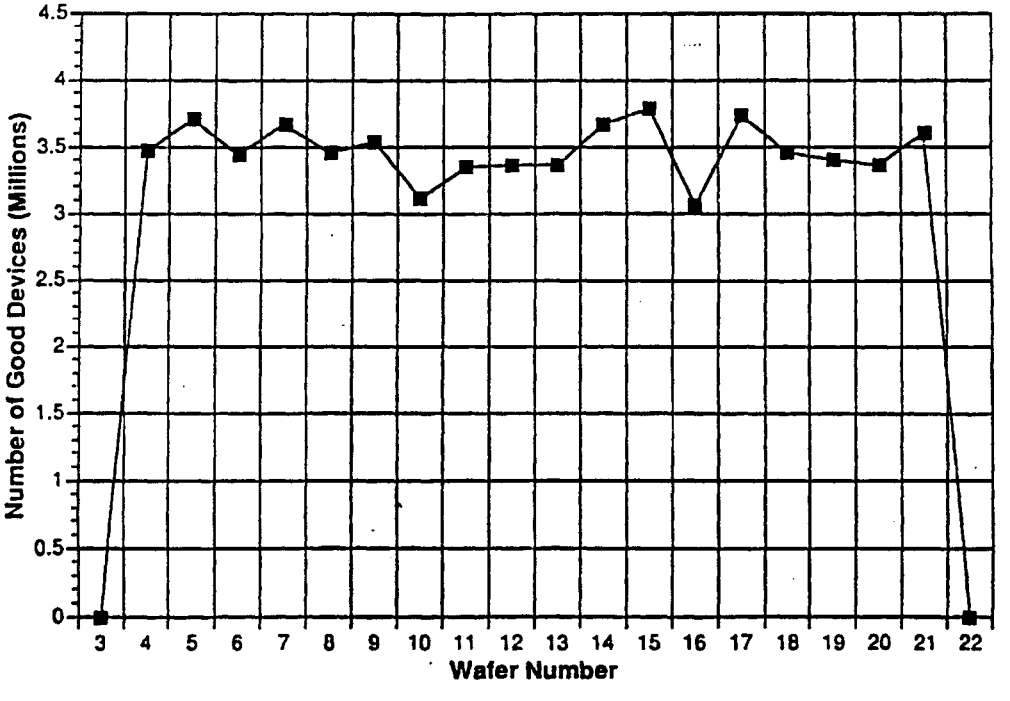


- Custom Rucker & Kolls Probe Card
- 360 Pin Probe Card
  - 286 Signal Pins
  - 50 Edge Power/Ground Pins
  - 24 Internal Power/Ground Pins
- 4.8 x 4.8 cm Opening

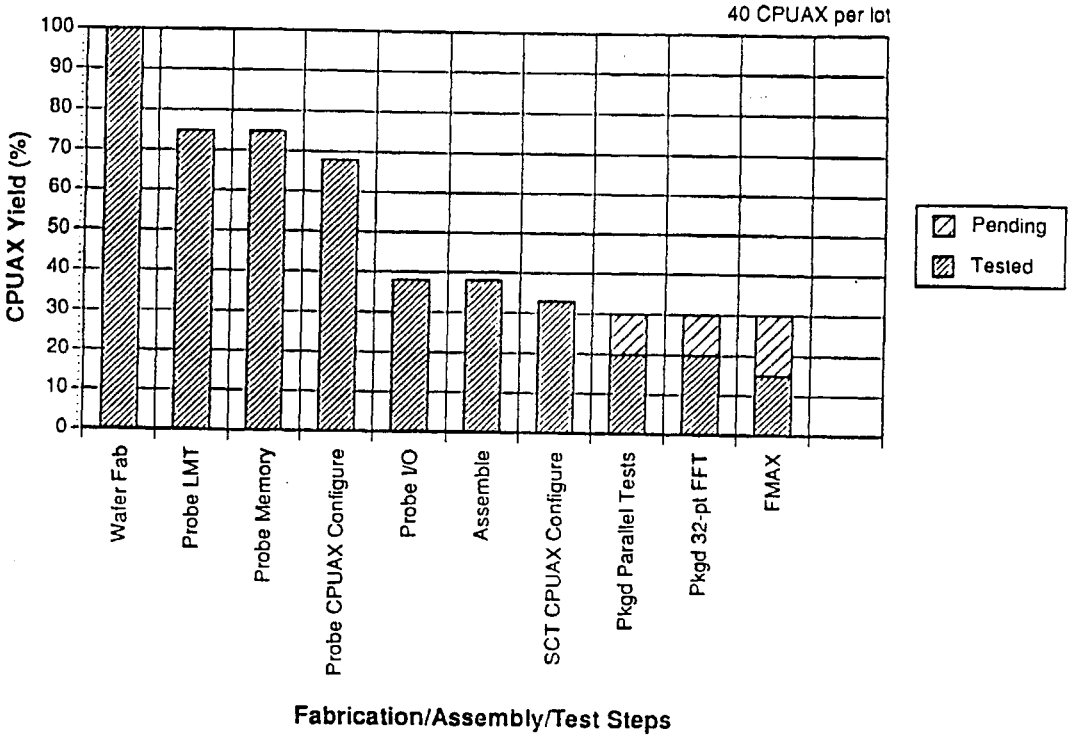
Spare Macrocell Yield (Lot CX-4)



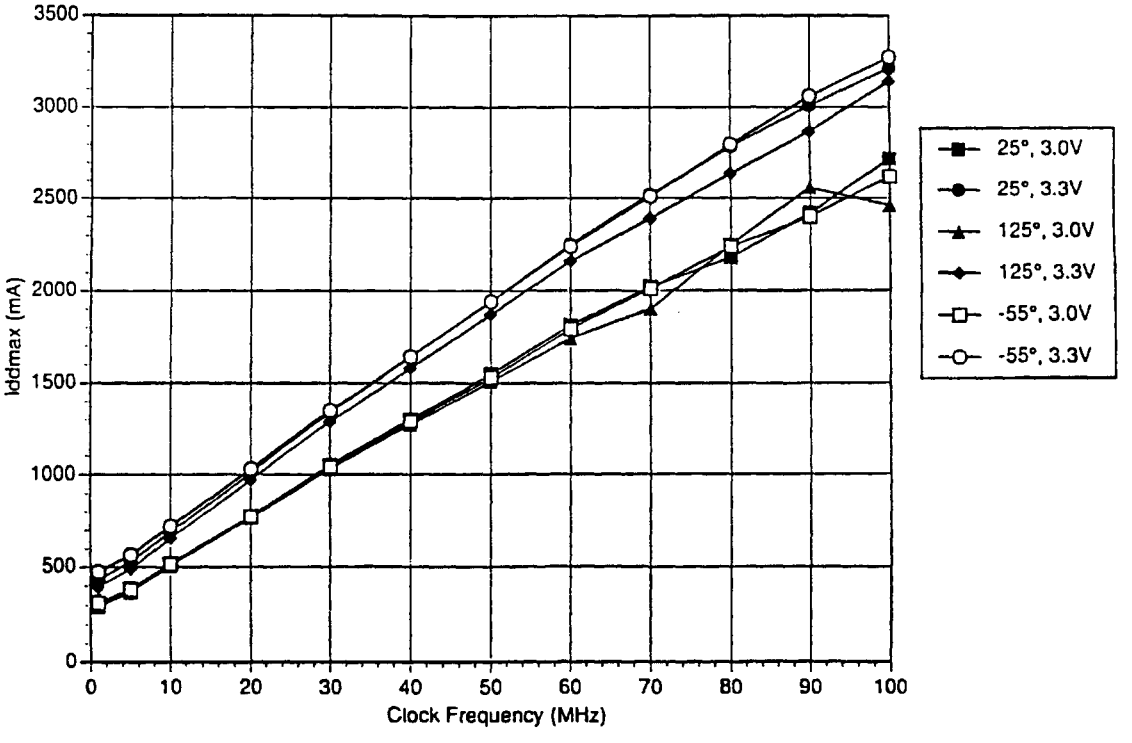
Cumulative Transistor Yield (Lot CX-4)



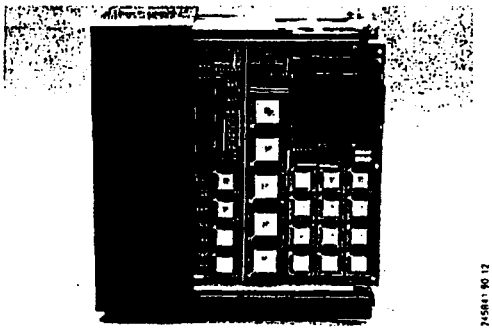
Pareto Yield Analysis (Lot CX-4)



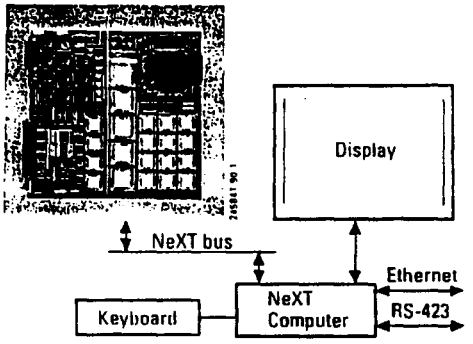
CPUAX Power Performance (S/N 022)



CPUAX Enables High Performance Signal Processor for NeXT Computer



NeXT Workstation



CPUAX/NeXT Computer Interface

- CPUAX-based vector co-processor board
- Targeted at computationally intenstive, high throughput signal processing applications
- Form, fit and function compatible with NeXT computer
- Provides hardware and application code development environment for CPUAX insertions

Performance

- 50 million floating point operations per second at 25 MHz
- 32 bit floating point/24 bit integer with multiple precision support
- 256K byte scratch pad memory with dedicated read and write address generators
- 8M byte I/O buffer memory
- Microcontrol unit with 4K instruction memory
- On-board bootup/configuration logic

Summary

- Demonstrated the design of a software-reconfigurable monolithic wafer-scale integration circuit
- Developed a 0.5μm CMOS technology capable yielding high transistor count circuits (>1.5M) and sustaining high clock rates (100 MHz)
- CPUAX can provide high throughput (200 MFLOPs) for general purpose signal processing for a variety of system applications
- Yield enhancements can be made through improved macrocell sparing and control over single point induced failures in nonredundant I/O circuitry
- The CPUAX has been demonstrated as a coprocessor element in the NeXT computer work station