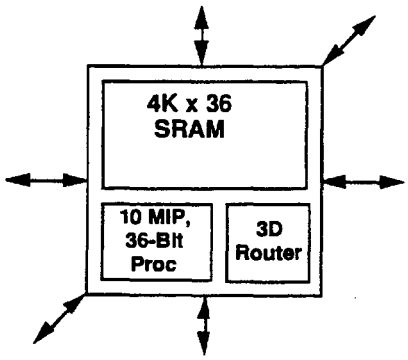
The Message Driven Processor

Dally, Ahmed*, Carrick*, Chien, Davison*, Fiske, Fyler*, Horwat, Keen, Lear*, Lethin, Nguyen*, Noakes, Nuth, Vestrich*, Wills

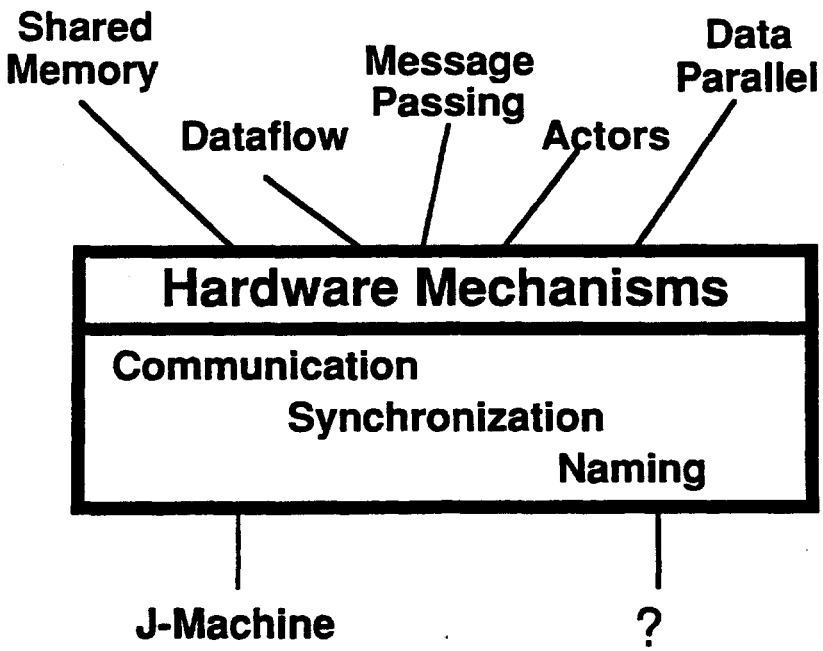
MIT AI Laboratory and Intel*

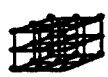
Hot Chips III, August 1991



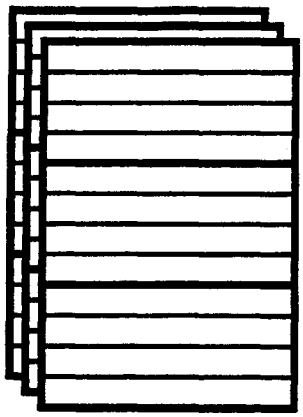
- Integrated Multicomputer building block
  - 36-bit 10MIPS Processor
  - 3D Network with router- 6 x 300Mb/s
  - 18KB SRAM + ECC DRAM Control
- General-Purpose Mechanisms
  - SEND Instruction/ Message dispatch
  - Synchronization tags
  - General Translation

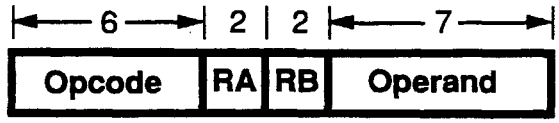
Mechanisms





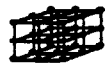
Instruction Set Architecture





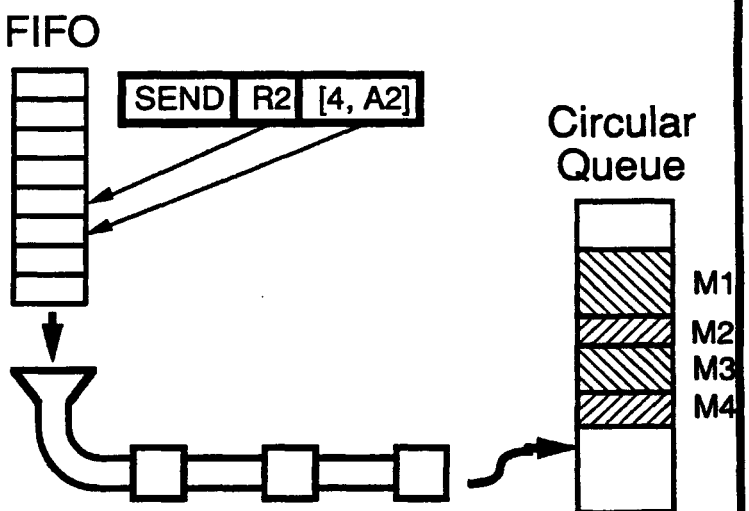
RA <-- RB (op) Operand
Operand <-- RB

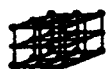
- 17-bit 3-address instructions (2 per 36-bit word)
- 3 Hardware contexts with fast (3 cycle) switching
- SEND, SUSPEND, XLATE instructions.



Communication

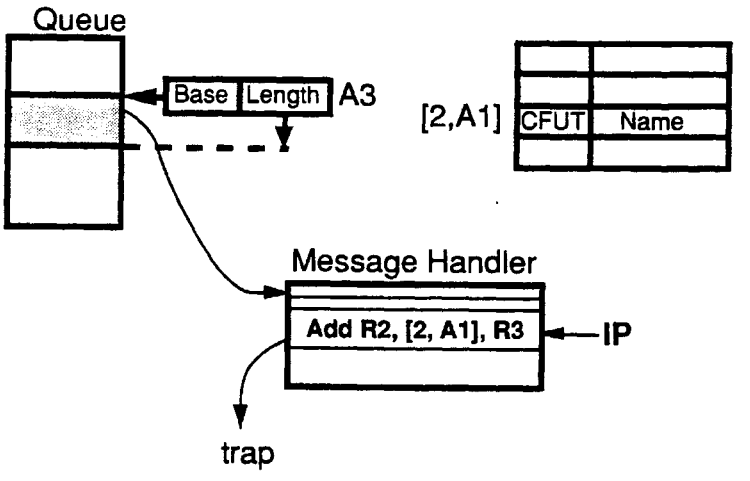
- SEND instruction injects messages.
- Delivery by routing network
- HW allocation and buffering
- Process created and dispatched on message arrival





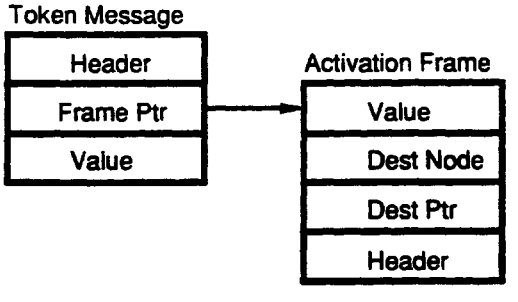
Synchronization

- Process creation and dispatch on message
- Hardware scheduling of processes
- Trap on presence tags in memory and registers
- Fast context switching



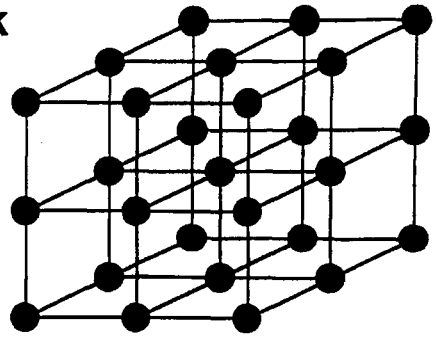
Example - Dynamic Dataflow Firing

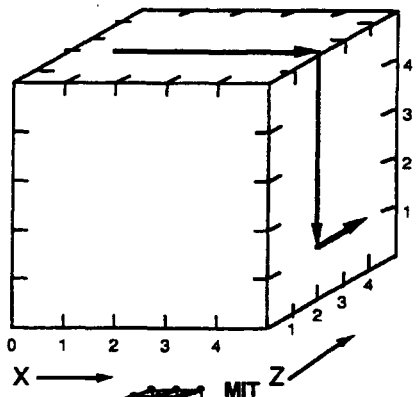
```
ADD: MOVE   [1,A3],R0      ; Frame ptr
     MOVE   R0,A2
     MOVE   [2,A3],R0      ; Value
     ADD    R0,[0,A2],R0   ; Fault if not present
     MOVE   [3,A2],R1      ; Dest 1
     SEND2  [1,A2],R3,0    ; Send dest, header,
     SEND2E [2,A2],R0,0    ; value, and frame
     SUSPEND               ; Process next msg
```



Network

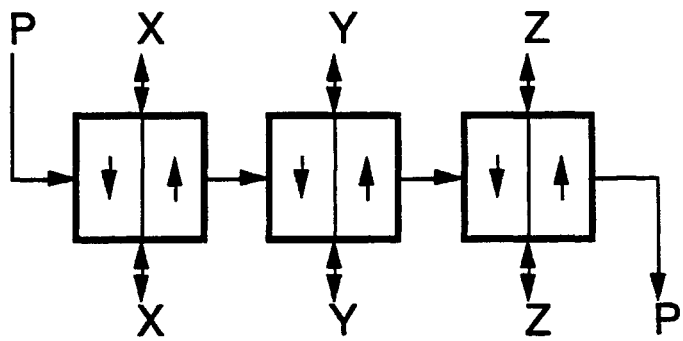
- 3-D mesh - up to 32x32x64
- 6 bidirectional channels each 9bits @ 33MHz
- Latency 120ns/word + 60ns/hop
- Deterministic X,Y,Z routing
- Blocking flow control
- Synchronous
- Autonomous from processor

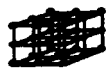




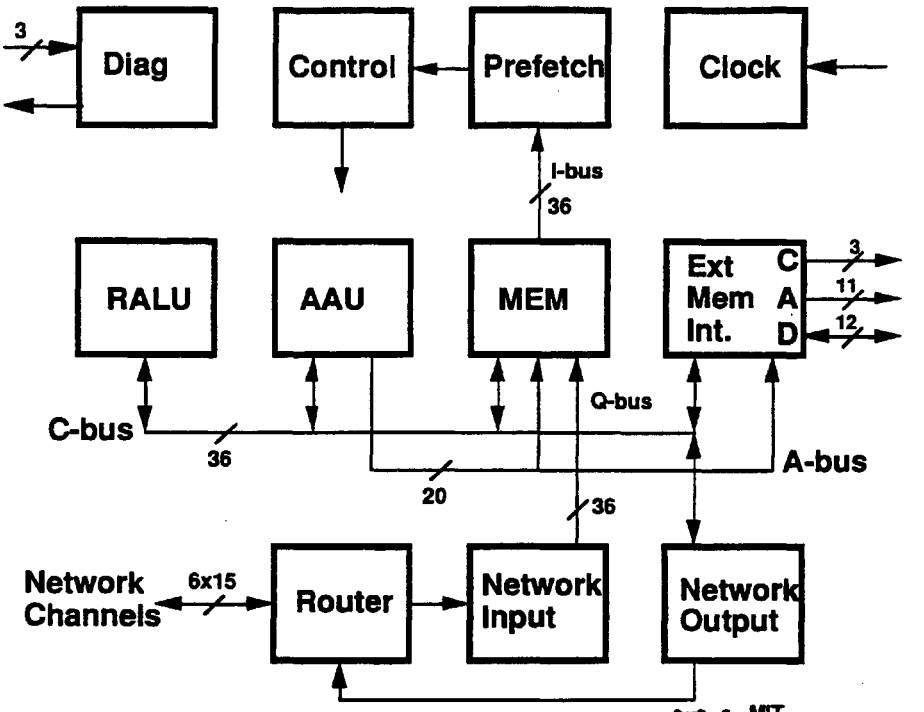
Network Implementation

- Two 9-bit phits/cycle on each channel
- 2-priorities x 3-dimensions x 3-directions = 15 datapaths
- Routing with absolute addresses
- Channels may turn around each cycle
- Tolerates clock skew





Block Diagram

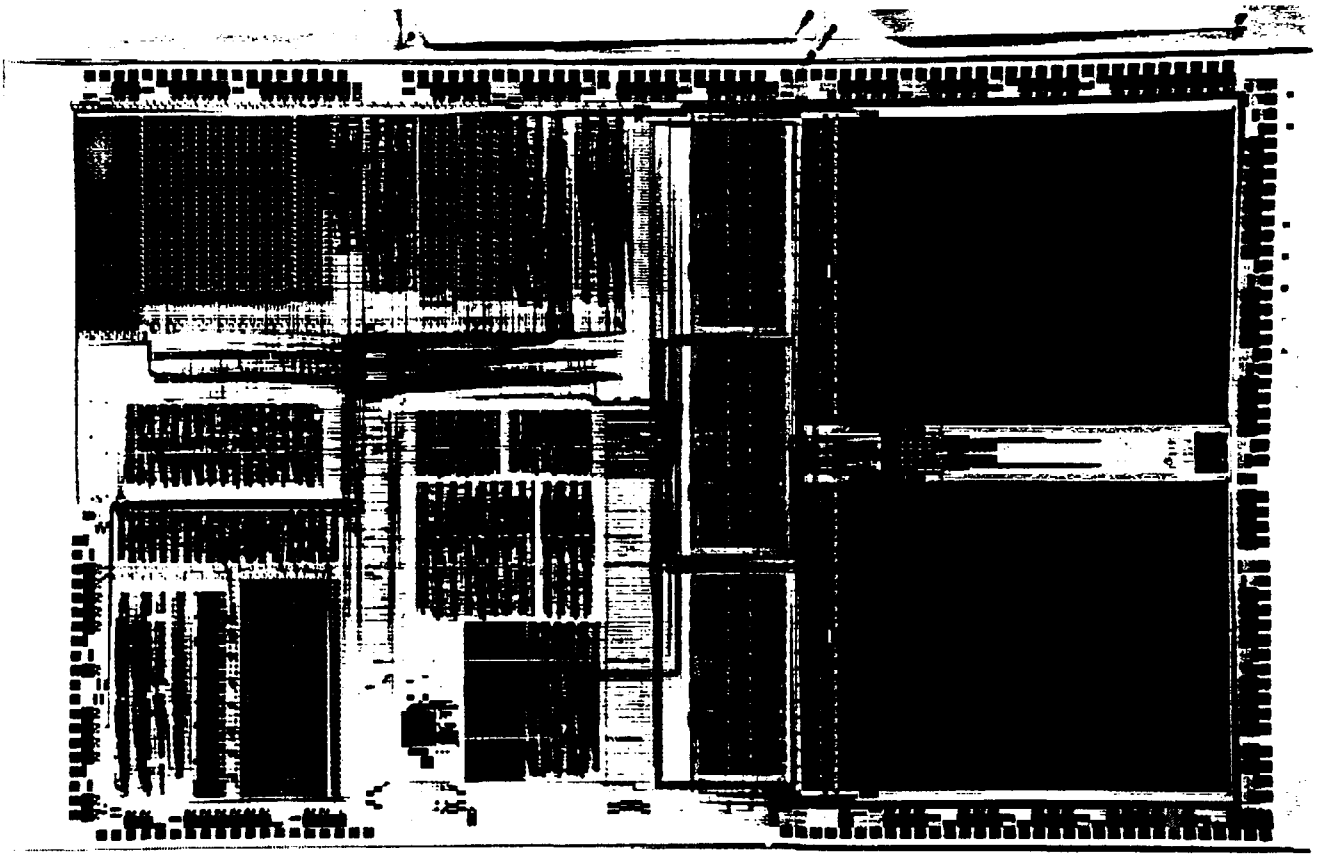


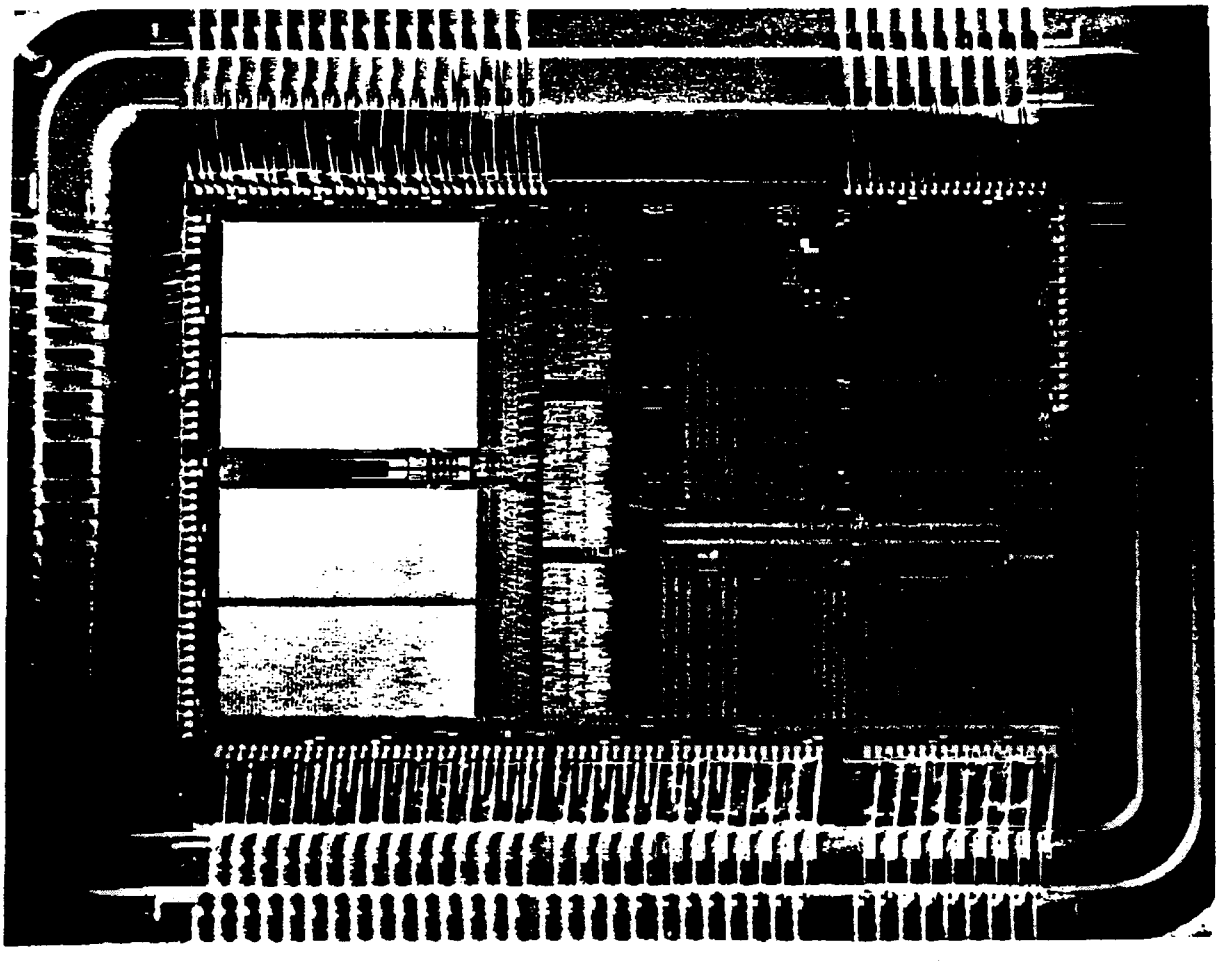
MIT
Concurrent VLSI
Architecture Group

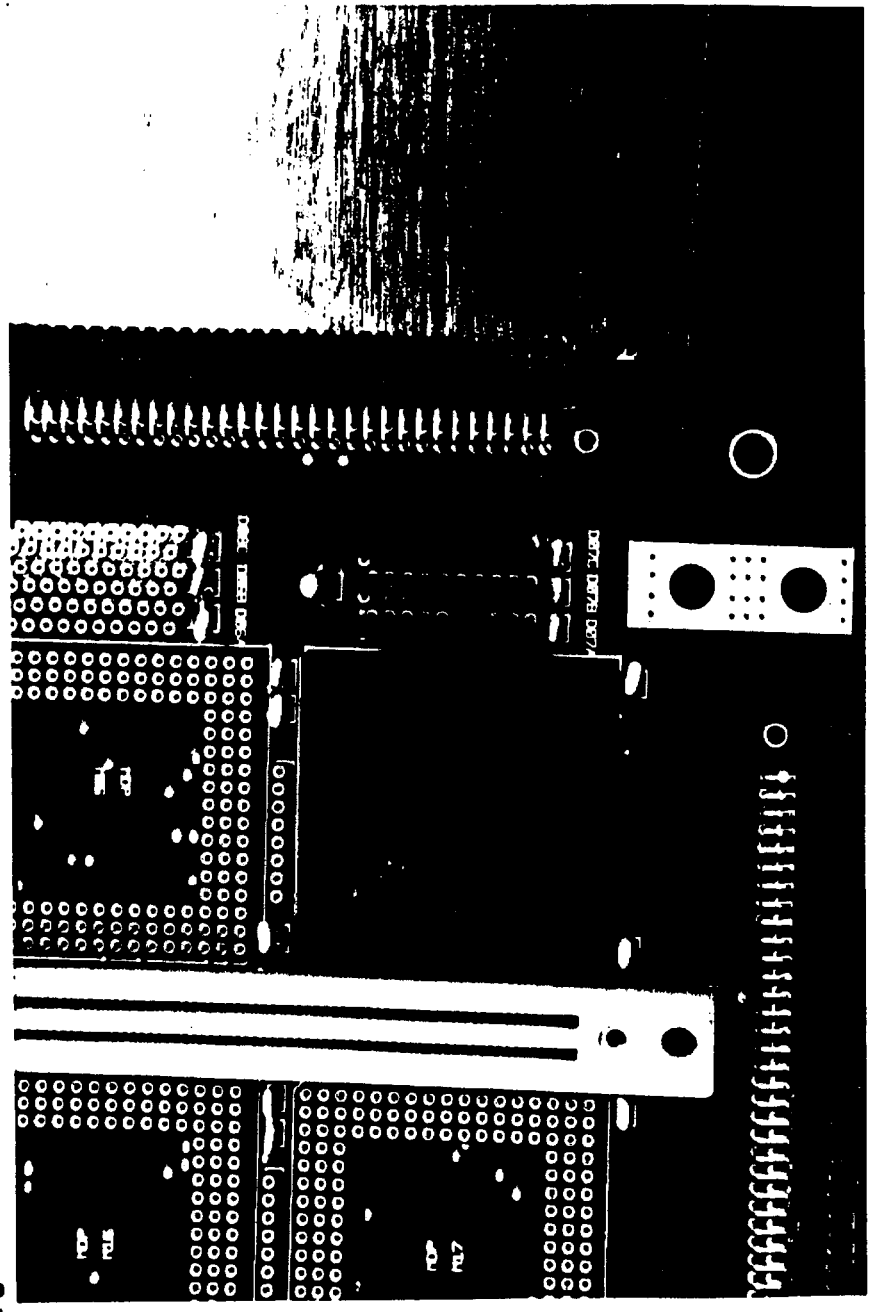
Area and Device Counts

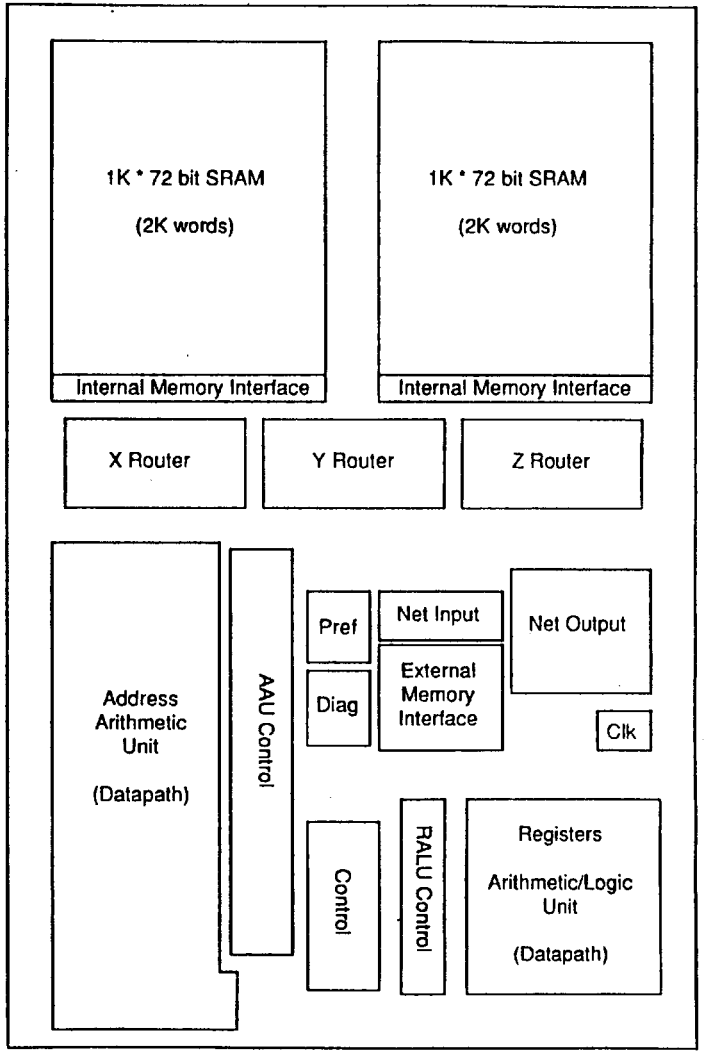
Unit	Area (mm x mm)	Area (mm^2)	Devices (x1000)
AAU	3.7 x 7.0	25.9	75.2
RALU	3.7 x 2.9	10.7	39.4
DIAG	0.9 x 1.1	1.0	3.7
PREF	0.9 x 1.1	1.0	3.2
CNTL	1.1 x 2.6	2.9	8.7
IMEM	7.8 x 0.5	3.9	13.4
EMI	1.6 x 1.8	2.9	9.0
NETIN	1.8 x 0.7	1.3	4.4
NETOUT	2.1 x 1.8	3.8	18.2
ROUTERS	8.4 x 1.3	10.9	29.2
RAM	8.8 x 4.9	43.1	880.0
CLOCK	0.7 x 0.8	0.6	0.1
PADS	50.5 x 0.2	8.4	2.6
FULL CHIP	10.2 x 15.0	153.0	1087.1

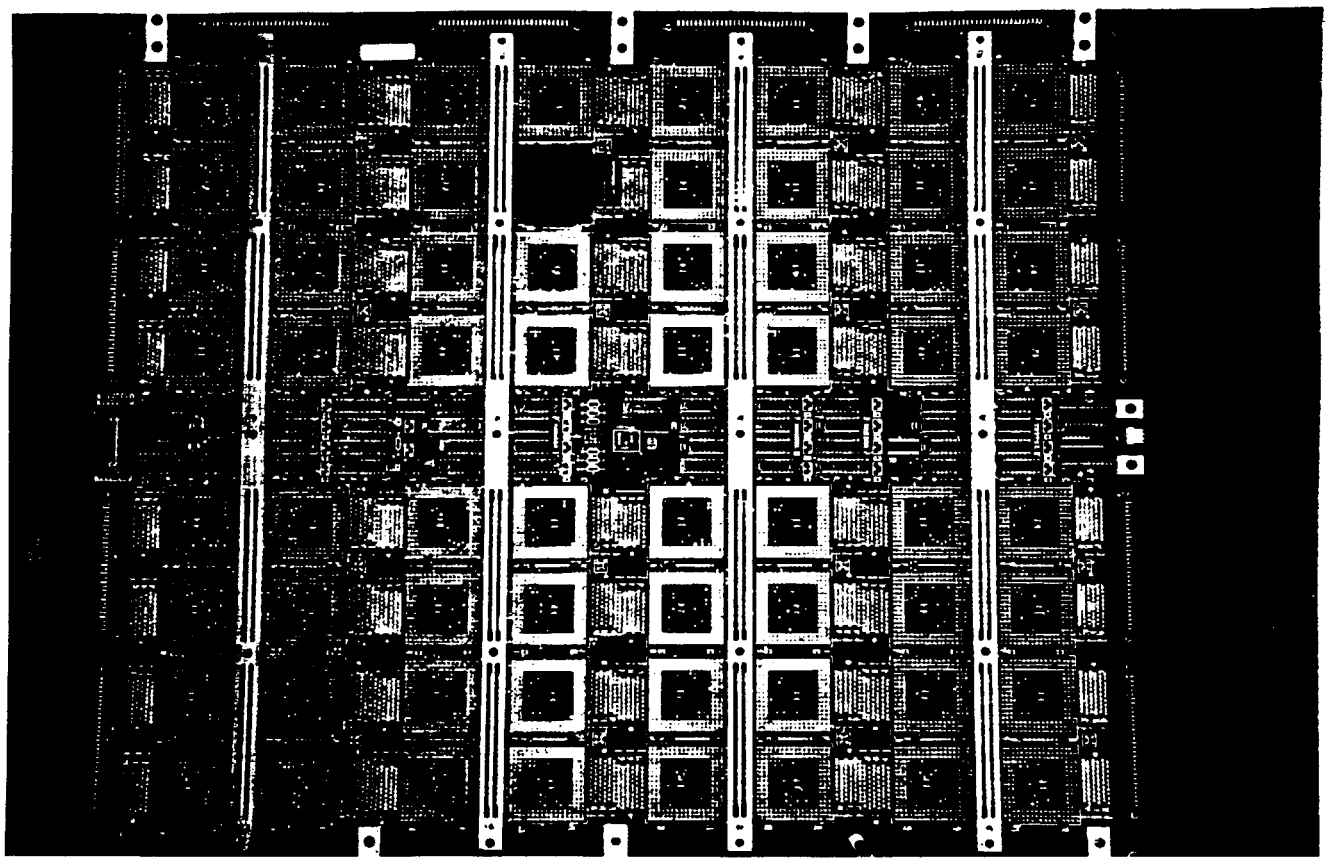
MIT
Concurrent VLSI
Architecture Group





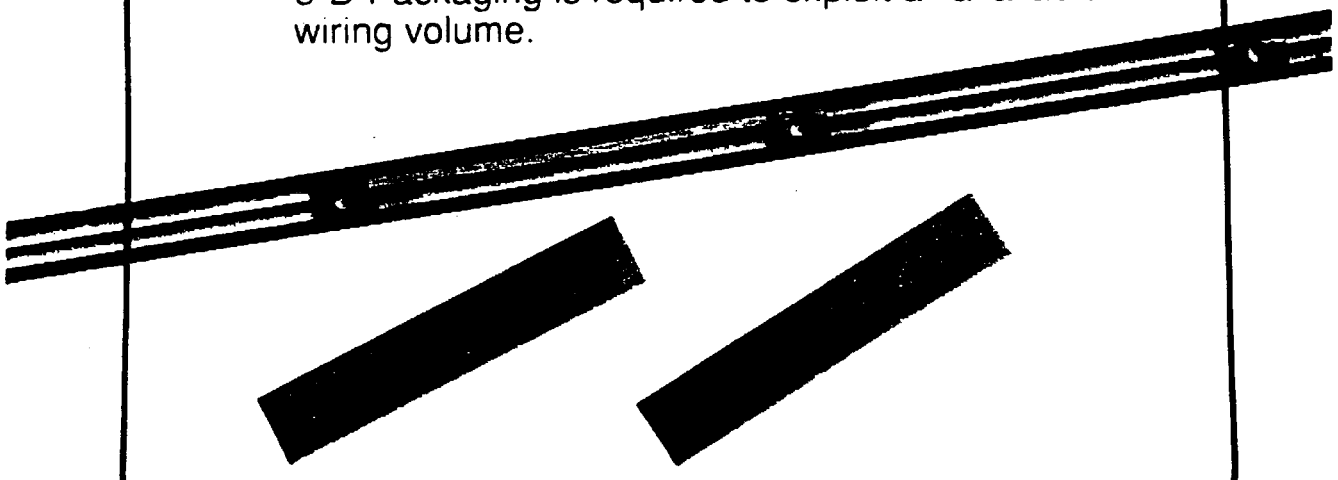



1K * 72 bit SRAM
(2K words)
Internal Memory Interface
1K * 72 bit SRAM
(2K words)
Internal Memory Interface
X Router
Y Router
Z Router
Address Arithmetic Unit
(Datapath)
AAU Control
Pref
Diag
Net Input
External Memory Interface
Net Output
Clk
Control
RALU Control
Registers
Arithmetic/Logic Unit
(Datapath)



Elastomeric Connector

- 3-D Packaging is required to exploit all available wiring volume.



Schedule

	Start	End
• Architecture	10/86	8/88
• RTL Design	6/88	12/89
• OS and Compiler	6/87	6/89
• Logic design	11/88	3/90
• Layout	6/89	12/90
• First Silicon		6/27/91
• Boots OS & Runs Program		7/16/91

CAD Tools and Methods

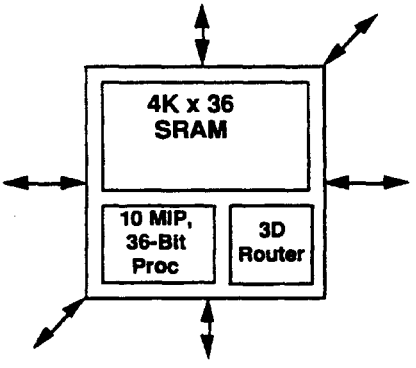
- Simulators:
  - Message-level
  - Instruction-level
  - RTL (C-code)
  - Logic & Switch-Level (Richsim)
- Schematic Entry: ORCAD
- Layout and checking: Intel Proprietary
- Regression suite (50,000 lines)
- Bug list and "Puck"
- Design reviews (RTL and Schematics)

J-Machine Software

- Concurrent Smalltalk (CST)
  - Object Oriented derivative of Smalltalk
  - 20 instruction process length
- COSMOS Operating System
- Id - Dataflow language
- Shared Memory
  - Hierarchical coherence protocol
- Applications

Conclusion

- General-purpose mechanisms for multicomputers
  - Communication
  - Synchronization
  - Translation
- Physically efficient design
  - More working silicon
  - Parallel communication



- University research projects can build >1M transistor chips.