HOT CHIPS SYMPOSIUM III

PA-RISC PROCESSOR FOR "SNAKES" WORKSTATIONS

TECHNICAL OVERVIEW

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Focus of New PA-RISC Processor

- Extend Family of Object-Code Compatible PA-RISC Implementations Down to Low Cost Desktop Systems
- Improved Capabilities on Numerical and Graphics Applications
- First Design to Implement Architected Extensions to PA-RISC

  First PA-RISC Designed in Partnership with External Silicon Supplier

Design Goals

- Balanced, High Performance on a Variety of Applications
  - Engineering, Scientific, Graphics, Multiuser, Transaction Processing, Commercial
- Consistent with Low Cost, High Volume Manufacturing
- Accelerated Design Schedule
- High Degree of Price/Performance Scalability
- HP Quality and Reliability

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Accelerated Design Schedule Goal
Influence on Design

- Existing Technologies Used
  - HP CMOS26 Technology
  - TI EPIC-2 Technology
  - Ceramic Pin Grid Array Packages
  - Industry Standard SRAMs
- Leverage of Previous Circuit Designs
  - TI Floating Point Megacells
  - Previous CMOS26 PA-RISC Design
- Design Emphasis on Reduced Complexity
- Thorough Verification at Transistor, Chip, System Levels
  - Fully Functional First Silicon
- Heavy Reliance on Design Productivity Tools
  - < 12 Month CPU and FPC Design Cycle

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Processor Components Overview

- Central Processing Unit (CPU)
  - HP Custom Design
  - HP CMOS26 Technology
- Floating Point Coprocessor (FPC)
  - Joint HP/Texas Instruments Design
  - TI EPIC-2 CMOS Technology
- Separate Instruction and Data Caches
  - Discrete Industry Standard TTL I/O SRAMs

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CMOS PA-RISC Vital Statistics

• Architecture	:	PA-RISC v 1.1
• Clock Frequency	:	0-66 MHz
• Instruction Cache	:	Virtual Index, Direct-Mapped, Physical Tag, 4 KB-1 MB, Discrete SRAMs, 32 Byte Line
• Data Cache	:	Virtual Index, Direct-Mapped, Physical Tag, 4 KB-2 MB, Discrete SRAMs, 32 Byte Line, Copy Back, 64 Bits
• Physical Memory Address	:	32 Bits
• Virtual Address	:	48 Bits
• Instruction TLB	:	96 Page Entries, 4 Block Entries, Fully Associative
• Data TLB	:	96 Page Entries, 4 Block Entries, Fully Associative

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Performance Overview

Processor Performance Equation:

$$\text{PERFORMANCE} = \frac{1}{\text{Path Length} \cdot \text{Cycle Time} \cdot \text{CPI}}$$

Architecture	Timing Design	Implementation:
Compilers	Technology	Pipeline
Operating System		Caches/TLBs
Application		Floating Point
		(Compilers)

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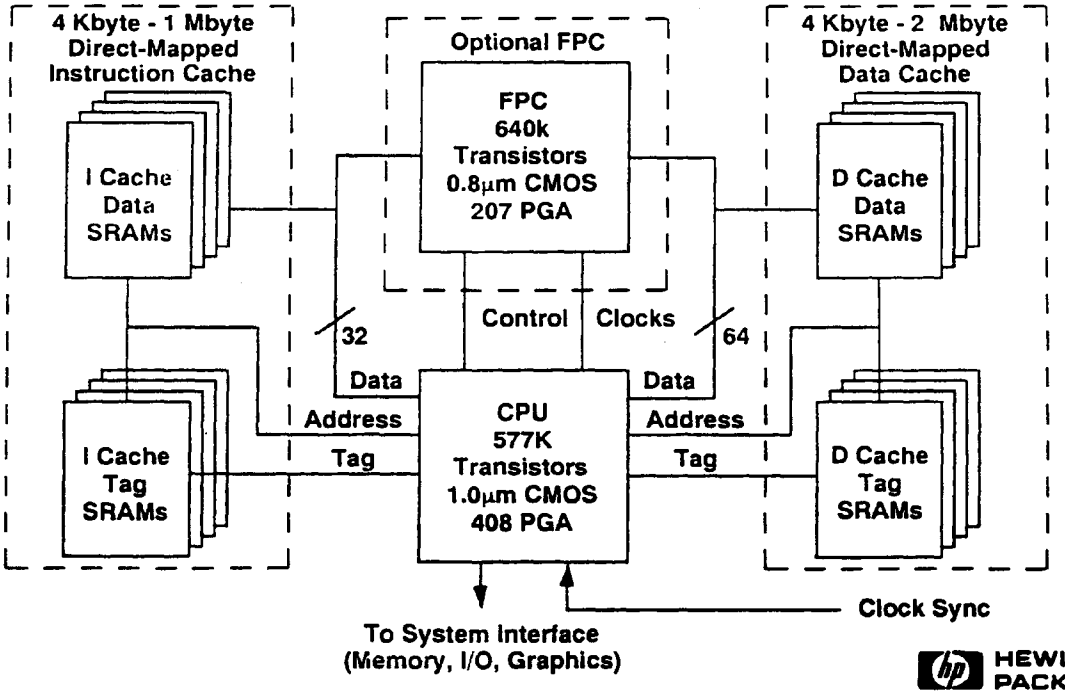
PA-RISC Processor Block Diagram



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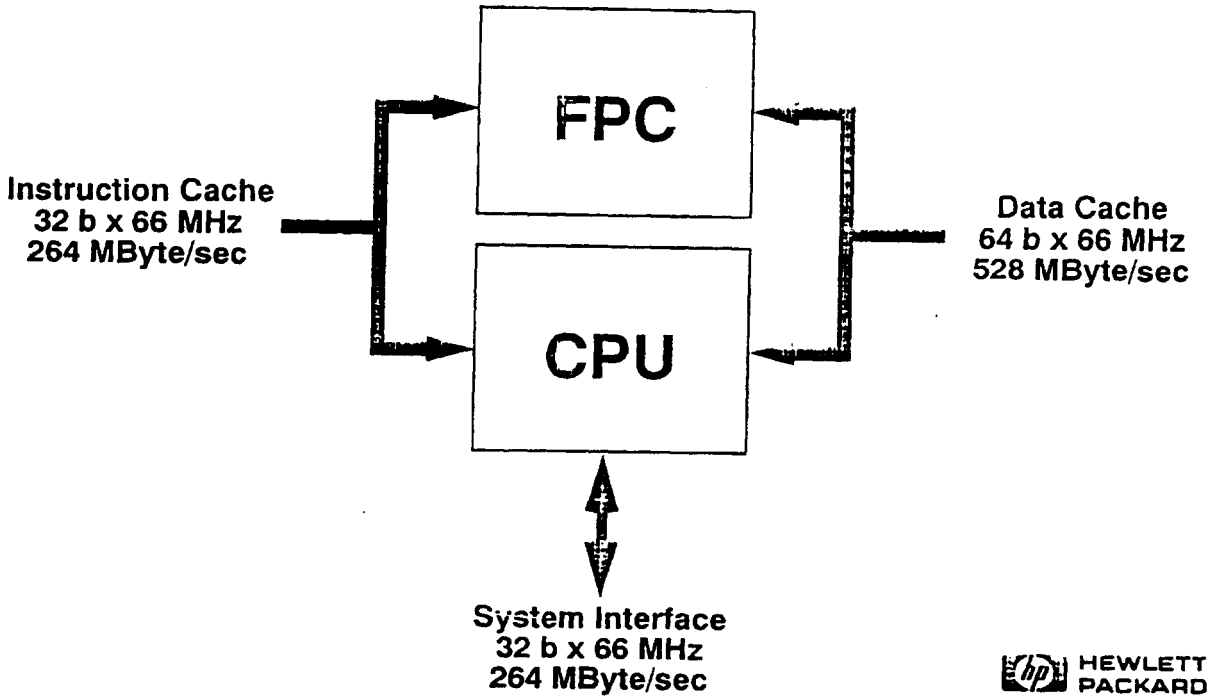
Interconnect Bus Performance



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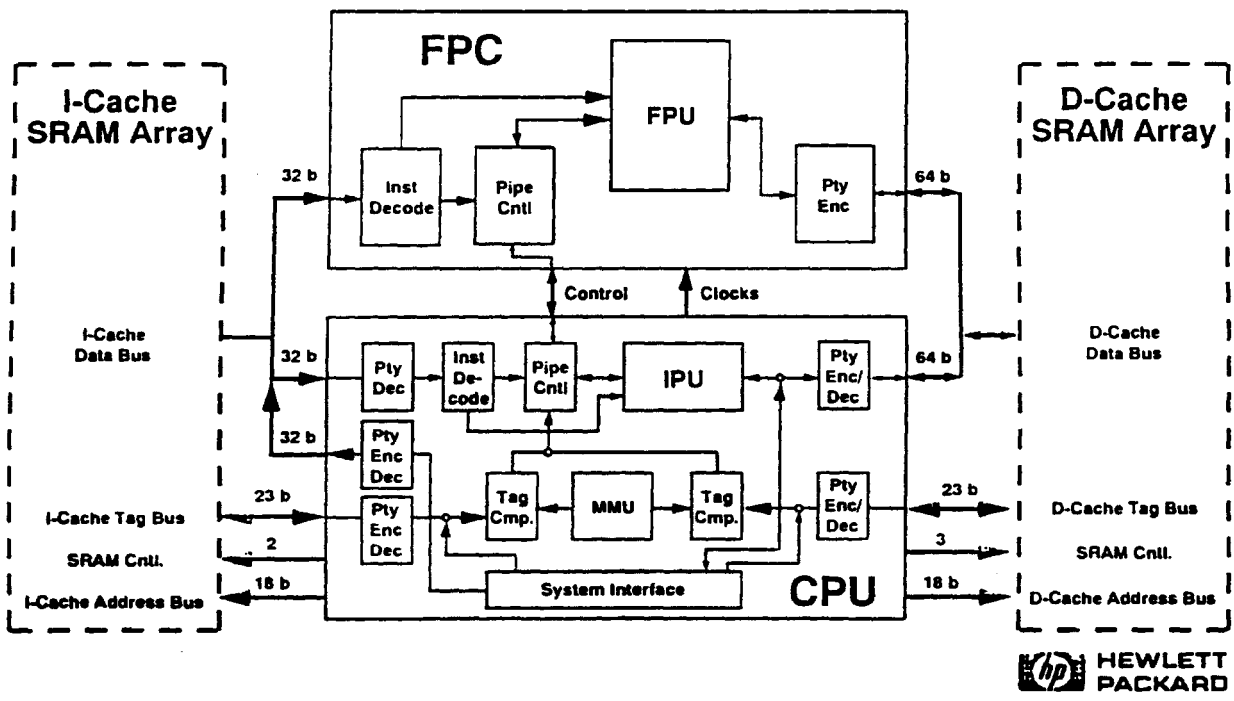
Partitioning of Functions



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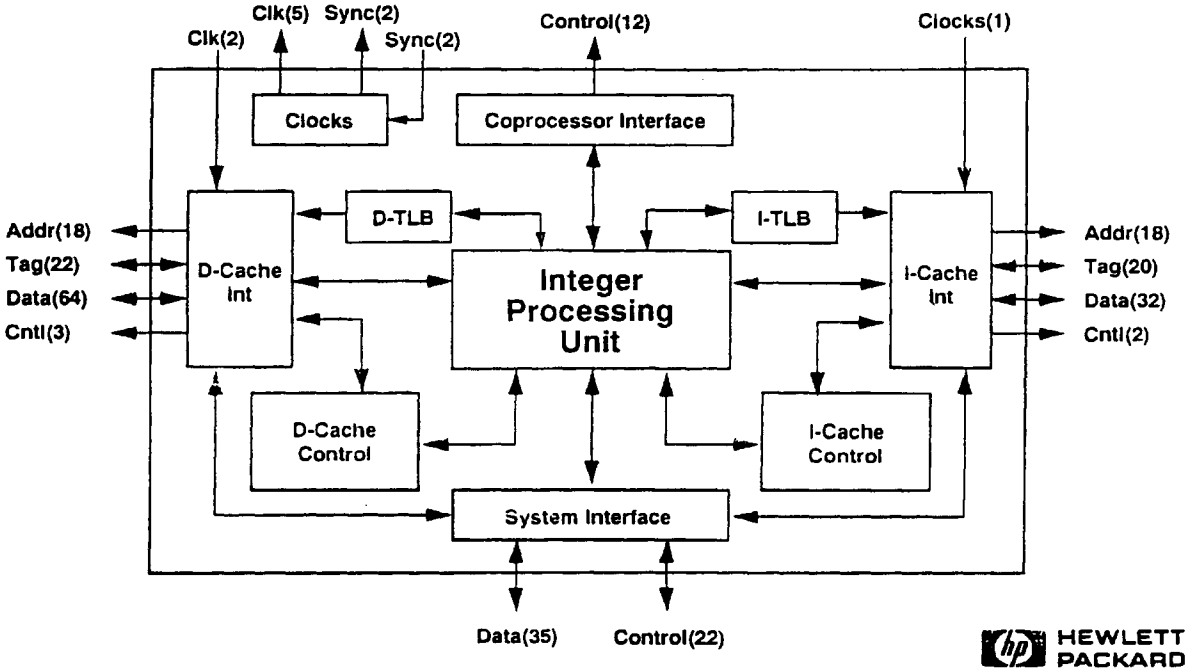
CPU Internal Block Diagram



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CPU Technology Overview

- VLSI Technology : 1.0/0.9 CMOS
- Transistors : 577K
- Die Size : 14.0 mm x 14.0 mm
- Interconnect : 1 Silicide Polysilicon
  3 Levels Al-Cu Metal
- Power Dissipation : < 8 W @ 66 MHz
- # Bonding Pads : 512
- Power Supply : 5.0 V (Internal)
  3.3 V (I/O Drivers)
- Package : 408 Pin Multilayer
  Ceramic PGA

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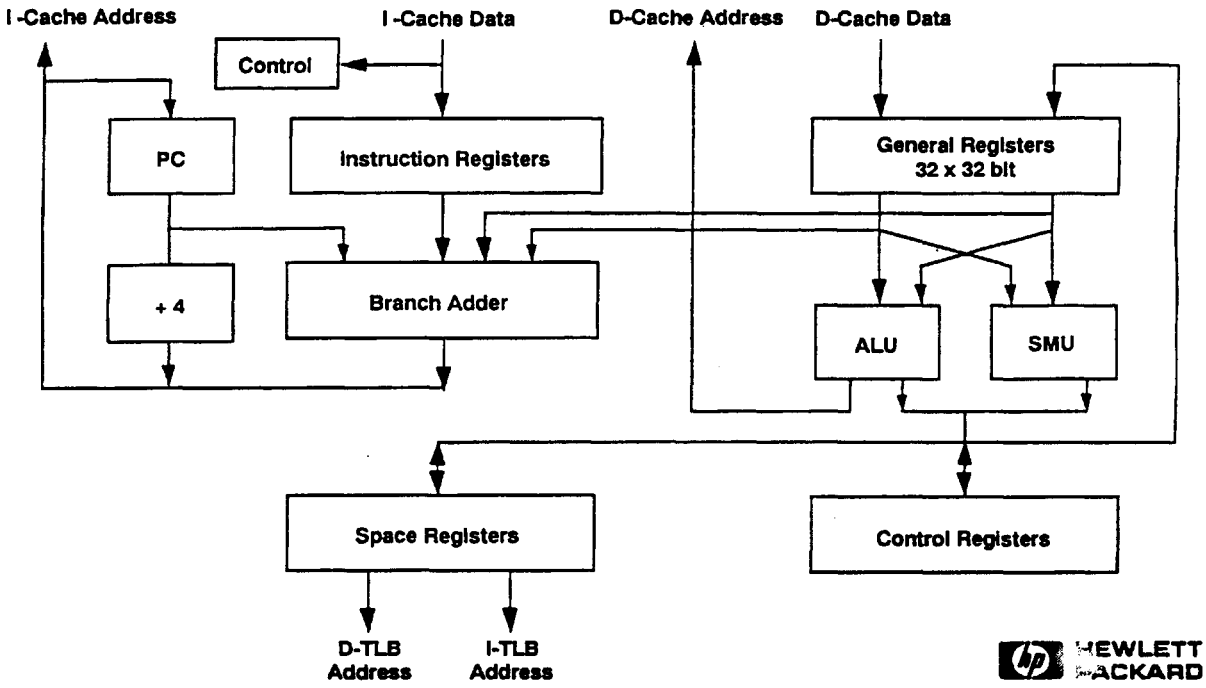
CPU Block Diagram: IPU Detail



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Instruction Pipeline

Inst. Fetch	Decode	Execute	Data Access	Register Write	Complete Store	
	Inst. Fetch	Decode	Execute	Data Access	Register Write	
		Inst. Fetch	Decode	Execute	Data Access	Register Write

Pipeline Penalties (Stalls):

Load-Use Penalty	-	1 Cycle
Branch Penalty	-	0-1 Cycles
Store Penalty	-	0-2 Cycles
Load Penalty	-	0 Cycles

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Performance-Timing Design

- High Clock Frequency was a Primary Design Goal
- Critical Timing paths Identified, Simulated, Tuned
- High Performance I/O Circuits and Packages are Critical
  - Reduced Voltage Swing Drivers w/ Subnanosecond Rise/Fall
  - Custom Ceramic PGA w/ Bypass Capacitors on Substrate
- Low Skew Clock Generation/Distribution
- Flow-Through Timing on External Cache
  - 66 MHz System w/ 12 ns SRAMs

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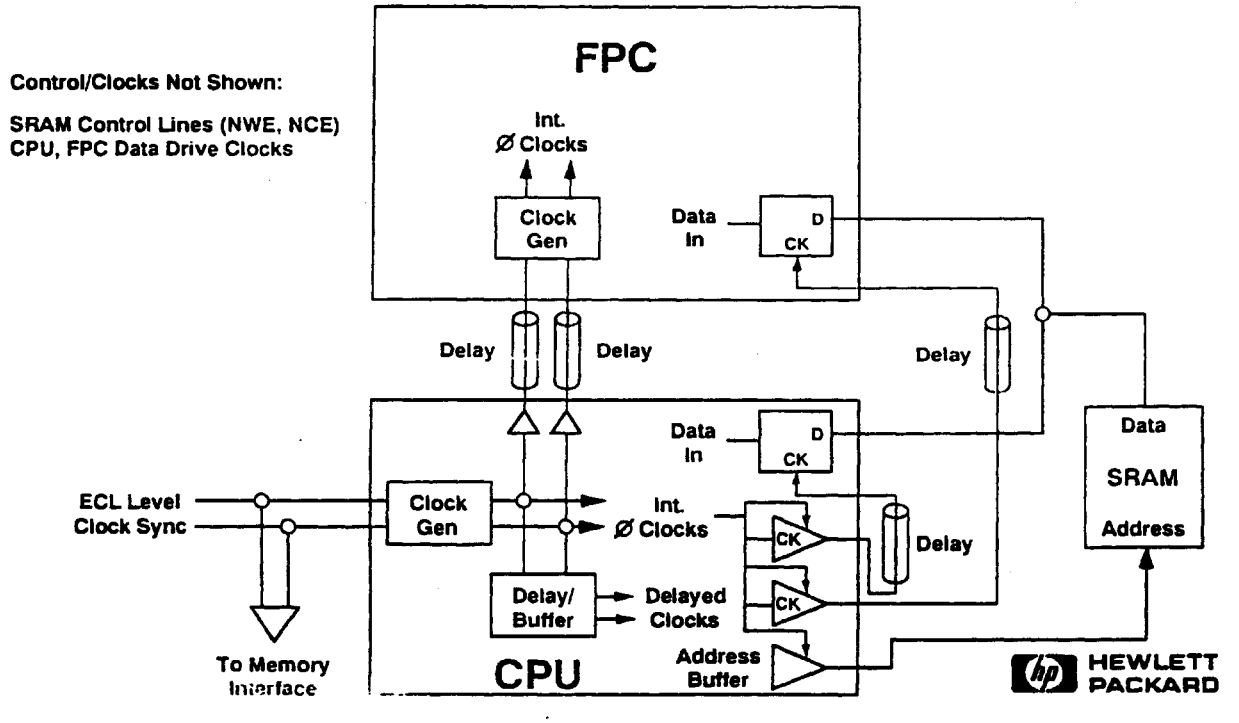
Clocking Diagram



CPU Functionality

- Integer Processing Unit
- Cache Control Unit
- Memory Management Unit
- System Interface
- Coprocessor Interface
- Test and Diagnose Hardware

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Performance Features
Integer Unit and Pipeline

- BRANCH Prediction Algorithm
  - No Penalty on Correctly Predicted Branches
- Extensive Bypassing to Minimize Stalls
- Concurrent Execution of Multicycle Instructions
- "Shadow" Registers for TLB Miss Traps
- Cache Streaming

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Performance Features
Cache Memories and TLBs

- Large, Separate Instruction and Data Caches
- 64 Bit Data Cache for High Bandwidth
- Cache Index Hashing Function
- Instruction Line Prefetching (in Memory Controller)
- High Speed System Bus for Cache Fills
- Dual 96 Page Entry, Fully Associative TLBs
- 8 Block TLB Entries Map 128 KB to 16 MB Spaces

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Performance Features
Floating Point Coprocessor

- Two fully Independent 64 b Functional Units (ALU + MUL/DIV/SQRT)
- Both Functional Units are Pipelined
- Large (32 x 64 b) FP Register File
- 5 Read Ports, 3 Write Ports on Register File
- Compound FP Instructions (MPY/ADD, MPY/SUB, MPY/CONVERT)
- Two Entry FP Instruction Queue

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Performance Features
Graphics Support

- Frame Buffer Mapped with Block TLB Entry
- Reciprocal Square Root and Clip Test Instructions
- Data Cache Prefetch for Display Lists
- Graphics Flush (Block Move) Instruction
- FP Register File Holds 64 Single-Precision Values
- Doubleword Loads/Stores Operate on Pairs of 32 Bit Values

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Summary
Key Contributions:

- High Clock Frequency in Low Cost CMOS Technology
- Exceptionally Large, Scalable Cache Memories
- Competitive Performance Achieved without:
  - High End Technology (ECL, GaAs)
  - High Density (> 1 M Transistor) Chip Designs
  - Multi-level Caches and TLBs
  - Superscalar or Superpipelined Instruction Execution
- Real, Proven Design and Implementation
  - Prototypes Produced since 5/90

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"SNAKES PROCESSOR" PERFORMANCE COMPARISONS

This slide will list the Snakes Workstation performance against existing competitive machines. Benchmark of SPEC, MIPS, LINPACK, and X-11 will be shared.

Conclusions

- PA-RISC Competitive in Workstation as well as Multiuser Implementations
- System Level Design Focus:
  - Balanced Application Performance versus Peak/Benchmark Performance
- Emphasis on Simplicity/Speed versus Complexity/Features
  - Improved Schedule/Cost/Reliability plus High Performance
- Solid Design/Technology Foundation on which to Build