MIPS R4000 Technical Overview

64 Bits/100 MHz or Bust

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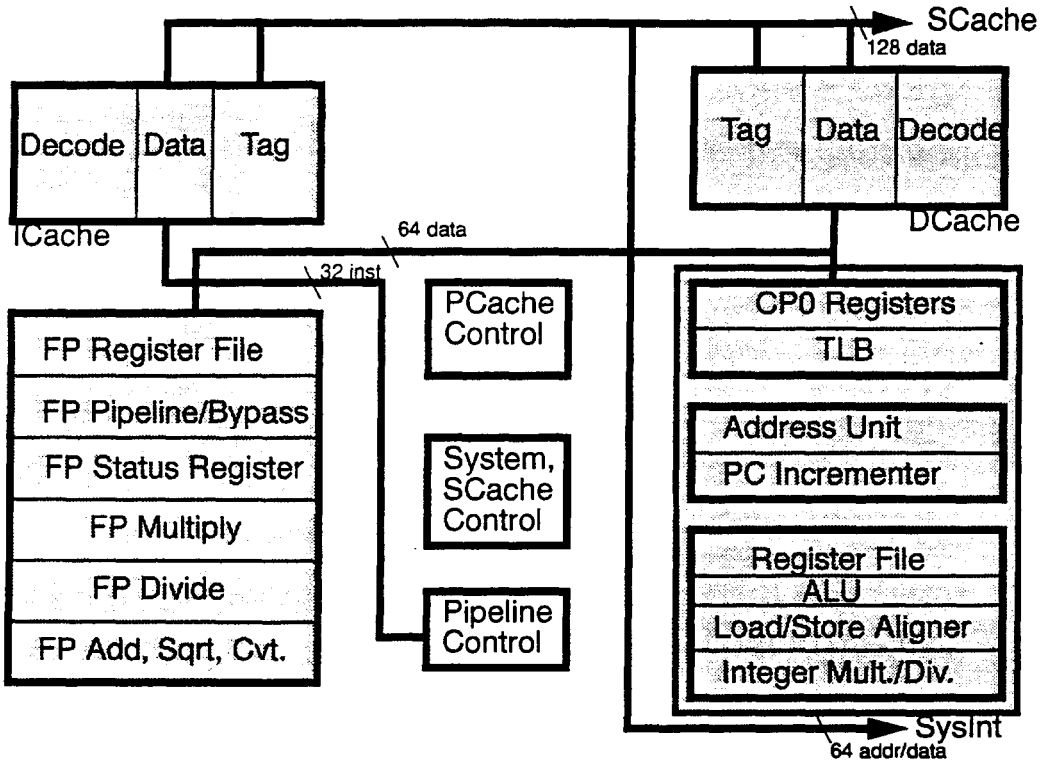
Overview

- Integrated I and D primary caches (8K->32K).
- Improved pipeline (<1/2 # of gates/cycle).
- Flexible system and secondary cache interface.
- Integrated floating point.
- Multi-processor support.
- 64 bit Integer Datapath and 64 bit TLB.

R4000 Block Diagram



R4000 Technology

- 1.0 micron CMOS technology.
- 2 Layer Metal technology.
- 1.3 Million transistors.
- 100 MHz internal clock.

MIPS R3000 Pipeline

Instruction Fetch

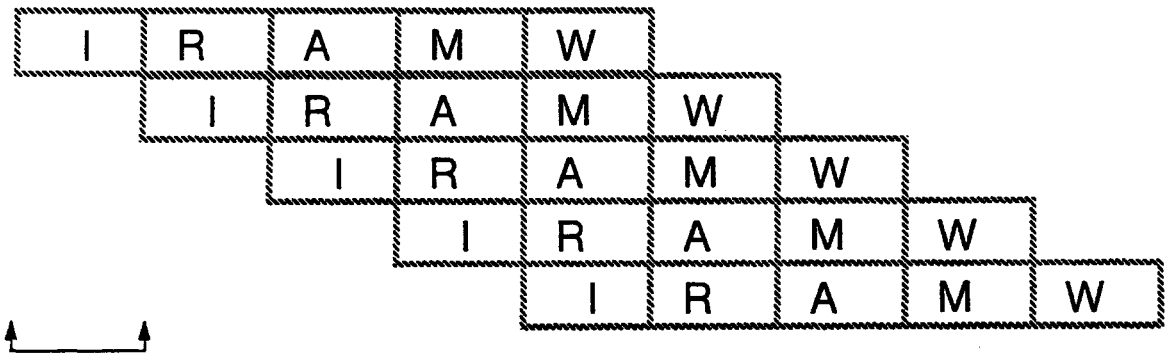
Register Access

ALU

Memory (cache)

Write (register)

MIPS R3000 Pipeline

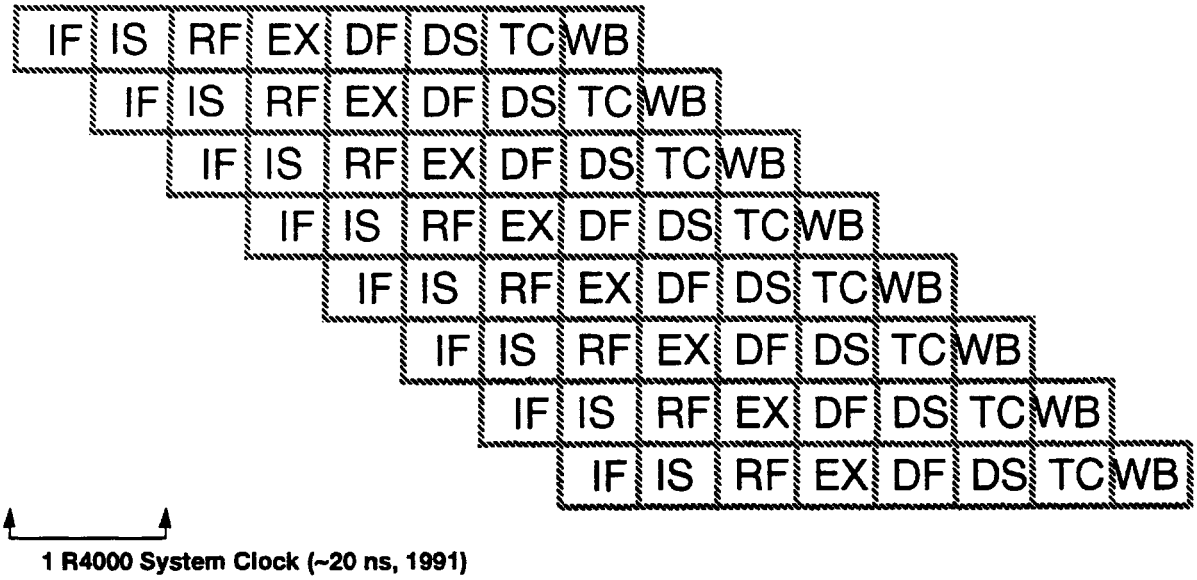


1 R3000 System Clock (~30 ns, 1990)

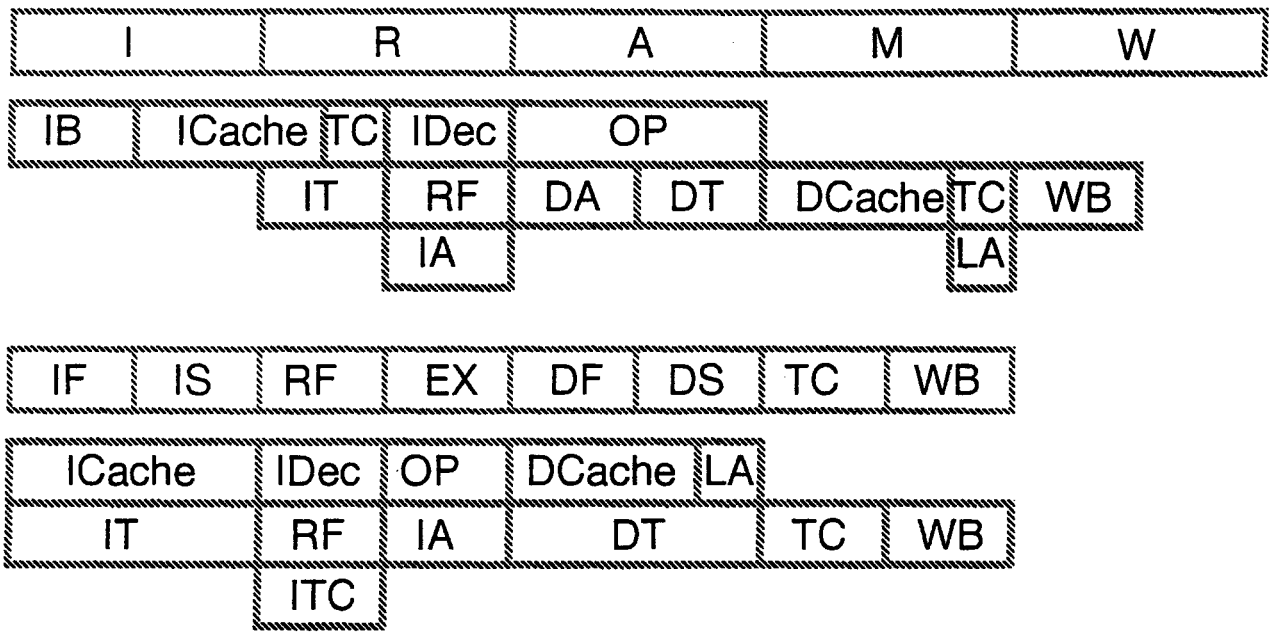
MIPS R4000 Pipeline

IF	Instruction Fetch
IS	
RF	Register Fetch
EX	Execution
DF	Data Access
DS	
TC	Tag Check
WB	Write Back (register)

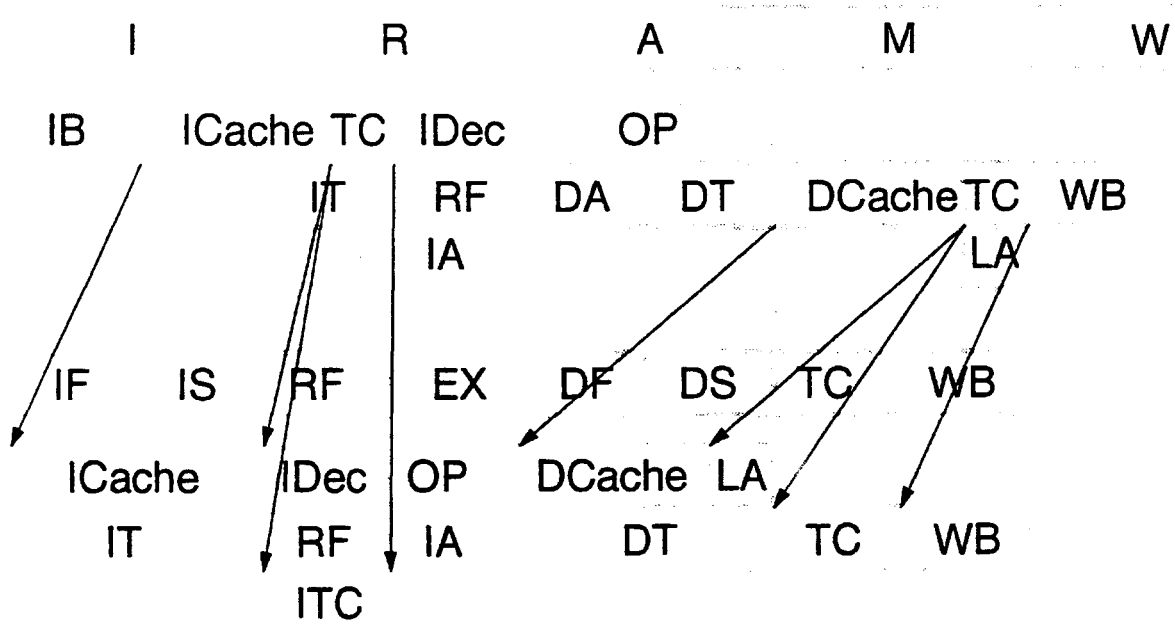
MIPS R4000 Pipeline



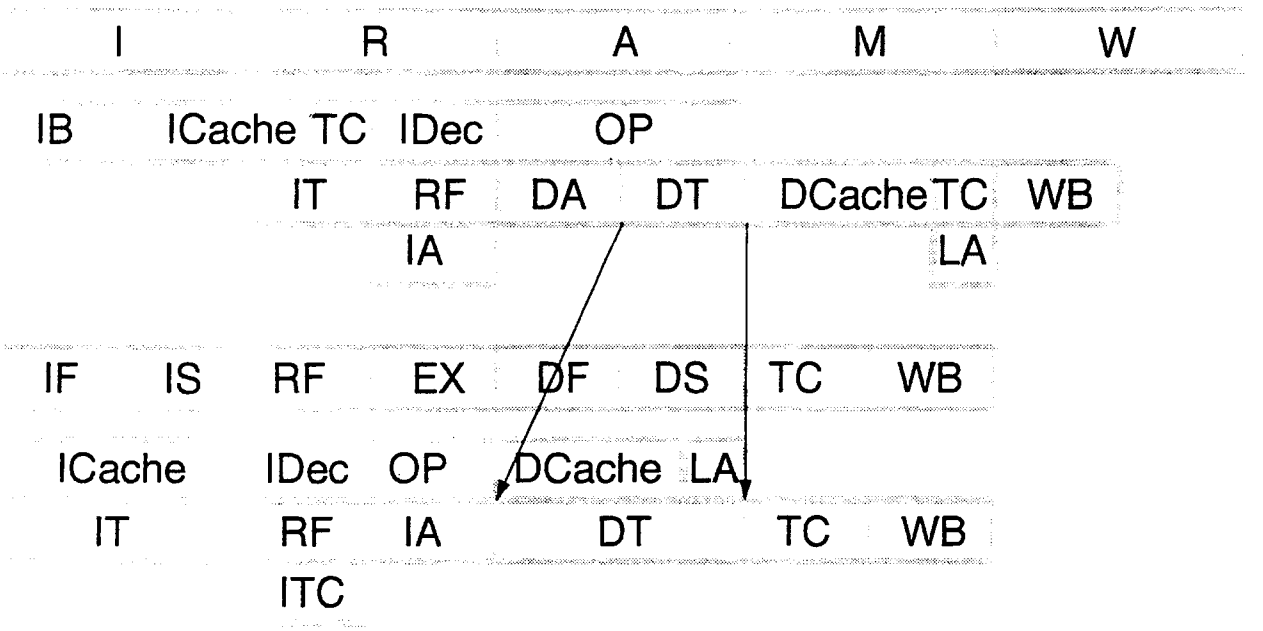
R3000 vs. R4000 Pipeline Details



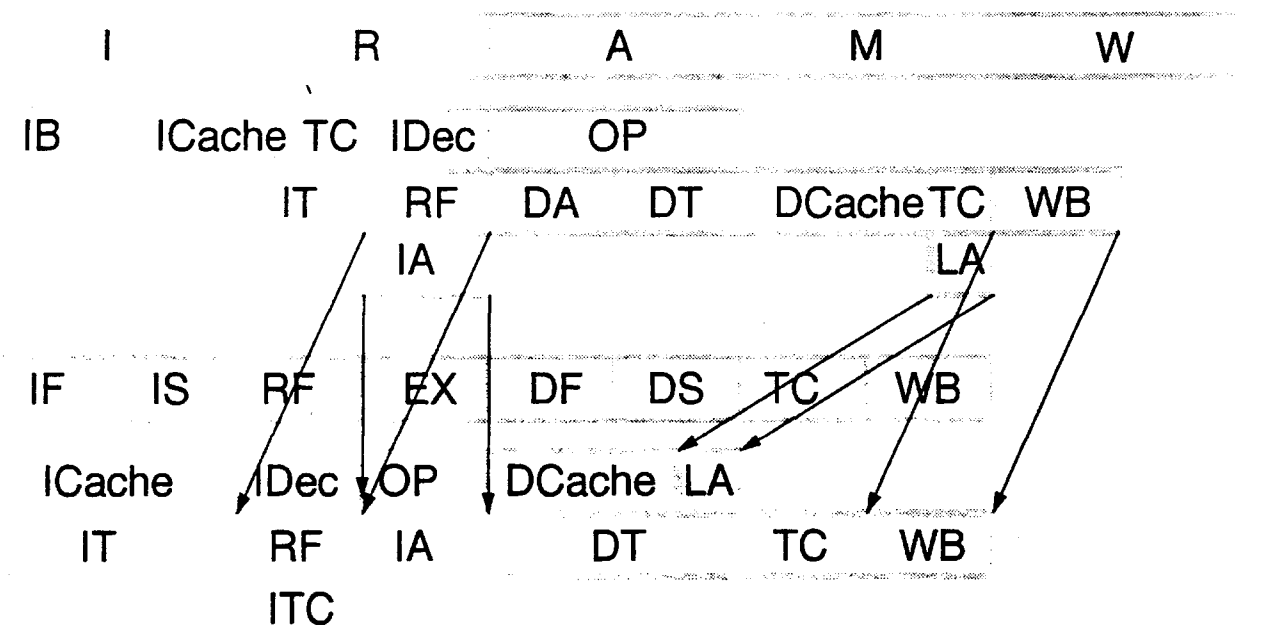
R3000 vs. R4000 Cache Access



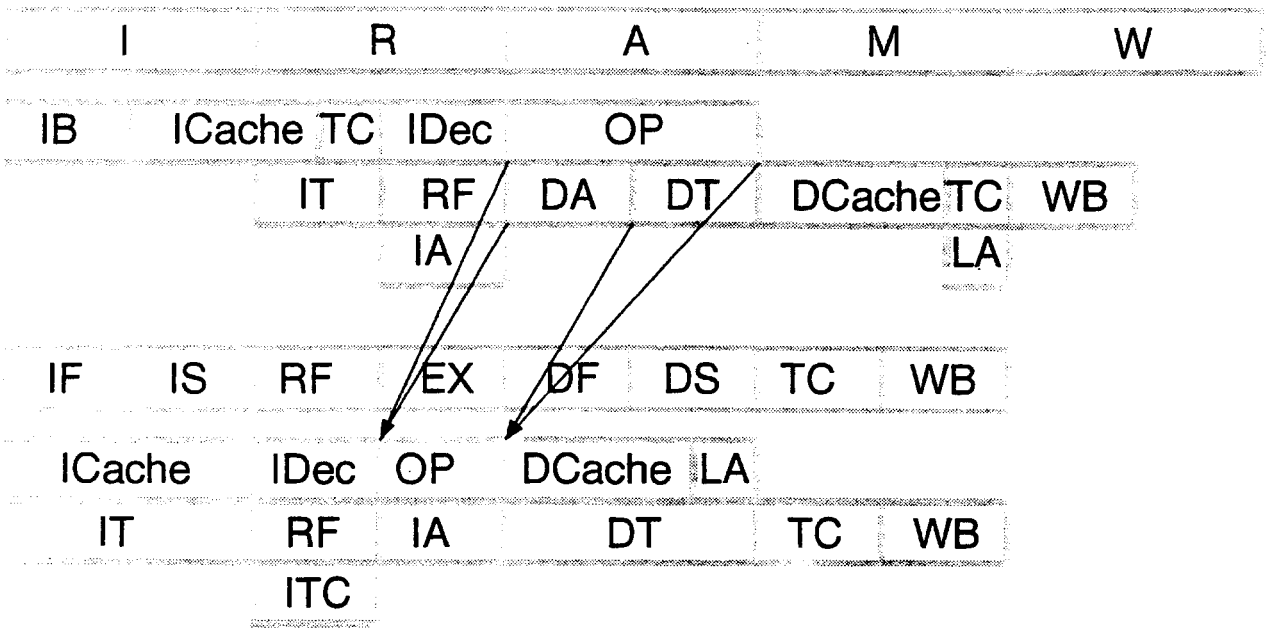
R3000 vs. R4000: Address Translation



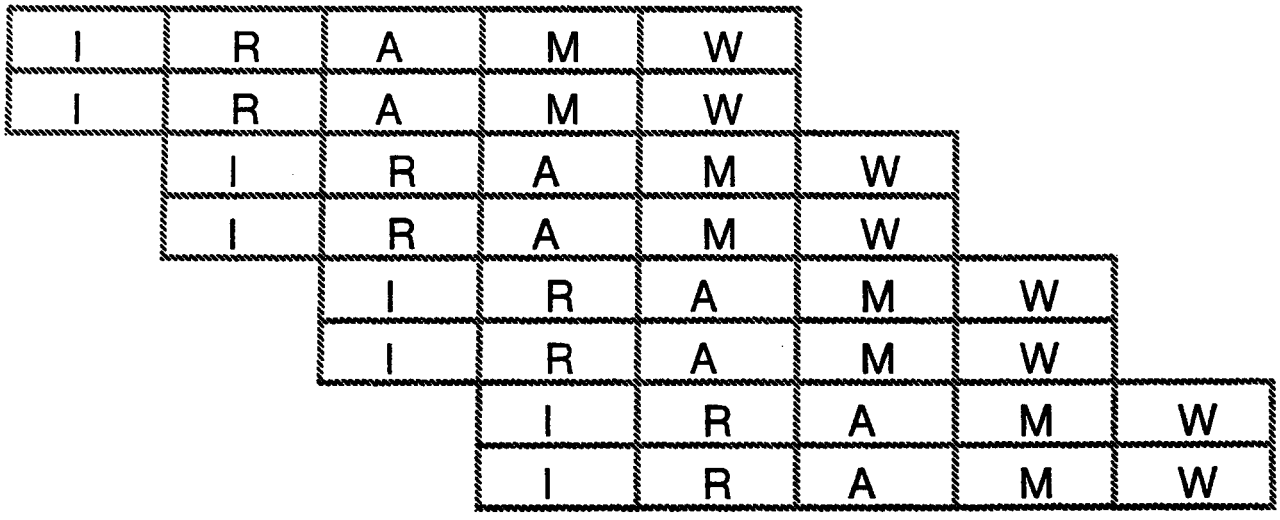
R3000 vs. R4000: Other operations



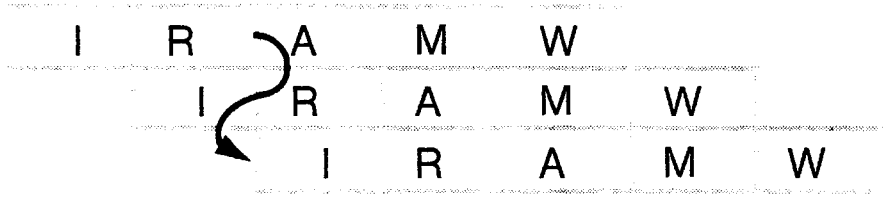
R3000 vs. R4000: ALU operations



Hypothetical MIPS Superscalar Pipeline



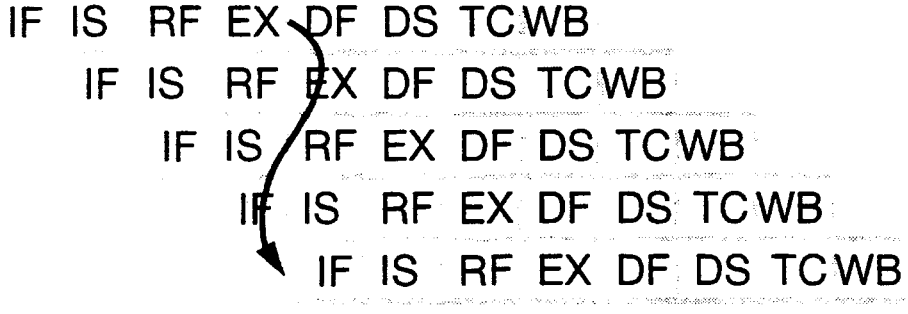
MIPS R3000 Branch Delay



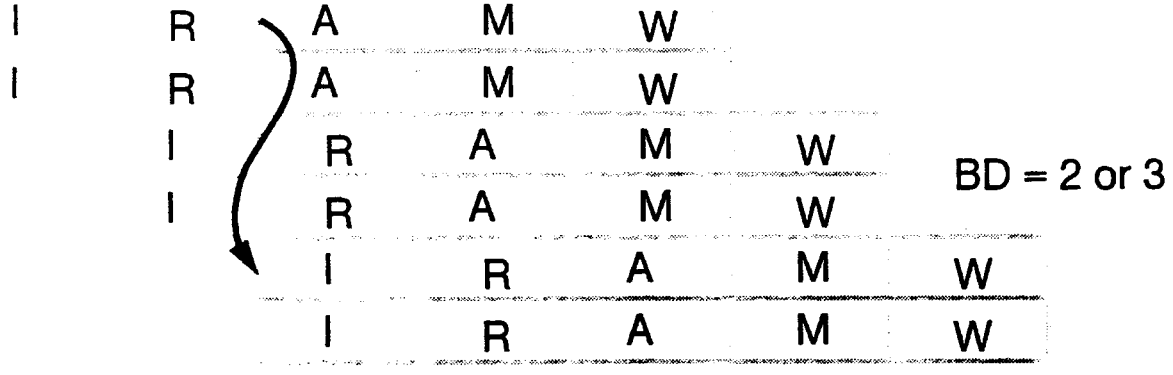
BD = 1

- One Branch Delay Cycle
- MIPS Architectural Branch Delay

R4000 v.s. Superscalar: Branch Delay

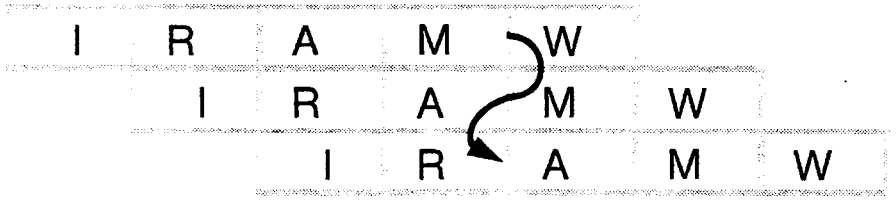


BD = 3



BD = 2 or 3

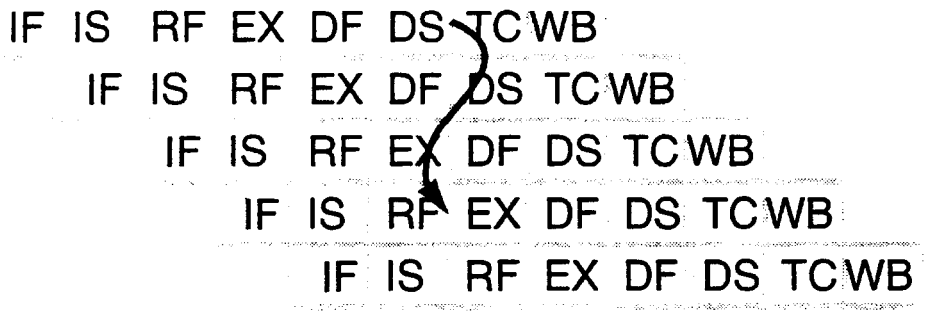
MIPS R3000 Load Delay



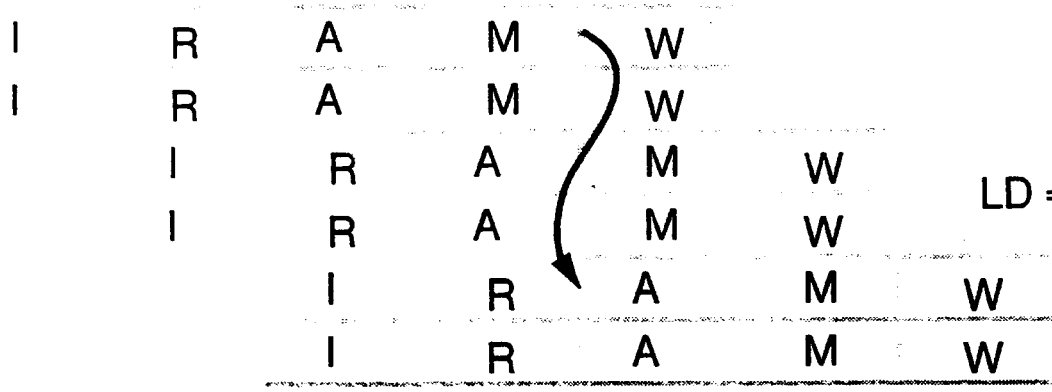
LD = 1

- One Load Delay Cycle
- MIPS Architectural Load Delay

R4000 v.s. Superscalar: Load Delay

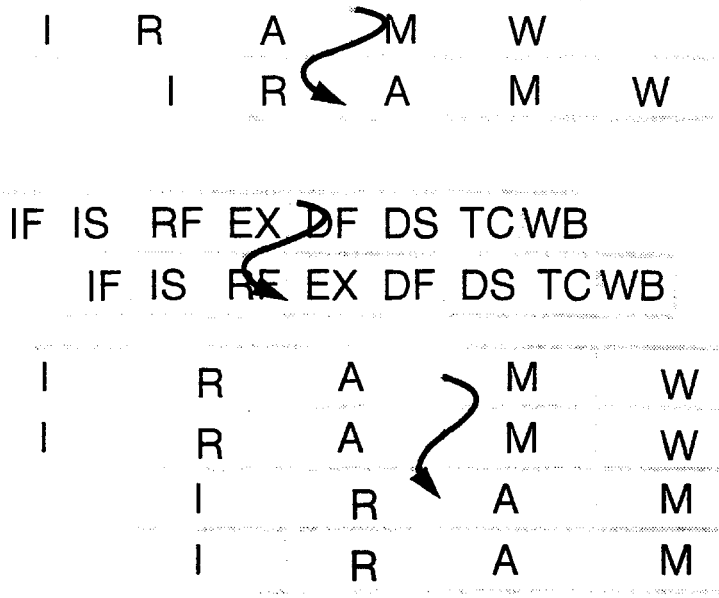


LD = 2



LD = 2 or 3

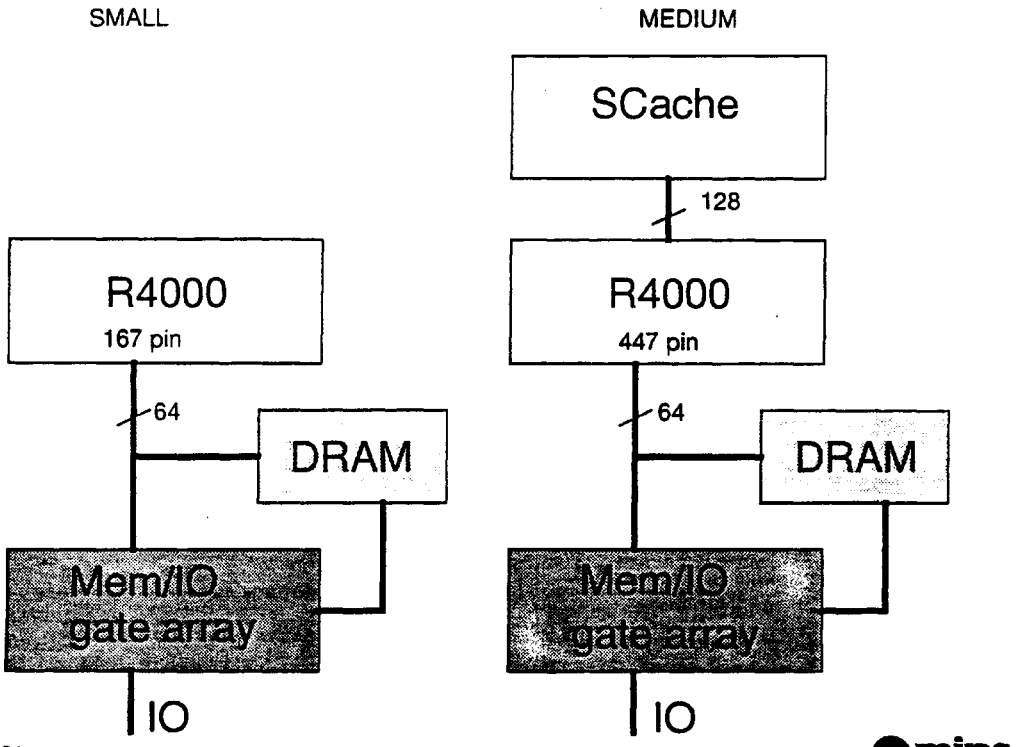
R3000, R4000 v.s. Superscalar: Dependent ALU ops



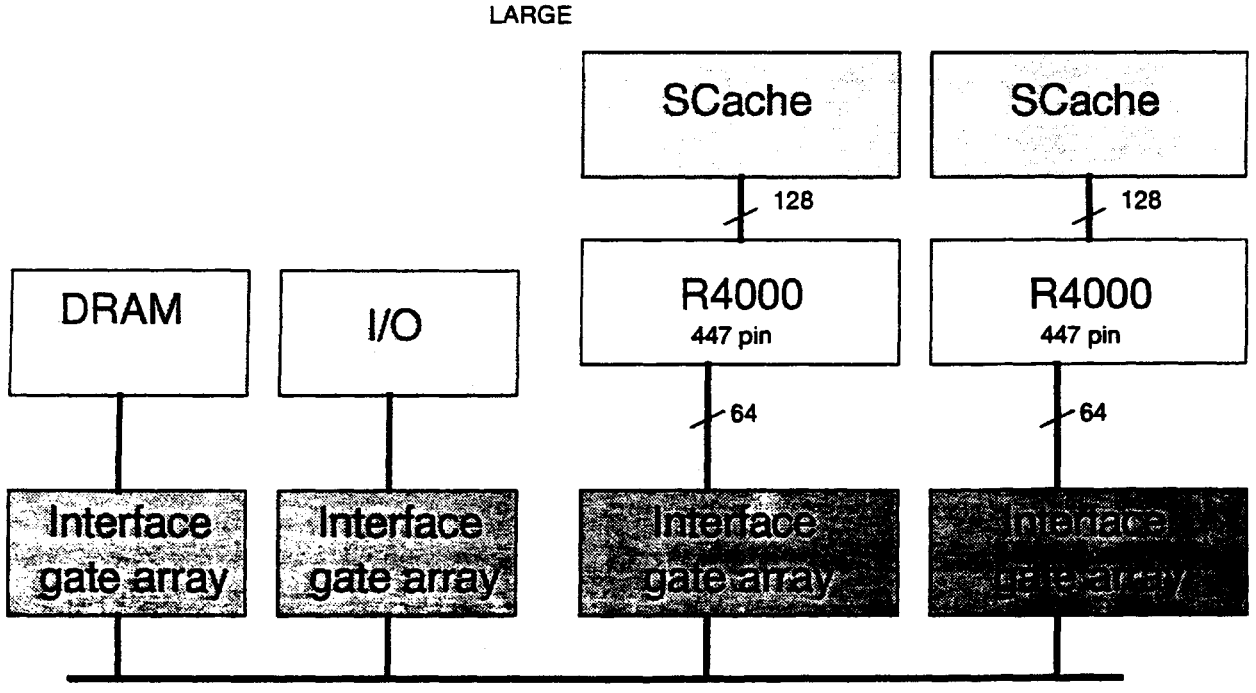
R4000 v.s. Superscalar: Other Issues

- R4000 can issue twice as many load/store insts.
- Fewer functional units required.
- Simpler pipeline controller.
- Fewer requirements on compiler .

R4000 Configurations



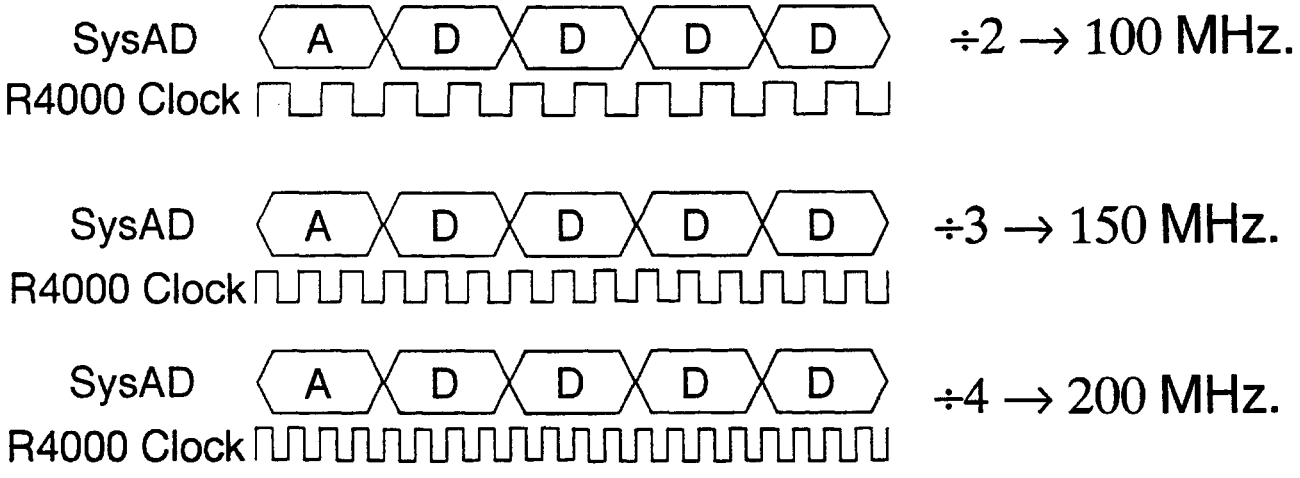
R4000 Configurations



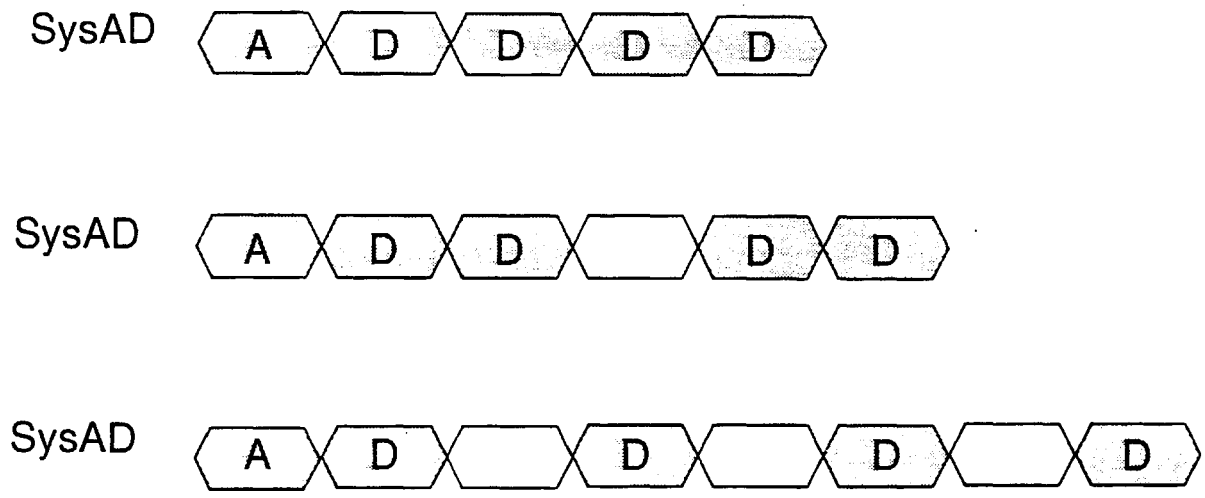
Flexible System Interface

- 64 bit wide System Interface for Addr/Data.
- Configurable clock divisors.
- Configurable transmit/receive data patterns.
- Overlapped operation for write back secondary cache systems.

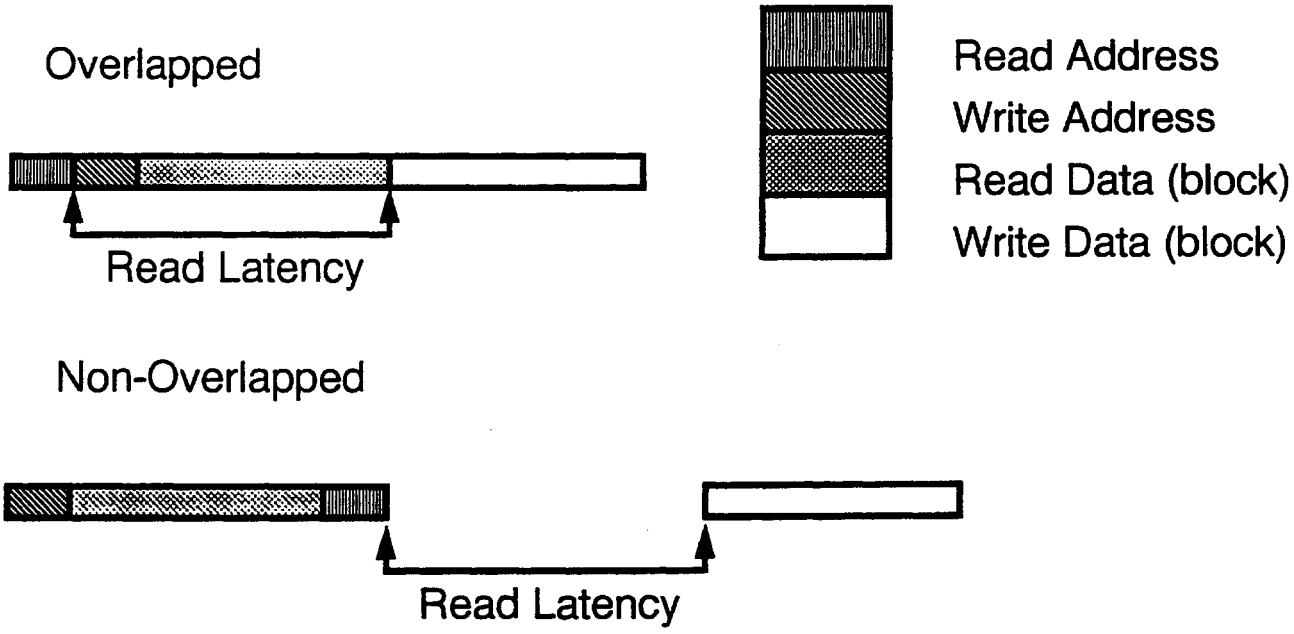
Configurable Clock Rates for 50 MHz interface



Configurable Transmit/Receive Patterns



Overlapped Operation v.s. Non-Overlapped Operation



Conclusion

- Third Generation RISC.
  Integrated Caches.
  Integrated Floating Point.
  64-Bit Datapath and TLB.
- Pipeline chosen for performance and economy.
- Flexible system interface for wide range of applications.