Super SPARC™

A Fully Integrated Superscalar Processor

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Program Objectives

Workstation Microprocessor Essentials	→ SuperSparc Solution
☐ High Performance	– 3 Instruction Resource-Rich SuperScalar – Fast Double-Precision Floating Point – Single Cycle Loads/Stores – BiCMOS
☐ 100% Application Binary Compatible	– SPARC Version 8 Architecture (IMUL/IDIV)
☐ High Integration	– IU/FPU/MMU/Cache/Mbus on-chip
☐ Useful in Several Configurations	– All Fully MP "ready" – Large Internal Caches – Companion Cache Controller
☐ Extensive Test/Debug Support	– Built-in Self Test – JTAG Scan Based Emulation – ICE-like debugging features

Super SPARC™

Microprocessor

- High Performance, Superscalar
- Highly Integrated
- 3.1 million transistors, BiCMOS
- 3 Instructions/Cycle Issue and Execution
- SPARC Version 8 Compatible
- Direct MBus Level II or used with External Cache Controller

Cache Controller

- Optional External Cache Controller
- Fully integrated, on-board cache tags
- Synch or Async interface to system bus
- 1MB unified, direct-mapped cache
- MBus Level-II Interface
  (Cache Consistent Multiprocessor Interconnect)

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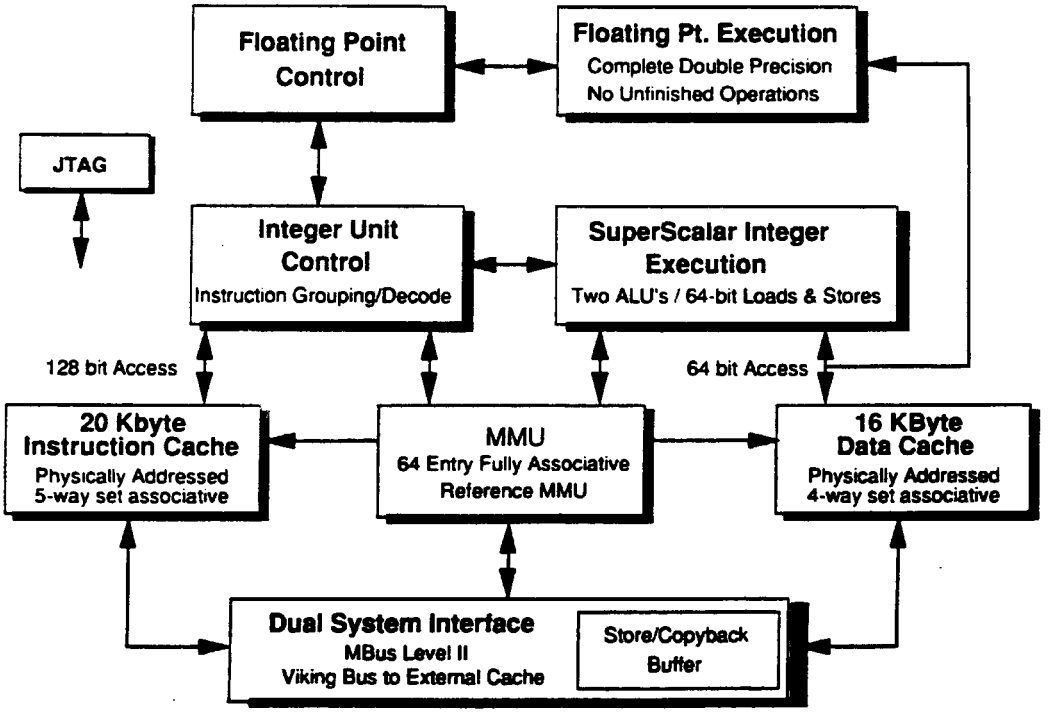
Super SPARC™



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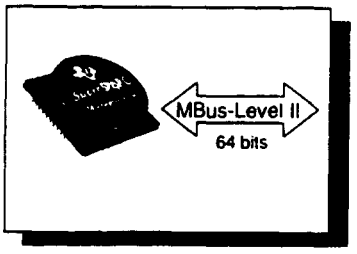
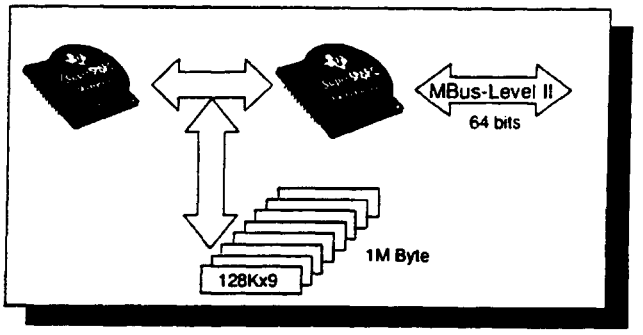
MBus Configurations

Lower Cost Systems



Higher Performance Systems



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Superscalar Principles of Operation

- 3 instruction/cycle issue & execute, fully dynamic scheduling
- Simulataneous execution may be constrained by:
  - data dependencies
  - control dependencies
  - internal resources
- SuperSPARC Resources:
  - Single 64-bit LD/ST
  - Two 32-bit ALUs
  - Single FP Issue
  - Single Br/Jmp/Call/Return
  - Two 32-bit integer results
- Designed to handle dependencies well, not wish them away

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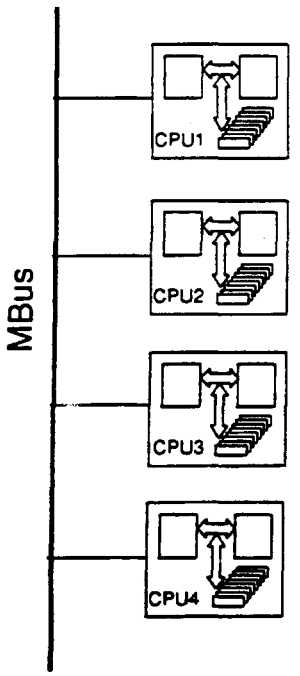
Superscalar Example

```
ldd          [%l0],%f2
faddd        %f2,%f0,%f6
add          %l0,0x8,%l0
! --- Break (Three instructions max)
ldd          [%l0],%f4
add          %l0,0x4,%l0
fmuld        %f4,%f0,%f8
! --- Break (Three instructions max)
ldd          [%l0+4],%f10
cmp          %l0,0x100
be           Loop
! --- Break (Branch, Three instructions)
faddd        %f6,%f8,%f0
.
.
```


MBus Multiprocessing



- SuperSPARC has complete multiprocessing support
- First and optional second level caches all coherent
- MBus interface has snoop logic
- Processor not affected by most snoop traffic
- System configuration, memory speed and applications, Limit number of processors that can be supported
- Supports SPARC Architecture Version 8 multiprocessor memory model (Total Store Ordering and Partial Store Ordering)

Technology

- SuperSPARC CPU and Cache Controller are manufactured in TI's EPIC IIB process
  - 0.8 micron minimum feature size
  - BiCMOS - Best of Bipolar and CMOS circuits
    - Bipolar: I/O and interconnect
    - CMOS: Density and simplicity
  - Triple Level Metal
- High Performance Dense Ceramic Pin Grid Array (CPGA) with heatsink
  - SuperSPARC CPU: 293 pins, 70 mil pin to pin
  - SuperSPARC CC: 369 pins, 70 mil pin to pin

Super SPARC™

Summary

- 3 instruction Superscalar groups and schedules instructions
- High integration of critical features gives higher performance at lower cost
- BiCMOS for the right balance of speed, density and simplicity
- MBus "multiprocessing ready"
- SPARC Architecture Version 8: 100% binary compatible