# HOT Chips III

*Stanford University*
*Palo Alto, California*
*August 26-27, 1991*

# Symposium

# Record
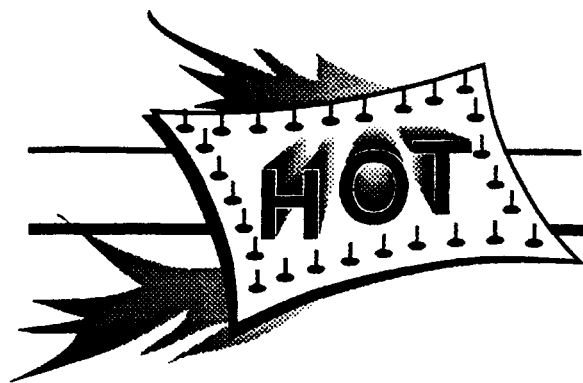
# HOT Chips III

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This is the third Hot Chips Symposium, and looking at the advanced registration figures, it certainly won't be the last. The first Hot Chips Symposium was the vision of Dr. Robert Stewart who wanted to provide the Silicon Valley engineer with the latest information on the hottest technical advancements, and to do it with a reasonable registration fee. We have tried to hold fast to this vision, and, as a result, we have had two previous very successful symposiums.

But, Hot Chips III has exceeded all of our expectations. The symposium has taken on an international perspective with many participants from all over the world. To accommodate a large registration we have had to move the symposium to a larger auditorium and have had to schedule all social functions out of doors.

This year we have added an evening panel session entitled, "Five Instructions Per Clock: Truth or Consequences." This session underscores the advances in technology that are the cornerstones of our "hottest" chips. These advances include superscalar, superpipeline and VLIW processor techniques.

Putting on a Hot Chips Symposium takes the dedication of many talented people. First, I would like to thank this year's Program Co-Chairmen Forest Baskett and John Hennessy who have assembled a first-rate program committee and have worked to put together a truly impressive program. Next, I would like to thank the Organizing Committee: Bob Stewart for the many hours he has spent making the local arrangements and handling the symposium registration, Andy Goforth for his efforts in getting the publicity out in a timely fashion in spite of many obstacles, Nam Ling for organizing the publications of the symposium proceedings, Hasan AlKhatib for handling the symposium finances. Special thanks are also due to Melissa Anderson and Elaine Grimes for their help in facilitating the work of both the Organizing Committee and the Program Committee. Finally, I would like to thank the Stanford University Department of Electrical Engineering for hosting the symposium, and, in particular, Professor Joseph Goodman for his support.

Martin Freeman
General Chairman
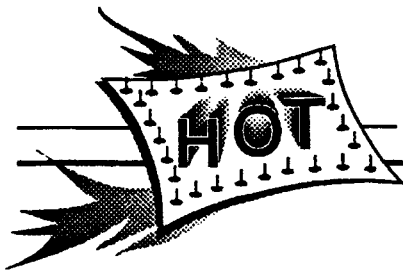
The development of high-performance processor chips continues to be one of the most exciting areas in the computer and electronics industries. The role played by such "hot chips" has expanded dramatically in the past few years. Everything from desktop machines to mainframes to large parallel super-computers are being constructed from these new high-performance integrated processors. In addition, many of the most interesting areas of development in software, from new operating systems and user interfaces to state-of-the-art optimizing compilers, focus on these processor chips.

This year the program committee has chosen 23 submissions for presentation. We encouraged designers to submit abstracts about chips in active develop-ment. Unfortunately, in a few cases this meant that the talks have had to be withdrawn.

While processor chips occupy a significant fraction of the program this year, we also have a number of interesting papers on special purpose processors, highly parallel processors, communications, caches, and floating point. In addition, there are several papers describing how to build systems whose performance is hot, but whose power demands and costs are "cool." We expect that several of these hot chips will be described in longer papers in an issue of *IEEE Micro* in 1992.

Last year's conference was a tremendous success, filling the capacity of the presentation hall. As we go to press, current preregistration is larger than last year's total registration and we are moving to larger quarters. The success of this conference stems not only from the exciting work going on in this field, but also from the enormous efforts of the organization committee and staff. They took care of an incredible number of details (including changing the conference facility a few weeks before the conference), which made it possible for us to focus on the program. We want to thank the committee, together with everyone who submitted a paper to Hot Chips III.

But most all we want to thank the program committee for helping to solicit and review the papers. Their efforts made the job of chairing the program committee an enjoyable experience.

Forest Baskett and John Hennessy
Program Committee Co-Chairmen

# August 26, 1991 — Memorial Hall Auditorium

**8:30 – 8:45**  **Welcome and Opening Remarks**
Martin Freeman, General Chair
Forest Baskett and John Hennessy, Program Co-Chairs

**8:45 – 10:15**  **Session 1:  High-Performance Processors – 1**
Session Chair: John Hennessy, Stanford University
- **SuperSPARC™:  A Fully Integrated Superscalar Processor**
  Greg Blanck, Sun Microsystems
  Steve Krueger, Texas Instruments
- **MIPS R4000 Technical Overview**
  Earl Killian, MIPS Computer Systems
- **PA-RISC Processor for "Snakes" Workstation**
  Charles Kohlhardt, Hewlett Packard

**10:15 – 10:45**  **Break**

**10:45 – 12:15**  **Session 2:  Highly Parallel Chips**
Session Chair: Martin Freeman, Philips Research
- **The LIFE Family of High-Performance Single Chip VLIWs**
  Gerrit Slavenburg and Yen Lee, Philips Research Palo Alto
  Andrew Huang, CMU
- **The Message-Driven Processor**
  - William Dally, J. Stuart Fiske, Waldemar Horwat, John Keen,
    Richard Lethin, Michael Noakes and Peter Nuth
    MIT Artificial Intelligence Laboratory
  - D. Scott Wills, University of Central Florida
  - Andrew Chien, University of Illinois
  - Salim Ahmed, Paul Carrick, Roy Davison, Greg Fyler
    Steve Lear, Mark Vestrich and Teg Nguyen, Intel
- **The TRW CPUAX Superchip**
  A. Miscione, R. Almeida, H. Hennecke and R. Mann
  TRW Electronics and Technology Division

**12:15 – 1:45**  **Lunch at Wilbur Hall Canopy**

**1:45 – 3:15**  **Session 3:  High-Performance Processors – 2**
Session Chair: Forest Baskett, Silicon Graphics
- **An 80 MHz 64-Bit Floating Point RISC Processor
  with Direct DRAM Support**
  James Hesson, Micron Technology
- **The I860™ XP: 2nd Generation of the I860™
  Supercomputing Microprocessor Family**
  David Perlmutter and Michael Kagan, Intel Israel
- **Beyond Claims of Free Transistors and Abundant
  Instruction-Level Parallelism**
  Michael Smith, Stanford University

**3:15 – 3:45**  **Break**

**3:45 – 5:15**  **Session 4:  Low Power and Low Cost**
Session Chair: Alan Smith, U.C. Berkeley
- **Tera microCORE Chipset**
  Greg Favor, Tera Microsystems
- **The SparKIT™ Chipset**
  Mohammed Wasfi, LSI Logic Corporation
- **SPARCore Modules**
  Raju Vegesna, Ross Technology

**5:15 – 7:15**  **Reception at Wilbur Hall Canopy**

**7:30**  **Evening Panel Session**
**Five Instructions Per Clock:  Truth or Consequences**
Session Chairs: Alan Smith, U.C. Berkeley and John Mashey, MIPS
Computer Systems
Panelists: Joseph A. Fisher, Hewlett Packard Laboratories; Norm Jouppi,
DEC Western Research Lab; Monica Lam, Stanford University; James
Smith, Cray Research; David Wall, DEC Western Research Lab
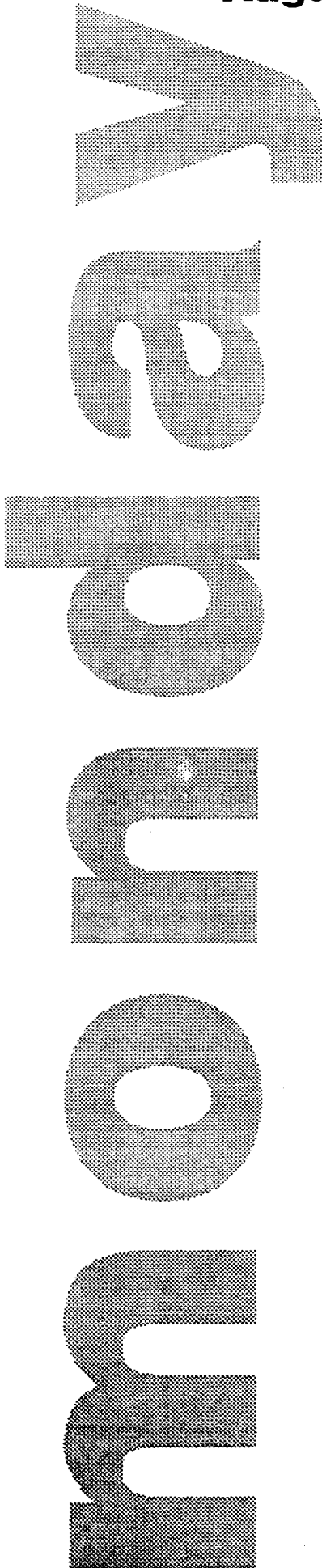
**9:00 – 10:30**  **Session 5:  Communications**
Session Chair:  Teresa Meng, Stanford University
- **A GaAs 200 Mbps 64x64 Crosspoint Chip**
  Ron Cates, Vitesse Semiconductor
- **An Enhanced Crossbar Router Chip for a Shared Memory Multiprocessor**
  Henry Minsky, Tom Knight and André DeHon, MIT AI Lab
- **The NEURON Chip Family Architecture**
  Robert Dolin, Echelon
- **The Protocol Engine Chipset**
  Des Young, Protocol Engines

**10:30 – 11:00**  **Break**

**11:00 – 12:30**  **Session 6:  Caches and Floating Point**
Session Chair:  John Crawford, Intel
- **MIPS R4000 Caches and Coherency**
  Paul Ries, MIPS Computer Systems
- **The Megacell Differentiated Floating Point Product Family**
  Merrick Darley, Don Steiss, Peter Groves, David Bural
  Maria Gill and Tod Wolf, Texas Instruments
- **82495DX/82490DX: A High-Performance 2nd Level Cache for the I486™ DX CPU**
  Adi Gobert, Intel Corporation

**12:30 – 2:00**  **Lunch at Wilbur Hall Canopy**

**2:00 – 3:30**  **Session 7:  Special Processors**
Session Chair:  John Mashey, MIPS Computer System
- **A Smart Frame Buffer**
  Joel McCormack, DEC Western Research Laboratory
  Bob McNamara and Lindsay Gage, DEC
- **CNAPS (Connected Network of Adaptive ProcessorS)**
  Dan Hammerstrom and Gary Tahara, Adaptive Solutions
- **SMM, The "Virtual 386™ "**
  Dave Vannier, Intel

**3:30 – 4:00**  **Break**

**4:00 – 5:00**  **Session 8:  High-Performance Processors – 3**
Session Chair:  Dave Ditzel, Sun Microsystems
- **National's Swordfish — A Superscalar with DSP**
  Reuven Marko and Motti Beck, National Semiconductor
- **T9000 — Superscalar Transputer**
  Bob Krysiak, Richard Forsyth and Roger Shepherd
  INMOS Ltd. — SGS-Thomson Microelectronics

**5:00**  **Closing Remarks**

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## Organizing Committee

**General Chairman:**
Martin Freeman, Philips Research
**Program Co-Chairmen:**
Forest Baskett, Silicon Graphics
John Hennessy, Stanford University
**Treasurer:**
Hasan AlKhatib, Santa Clara University

**Registration Chairman and Local Arrangements Chairman:**
Robert Stewart, Stewart Research
**Publicity Chairman:**
Andre Goforth, NASA Ames Research Center
**Publication Chairman:**
Nam Ling, Santa Clara University

## Program Committee

**Co-Chairmen:  Forest Baskett, Silicon Graphics**
John Crawford, Intel
David Ditzel, Sun Microsystems
John Mashey, MIPS Computer Systems

**John Hennessy, Stanford University**

**Teresa Meng, Stanford University**
Alan Smith, U.C. Berkeley